

FAN4822 ZVS Average Current PFC Controller

Features

- Average current sensing, continuous boost, leading edge PFC for low total harmonic distortion and near unity power factor
- Built-in ZVS switch control with fast response for high efficiency at high power levels
- Average line voltage compensation with brownout control
- Current fed gain modulator improves noise immunity and provides universal input operation
- Overvoltage comparator eliminates output "runaway" due to load removal
- UVLO, current limit, and soft-start
- Precision 1.3% reference

General Description

The FAN4822 is a PFC controller designed specifically for high power applications. The controller contains all of the functions necessary to implement an average current boost PFC converter, along with a Zero Voltage Switch (ZVS) controller to reduce diode recovery and MOSFET turn-on losses.

The average current boost PFC circuit provides high power factor (>98%) and low Total Harmonic Distortion (THD). Built-in safety features include undervoltage lockout, overvoltage protection, peak current limiting, and input voltage brownout protection.

The ZVS control section drives an external ZVS MOSFET which, combined with a diode and inductor, soft switches the boost regulator. This technique reduces diode reverse recovery and MOSFET switching losses to reduce EMI and maximize efficiency.

Block Diagram



Pin Configuration



Pin Description (Pin numbers is parentheses are for 16-pin package)

Pin	Name	Function	
1 (1)	VEAO	Transconductance voltage error amplifier output.	
2 (2)	IEAO	Transconductance current error amplifier output.	
3 (3)	ISENSE	Current sense input to the PFC current limit comparator.	
4 (4)	IAC	PFC gain modulator reference input.	
5 (5)	VRMS	Input for RMS line voltage compensation.	
6 (6)	RTCT	Connection for oscillator frequency setting components.	
7 (7)	ZV SENSE	Input to the high speed zero voltage crossing comparator.	
8 (10)	GND	Analog signal ground.	
9 (11)	PWR GND	Return for the PFC and ZVS driver outputs.	
10 (12)	ZVS OUT	ZVS MOSFET driver output.	
11 (13)	PFC OUT	PFC MOSFET driver output.	
12 (14)	Vcc	Shunt-regulated supply voltage.	
13 (15)	REF	Buffered output for the internal 7.5V reference.	
14 (16)	FB	Transconductance voltage error amplifier input.	

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min	Max	Unit
Shunt Regulator Current (I _{CC})		55	mA
Peak Driver Output Current		±500	mA
Analog Inputs	-0.3	7	V
Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Lead Temperature (Soldering, 10 sec)		150	°C
Thermal Resistance (θ _{JA}) Plastic DIP Plastic SOIC		80 110	°C/W °C/W

Operating Conditions

Temperature Range	Min.	Max.	Units	
FAN4822IX	-40	85	°C	

Electrical Characteristics

Unless otherwise specified, $R_T = 52.3k\Omega$, $C_T = 470pF$, $T_A = Operating Temperature Range (Note 1)$

Parameter	Conditions	Min.	Тур.	Max.	Units
Voltage Error Amplifier					
Input Voltage Range		0		7	V
Transconductance	VNON-INV = VINV, VEAO = 3.75V	50	70	120	μΩ
Feedback Reference Voltage	VEAO = VFB	2.4	2.5	2.6	V
Open Loop Gain		60	75		dB
PSRR	VCCZ - 3V < VCC < VCCZ - 0.5V	60	75		dB
Output Low			0.65	1	V
Output High		6.0	6.7		V
Source Current	$\Delta V_{IN} = \pm 0.5 V, V_{OUT} = 6 V$	-40	-80		μA
Sink Current	$\Delta VIN = \pm 0.5 V$, VOUT = 1.5V	40	80		mA
Current Error Amplifier					
Input Voltage Range		-1.5		2	V
Transconductance	$V_{NON-INV} = V_{INV}$, IEAO = 3.75V	130	195	310	hΩ
Input Offset Voltage			±3	±15	mV
Open Loop Gain		60	75		dB
PSRR	VCCZ - 3V < VCC < VCCZ - 0.5V	60	75		dB
Output Low			0.65	1	V
Output High		6.0	6.7		V
Source Current	$\Delta V_{IN} = \pm 0.5 V, V_{OUT} = 6 V$	-30	-80		μΑ
Sink Current	$\Delta V_{IN} = \pm 0.5 V, V_{OUT} = 1.5 V$	40	80		μΑ
OVP Comparator					
Threshold Voltage		2.6	2.7	2.8	V
Hysteresis		80	120	150	mV
ISENSE Comparator					
Threshold Voltage		-0.8	-1.0	-1.15	V
Delay to Output			150	300	ns
ZV Sense Comparator					
Propagation Delay	100mV Overdrive			50	ns
Threshold Voltage		7.35	7.5	7.65	V
Input Capacitance			6		pF

Electrical Characteristics (Continued)

Unless otherwise specified, $R_T = 52.3k\Omega$, $C_T = 470pF$, $T_A = Operating Temperature Range (Note 1)$

Gain (Note 2) IAC = 100mA, VVRMS = 0V, VFB = 0V 0.36 0.51 0.66 IIAC = 50mA, VVRMS = 1.2V, VFB = 0V 1.20 1.72 2.24 IIAC = 100µA, VVRMS = 1.8V, VFB = 0V 0.55 0.78 1.01 IIAC = 100µA, VVRMS = 3.3V, VFB = 0V 0.14 0.20 0.26 Bandwidth IIAC = 250µA 0.14 0.20 0.26 Output Voltage VFB = 0V, VVRMS = 1.15V, IIAC = 20µA 0.72 0.8 0.9 V Oscillator IIAC = 250µA 10 MHz % % Temperature Stability VCC 2 - 3V <vcc -="" 0.5v<="" 2="" <="" td="" vcc=""> 1 % % Total Variation Line, temperature 72 89 KHz Ramp Valley to Peak Voltage 2.5 V % Output Voltage TA = 25°C, IREF = 1MA 7.4 7.5 7.6 V Dead Time 100 300 450 ns c 15 mV Load Regulation VCC2 - 3V < VCC < 0.5V 2 10 mV Load Regulation</vcc>	Parameter	Conditions	Min.	Тур.	Max.	Units
Gain (Note 2) IAC = 100mA, VVRMS = 0V, VFB = 0V 0.36 0.51 0.66 IIAC = 50mA, VVRMS = 1.2V, VFB = 0V 1.20 1.72 2.24 IIAC = 100µA, VVRMS = 1.8V, VFB = 0V 0.55 0.78 1.01 IIAC = 100µA, VVRMS = 3.3V, VFB = 0V 0.14 0.20 0.26 Bandwidth IIAC = 250µA 10 MHz Output Voltage VFB = 0V, VVRMS = 1.15V, IIAC = 250µA 0.72 0.8 0.9 V Socillator 11A 50µA 2 % % % Temperature Stability VCC2 - 3V < VCC < VCC2 - 0.5V	Gain Modulator					
$\begin{tabular}{ c c c c c c } \begin{tabular}{ c c c c c c c } line (= 100\mu A, VVRMS = 1.2V, VFB = 0V & 1.72 & 2.24 \\ \hline VFB = 0V & 0.55 & 0.78 & 1.01 \\ \hline VFB = 0V & 0.55 & 0.78 & 1.01 \\ \hline VFB = 0V & VVRMS = 1.3V, V0.14 & 0.20 & 0.26 \\ \hline VFB = 0V, VVRMS = 1.15V, IAC = & 0.72 & 0.8 & 0.9 \\ \hline Output Voltage & VFB = 0V, VVRMS = 1.15V, IAC = & 0.72 & 0.8 & 0.9 \\ \hline Output Voltage & VFB = 0V, VVRMS = 1.15V, IAC = & 0.72 & 0.8 & 0.9 \\ \hline Oscillator & & & & & & & & & & & & & & & & & & &$	Gain (Note 2)	IIAC = 100mA, VVRMS = 0V, VFB = 0V	0.36	0.51	0.66	
$\begin{tabular}{ c $		IIAC = 50mA, VVRMS = 1.2V, VFB = 0V	1.20	1.72	2.24	
$\begin{tabular}{ c $		IIAC = 100μA, V _{VRMS} = 1.8V, V _{FB} = 0V	0.55	0.78	1.01	
Bandwidth IIAC = 250μA 10 MHz Output Voltage VFB = 0V, VVRMS = 1.15V, IIAC = 2.0,8 0.9 V Oscillator 250μA 0.72 0.8 0.9 V Initial Accuracy TA = 25°C 74 80 87 KHz Voltage Stability VCC2 - 3V < VCC < VCC2 - 0.5V		I _{IAC} = 100μA, V _{VRMS} = 3.3V, V _{FB} = 0V	0.14	0.20	0.26	
Output Voltage VFB = 0V, VVRMS = 1.15V, IIAC = 0.72 0.8 0.9 V Oscillator Initial Accuracy TA = 25°C 74 80 87 kHz Voltage Stability VCCZ - 3V < VCC < VCCZ - 0.5V 1 % Temperature Stability VCCZ - 3V < VCC < VCCZ - 0.5V 1 % Temperature Stability Line, temperature 72 89 kHz Ramp Valley to Peak Voltage C 2.5 V V Dead Time 100 300 450 ns C _T Discharge Current TA = 25°C, IREF = 1mA 7.4 7.5 7.6 V Line Regulation VCCZ - 3V < VCC < VCCZ - 0.5V 2 10 mV Load Regulation 1mA < IREF, < 20mA 7.4 7.5 7.6 V Load Regulation Ime, load, and temperature 7.35 7.65 V Load Regulation Ime, load, and temperature 7.35 7.65 V Long Term Stability Tj = 125°C, 1000 hours 5 25<	Bandwidth	IIAC = 250μA		10		MHz
Oscillator Initial Accuracy TA = 25°C 74 80 87 kHz Voltage Stability VCCZ - 3V < VCC < VCCZ - 0.5V	Output Voltage	VFB = 0V, VVRMS = 1.15V, IIAC = 250μA	0.72	0.8	0.9	V
Initial Accuracy TA = 25°C 74 80 87 kHz Voltage Stability VCCZ - 3V < VCC < VCCZ - 0.5V	Oscillator					
Voltage Stability VCCZ - 3V < VCC < VCCZ - 0.5V 1 1 % Temperature Stability Ine, temperature 2 % Total Variation Line, temperature 72 89 kHz Ramp Valley to Peak Voltage 72 89 kHz Dead Time 100 300 450 ns Cr Discharge Current 100 300 450 ns Reference 100 300 450 ns Output Voltage TA = 25°C, IREF = 1mA 7.4 7.5 7.6 V Load Regulation VCCZ - 3V < VCC < VCCZ - 0.5V	Initial Accuracy	$T_A = 25^{\circ}C$	74	80	87	kHz
Temperature Stability Line, temperature 2 % Total Variation Line, temperature 72 89 kHz Ramp Valley to Peak Voltage 2.5 V Dead Time 100 300 450 ns Cr Discharge Current 4.5 7.5 9.5 mA Reference 7.4 7.5 7.6 V Output Voltage TA = 25°C, IREF = 1mA 7.4 7.5 7.6 V Load Regulation VCCZ - 3V < VCC < VCCZ - 0.5V	Voltage Stability	$V_{CCZ} - 3V < V_{CC} < V_{CCZ} - 0.5V$		1		%
Total Variation Line, temperature 72 89 kHz Ramp Valley to Peak Voltage 2.5 V Dead Time 100 300 450 ns Cr Discharge Current 4.5 7.5 9.5 mA Reference	Temperature Stability			2		%
Ramp Valley to Peak Voltage 2.5 V Dead Time 100 300 450 ns Cr Discharge Current 4.5 7.5 9.5 mA Reference 4.5 7.5 9.5 mA Output Voltage TA = 25°C, IREF = 1mA 7.4 7.5 7.6 V Line Regulation VCCZ - 3V < VCC < VCCZ - 0.5V	Total Variation	Line, temperature	72		89	kHz
Dead Time Information Information <thinformation< th=""> Information</thinformation<>	Ramp Valley to Peak Voltage			2.5		V
Cr Discharge Current 4.5 7.5 9.5 mA Reference	Dead Time		100	300	450	ns
Reference Output Voltage $T_A = 25^{\circ}C$, $I_{REF} = 1mA$ 7.4 7.5 7.6 V Line Regulation $VCCZ - 3V < VCC < VCCZ - 0.5V$ 2 10 mV Load Regulation $1mA < I_{REF}$, $< 20mA$ 2 15 mV Temperature Stability Image: constraint of the stability 0.4 % % Total Variation Line, load, and temperature 7.35 7.65 V Long Term Stability Tj = 125^{\circ}C, 1000 hours 5 25 mV Short Circuit Current VCC < VCCZ - 0.5V, VREF = 0V	C _T Discharge Current		4.5	7.5	9.5	mA
$\begin{tabular}{ c c c c c c } \hline $T_A = 25^\circ$C, $I_REF = 1mA$ 7.4 7.5 7.6 V $$Line Regulation $VCCZ - 3V < VCC < VCCZ - 0.5V$ $$2$ 10 mV $$Load Regulation $1mA < I_REF, < 20mA$ $$2$ $$15$ mV $$$Temperature Stability $$1mA < I_REF, < 20mA$ $$2$ $$15$ mV $$$$$$0.4$ $$10$ $$1mA < I_REF, < 20mA$ $$2$ $$15$ mV $$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$$	Reference			!		1
$\begin{tabular}{ c c c c c c } \hline \begin{tabular}{ c c c c } Line Regulation & VCCZ - 3V < VCC < VCCZ - 0.5V & 2 & 10 & mV \\ \hline \begin{tabular}{ c c c c c c } Line Regulation & ImA < IREF, < 20mA & 0.4 & 2 & 15 & mV \\ \hline \begin{tabular}{ c c c c c } Temperature Stability & ImA < IREF, < 20mA & 0.4 & 0.4 & \% \\ \hline \begin{tabular}{ c c c c c } Total Variation & Line, load, and temperature & 7.35 & 7.65 & V \\ \hline \begin{tabular}{ c c c } Line, load, and temperature & 7.35 & 7.65 & V \\ \hline \begin{tabular}{ c c c } Long Term Stability & Tj = 125^\circC, 1000 hours & 5 & 25 & mV \\ \hline \begin{tabular}{ c c c c } Short Circuit Current & VCC < VCCZ - 0.5V, VREF = 0V & -15 & -40 & -100 & mA \\ \hline \begin{tabular}{ c c c c c c } PFC Comparator & VIEAO > 6.7V & 0 & 0 & \% \\ \hline \begin{tabular}{ c c c c c c c } Minimum Duty Cycle & VIEAO > 6.7V & 90 & 95 & 0.6 & \% \\ \hline \begin{tabular}{ c c c c c c c } MOSFET Driver Outputs & VIEAO < 1.2V & 90 & 95 & 0.6 & \% \\ \hline \begin{tabular}{ c c c c c c c } MOSFET Driver Outputs & VIEAO < 1.2V & 90 & 95 & 0.4 & \% \\ \hline \begin{tabular}{ c c c c c c c } IOUT = -20mA & 0.4 & 1.0 & V \\ IOUT = -100mA & 1.5 & 3.5 & V \\ IOUT = -10mA, VCC = 8V & 0.8 & 1.5 & V \\ \hline \begin{tabular}{ c c c c c c } IOUT = 20mA & 9.5 & 10.3 & V \\ \hline \begin{tabular}{ c c c c c c c } IOUT = 100mA & 9 & 10.3 & V \\ \hline \begin{tabular}{ c c c c c c c c c c c } IOUT = 100mA & 9 & 10.3 & V \\ \hline \begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Output Voltage	T _A = 25°C, I _{REF} = 1mA	7.4	7.5	7.6	V
$\begin{tabular}{ c c c c c } \hline Load Regulation & 1mA < IREF, < 20mA & 2 & 15 & mV \\ \hline Temperature Stability & Image - 2 & 0.4 & 0.4 & 0.4 \\ \hline Total Variation & Line, load, and temperature & 7.35 & 7.65 & V \\ \hline Long Term Stability & Tj = 125°C, 1000 hours & 5 & 25 & mV \\ \hline Short Circuit Current & V_{CC} < V_{CCZ} - 0.5V, V_{REF} = 0V & -15 & -40 & -100 & mA \\ \hline PFC Comparator & & & & & & & & & & & & & & & & & & &$	Line Regulation	VCCZ – 3V < VCC < VCCZ – 0.5V		2	10	mV
$\begin{tabular}{ c c c c c } \hline Temperature Stability & Line, load, and temperature & 7.35 & 7.65 & V \\ \hline Total Variation & Line, load, and temperature & 7.35 & 7.65 & V \\ \hline Long Term Stability & Tj = 125°C, 1000 hours & 5 & 25 & mV \\ \hline Short Circuit Current & VCC < VCCZ - 0.5V, VREF = 0V & -15 & -40 & -100 & mA \\ \hline PFC Comparator & & & & & & & & & & & & & & & & & & &$	Load Regulation	1mA < IREF, < 20mA		2	15	mV
$\begin{tabular}{ c c c c c c } \hline Total Variation & Line, load, and temperature & 7.35 & 7.65 & V \\ $Long Term Stability & T_{j} = $125^{\circ}C$, $1000 hours & 5 & 25 & mV \\ \hline Short Circuit Current & V_{CC} < V_{CC} - $0.5V$, V_{REF} = $0V$ & -15 & -40 & -100 & mA \\ \hline $PFC \ Comparator & V_{IEAO} > $6.7V$ & -15 & -40 & 0 & $\%$ \\ \hline $Maximum Duty Cycle & V_{IEAO} > $6.7V$ & 90 & 95 & $\%$ & $\%$ \\ \hline $MosFET \ Driver \ Outputs & V_{IEAO} < $1.2V$ & 90 & 95 & $\%$ & $$MOSFET \ Driver \ Output Low Voltage & I_{OUT} = $-20mA$ & 0.4 & 1.0 & V & $$I_{OUT}$ = $-100mA$ & 1.5 & 3.5 & V & I_{OUT} = $-10mA$, V_{CC} = $8V$ & 0.8 & 1.5 & V & $$Output High Voltage & I_{OUT} = $20mA$ & 9.5 & 10.3 & V & $$I_{OUT}$ = $100mA$ & 9 & 10.3 & V & $$Output Rise/Fall Time & CL = $1000pF$ & 40 & ns & $$Undervoltage Lockout & $$UDT = $-20mA$ & 0.4 & 1.5 & V & $$0.5$ & 10.3 & V & $$0.5$ & 10.5 & V & $$0.5$ & V & 0.5 & V & 0.5 & V & 0.5 & V	Temperature Stability			0.4		%
$\begin{tabular}{ c c c c c c } \hline T_{j} = 125°C, 1000 hours & 5 & 25 & mV \\ \hline $Short Circuit Current & $V_{CC} < V_{CCZ} - 0.5V, V_{REF} = 0V & -15 & -40 & -100 & mA \\ \hline $PFC Comparator $ & $V_{IEAO} > 6.7V & $100 hours & $V_{IEAO} > 6.7V & 0 & $	Total Variation	Line, load, and temperature	7.35		7.65	V
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	Long Term Stability	Tj = 125°C, 1000 hours		5	25	mV
PFC Comparator Minimum Duty Cycle $V_{IEAO > 6.7V$ 0 % Maximum Duty Cycle $V_{IEAO < 1.2V$ 90 95 % MOSFET Driver Outputs 0UT = -20mA 0.4 1.0 V Output Low Voltage IOUT = -20mA 0.4 1.5 3.5 V IOUT = -100mA 0.8 1.5 V V Output High Voltage IOUT = 20mA 9.5 10.3 V Output High Voltage IOUT = 20mA 9.5 10.3 V Output Rise/Fall Time CL = 1000pF 40 ns Undervoltage Lockout V V V	Short Circuit Current	$V_{CC} < V_{CCZ} - 0.5V, V_{REF} = 0V$	-15	-40	-100	mA
$\begin{tabular}{ c c c c c c c } \hline Minimum Duty Cycle & VIEAO > 6.7V & 90 & 95 & 0 & \% \\ \hline Maximum Duty Cycle & VIEAO < 1.2V & 90 & 95 & 0 & \% \\ \hline \mbox{MOSFET Driver Outputs} & & & & & & & & & & & & & & & & & & &$	PFC Comparator					1
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Minimum Duty Cycle	VIEAO > 6.7V			0	%
$\begin{tabular}{ c c c c c } \hline MOSFET Driver Outputs \\ \hline Output Low Voltage & IOUT = -20mA & 0.4 & 1.0 & V \\ \hline IOUT = -100mA & 1.5 & 3.5 & V \\ \hline IOUT = -10mA, V_{CC} = 8V & 0.8 & 1.5 & V \\ \hline IOUT = -10mA, V_{CC} = 8V & 0.8 & 1.5 & V \\ \hline IOUT = 20mA & 9.5 & 10.3 & V \\ \hline IOUT = 100mA & 9 & 10.3 & V \\ \hline IOUT = 100mA & 9 & 10.3 & V \\ \hline Output Rise/Fall Time & CL = 1000pF & 40 & ns \\ \hline Undervoltage Lockout & V & V \\ \hline V & V & V & V \\ \hline V$	Maximum Duty Cycle	VIEAO < 1.2V	90	95		%
$ \begin{array}{c c c c c c c c c c c c c c c c c c c $	MOSFET Driver Outputs				1	
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	Output Low Voltage	IOUT = -20mA		0.4	1.0	V
$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$		IOUT = -100mA		1.5	3.5	V
Output High Voltage IOUT = 20mA 9.5 10.3 V IOUT = 100mA 9 10.3 V Output Rise/Fall Time CL = 1000pF 40 ns Undervoltage Lockout V V V		$I_{OUT} = -10 \text{mA}, V_{CC} = 8 \text{V}$		0.8	1.5	V
IOUT = 100mA 9 10.3 V Output Rise/Fall Time CL = 1000pF 40 ns Undervoltage Lockout V V V	Output High Voltage	IOUT = 20mA	9.5	10.3		V
Output Rise/Fall Time CL = 1000pF 40 ns Undervoltage Lockout		IOUT = 100mA	9	10.3		V
Undervoltage Lockout	Output Rise/Fall Time	CL = 1000pF		40		ns
	Undervoltage Lockout					
Threshold Voltage VCCZ - VCCZ - VCCZ - V 0.9 0.6 0.2 V	Threshold Voltage		VCCZ - 0.9	VCCZ - 0.6	VCCZ - 0.2	V
Hysteresis 2.4 2.9 3.45 V	Hysteresis		2.4	2.9	3.45	V

Electrical Characteristics (Continued)

Unless otherwise specified, $R_T = 52.3k\Omega$, $C_T = 470pF$, $T_A = Operating Temperature Range (Note 1)$

Parameter	Conditions	Min.	Тур.	Max.	Units	
Supply	Supply					
Shunt Voltage (V _{ccz})	ICC =25mA	12.8	13.5	14.2	V	
Load Regulation	25mA < ICC < 55mA		±150	±300	mV	
Total Variation	Load and temperature	12.4		14.6	V	
Start-up Current	VCC < 12.3V		0.7	1.1	mA	
Operating Current	$V_{CC} = V_{CCZ} - 0.5V$		22	28	mA	

Notes

1. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

2. Gain = K x 5.3 V; K = (IGAINMOD – IOFFSET) x IAC x (VEAO – 1.5) $-^1$.

Functional Description

Switching losses of wide input voltage range PFC boost converters increase dramatically as power levels increase above 200 watts. The use of zero-voltage switching (ZVS) techniques improves the efficiency of high power PFCs by significantly reducing the turn-on losses of the boost MOSFET. ZVS is accomplished by using a second, smaller MOSFET, together with a storage element (inductor) to convert the turn-on losses of the boost MOSFET into useful output power.

The basic function of the FAN4822 is to provide a power factor corrected, regulated DC bus voltage using continuous, average current-mode control. Like Micro Linear's family of PFC/PWM controllers, the FAN4822 employs leading-edge pulse width modulation to reduce system noise and permit frequency synchronization to a trailing edge PWM stage for the highest possible DC bus voltage bandwidth. For minimization of switching losses, circuitry has been incorporated to control the switching of the ZVS FET.

Theory of Operation

Figure 1 shows a simplified schematic of the output and control sections of a high power PFC circuit. Figure 2 shows the relationship of various waveforms in the circuit. Q1 functions as the main switching FET and Q2 provides the ZVS action. During each cycle, Q2 turns on before Q1, diverting the current in L1 away from D1 into L2. The current in L2 increases linearly until at t2 it equals the current through L1. When these currents are equal, L1 ceases discharging current and is now charged through L2 and Q2. At time t2, the drain voltage of Q1 begins to fall. The shape of the voltage waveform is sinusoidal due to the interaction of L2 and the combined parasitic capacitance of D1 and Q1 (or optional ZVS capacitor C_{ZVS}). At t3, the voltage across Q1 is sufficiently low that the controller turns Q2 off and Q1 on. Q1 then behaves as an ordinary PFC switch, storing energy in the boost inductor L1. The energy stored in L2 is completely discharged into the boost capacitor via D2 during the Q1 off-time and the value of L2 must be selected for discontinuous-mode operation.

Component Selection

Q1 Turn-Off

Because the FAN4822 uses leading edge modulation, the PFC MOSFET (Q1) is always turned off at the end of each oscillator ramp cycle. For proper operation, the internal ZVS flip-flop must be reset every cycle during the oscillator discharge time. This is done by automatically resetting the ZVS comparator a short time after the drain voltage of the main Q has reached zero (refer to Figure 1 sense circuit). This sense circuit terminates the ZVS on time by sensing the main Q drain voltage reaching zero. It is then reset by way of a resistor pull-up to V_{CC} (R6). The advantage of this circuit is that the ZVS comparator is not reset at the main Q turn off which occurs at the end of the clock cycle. This avoids the potential for improper reset of the internal ZVS flip-flop.

Another concern is the proper operation of the ZVS comparator during discontinuous mode operation (DCM), which will occur at the cusps of the rectified AC waveform and at light loads. Due to the nature of the voltage seen at the drain of the main boost Q during DCM operation, the ZVS comparator can be fooled into forcing the ZVS Q on for the entire period. By adding a circuit which limits the maximum on time of the ZVS Q, this problem can be avoided. Q3 in Figure 1 provides this function.



Figure 1. Simplified PFC/ZVS Schematic.

PRODUCT SPECIFICATION

Q1 Turn-On

The turn-on event consists of the time it takes for the current through L2 to ramp to the L1 current plus the resonant event of L2 and the ZVS capacitor. The total event should occur in a minimum of 350–450ns, but can be longer at the risk of increasing the total harmonic distortion. Setting these times equal should minimize conducted and radiated emissions.

$$t_{Q1(OFF)} = t_{IL2} + t_{RES} = 400ns$$
 (1)

Where I_{L2} is equal to I_{L1} .

The value of L2 is calculated to remain in discontinuousmode:

$$L2 = \frac{V_{BUS} \times V_{RMS(MIN)} \times t_{IL2}}{\sqrt{2} \times P_{OUT}}$$
(2)

The resonant event occurs in 1/4 of a full sinusoidal cycle. For example, when a 1/4 cycle occurs in 200ns, the frequency is 1.25MHz.

$$f_{RES} = \frac{1}{2\pi \sqrt{L2 \times C_{ZVS}}} = \frac{1}{4 \times t_{RES}}$$
(3)

Rearranging and solving for L2:

$$L2 = \frac{4 \times t_{RES^2}}{\pi^2 \times C_{ZVS}}$$
(4)

The resonant capacitor (C_{ZVS}) value is found by setting equations 2 and 4 equal to each other and solving for C_{ZVS} .

$$C_{ZVS} = \frac{4 \times t_{RES^2} \times \sqrt{2} \times P_{OUT}}{\pi^2 \times V_{BUS} \times V_{RMS(MIN)} \times t_{IL2}}$$
(5)

Application

Figure 3 displays a typical application circuit for a 500W ZVS PFC supply. Full design details are covered in application note 33, FAN4822 Power Factor Correction With Zero Voltage Resonant Switching.



Figure 2. Timing Diagrams

FAN4822



Figure 3. FAN4822 Schematic.



Ordering Information

Part Number	PFC/PWM Frequency	Package
FAN4822IN	-40°C to 85°C	14-Pin PDIP (P14)
FAN4822IM	-40°C to 85°C	16-Pin Wide SOIC (S16W)

DISCLAIMER

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LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.