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FAN4822

ZVS Average Current PFC Controller

Features

- Average current sensing, continuous boost, leading edge PFC for low total harmonic distortion and near unity power factor
- Built-in ZVS switch control with fast response for high efficiency at high power levels
- Average line voltage compensation with brownout control
- Current fed gain modulator improves noise immunity and provides universal input operation
- Overvoltage comparator eliminates output “runaway” due to load removal
- UVLO, current limit, and soft-start
- Precision 1.3% reference

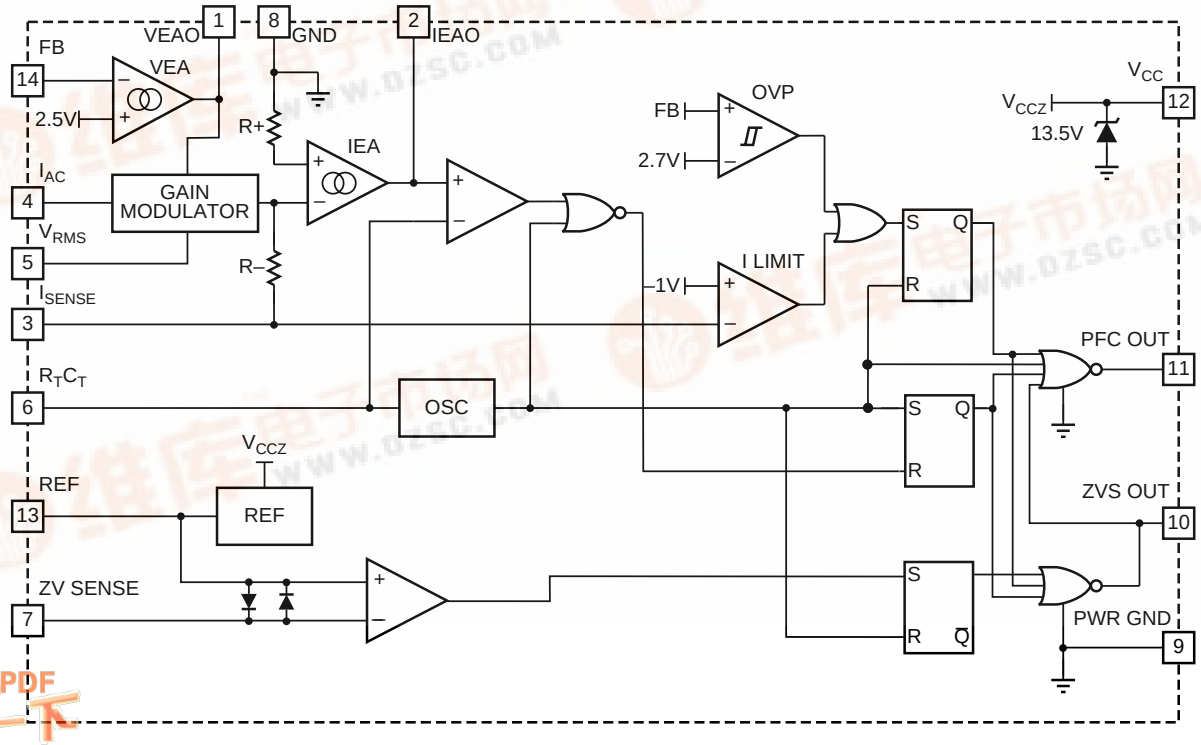
General Description

The FAN4822 is a PFC controller designed specifically for high power applications. The controller contains all of the functions necessary to implement an average current boost PFC converter, along with a Zero Voltage Switch (ZVS) controller to reduce diode recovery and MOSFET turn-on losses.

The average current boost PFC circuit provides high power factor (>98%) and low Total Harmonic Distortion (THD). Built-in safety features include undervoltage lockout, overvoltage protection, peak current limiting, and input voltage brownout protection.

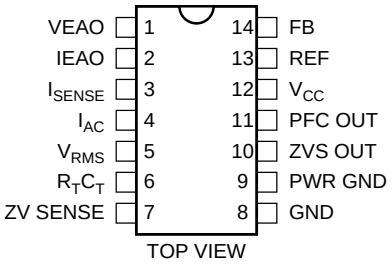
The ZVS control section drives an external ZVS MOSFET which, combined with a diode and inductor, soft switches the boost regulator. This technique reduces diode reverse recovery and MOSFET switching losses to reduce EMI and maximize efficiency.

Block Diagram



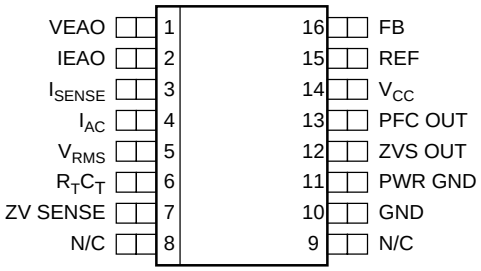
Pin Configuration

FAN4822
14-Pin DIP (P14)



TOP VIEW

FAN4822
16-Pin SOIC (S16W)



TOP VIEW

Pin Description (Pin numbers is parentheses are for 16-pin package)

Pin	Name	Function
1 (1)	VEAO	Transconductance voltage error amplifier output.
2 (2)	IEAO	Transconductance current error amplifier output.
3 (3)	I_{SENSE}	Current sense input to the PFC current limit comparator.
4 (4)	I_{AC}	PFC gain modulator reference input.
5 (5)	V_{RMS}	Input for RMS line voltage compensation.
6 (6)	R_TC_T	Connection for oscillator frequency setting components.
7 (7)	ZV SENSE	Input to the high speed zero voltage crossing comparator.
8 (10)	GND	Analog signal ground.
9 (11)	PWR GND	Return for the PFC and ZVS driver outputs.
10 (12)	ZVS OUT	ZVS MOSFET driver output.
11 (13)	PFC OUT	PFC MOSFET driver output.
12 (14)	V_{CC}	Shunt-regulated supply voltage.
13 (15)	REF	Buffered output for the internal 7.5V reference.
14 (16)	FB	Transconductance voltage error amplifier input.

Absolute Maximum Ratings

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Parameter	Min	Max	Unit
Shunt Regulator Current (I_{CC})		55	mA
Peak Driver Output Current		±500	mA
Analog Inputs	–0.3	7	V
Junction Temperature		150	°C
Storage Temperature Range	–65	150	°C
Lead Temperature (Soldering, 10 sec)		150	°C
Thermal Resistance (θ_{JA}) Plastic DIP Plastic SOIC		 80 110	 °C/W °C/W

Operating Conditions

Temperature Range	Min.	Max.	Units
FAN4822IX	–40	85	°C

Electrical Characteristics

Unless otherwise specified, R_T = 52.3kΩ, C_T = 470pF, T_A = Operating Temperature Range (Note 1)

Parameter	Conditions	Min.	Typ.	Max.	Units
Voltage Error Amplifier					
Input Voltage Range		0		7	V
Transconductance	$V_{NON-INV} = V_{INV}$, VEAO = 3.75V	50	70	120	µ℧
Feedback Reference Voltage	$V_{EAO} = V_{FB}$	2.4	2.5	2.6	V
Open Loop Gain		60	75		dB
PSRR	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V	60	75		dB
Output Low			0.65	1	V
Output High		6.0	6.7		V
Source Current	ΔV_{IN} = ±0.5V, V_{OUT} = 6V	–40	–80		µA
Sink Current	ΔV_{IN} = ±0.5V, V_{OUT} = 1.5V	40	80		mA
Current Error Amplifier					
Input Voltage Range		–1.5		2	V
Transconductance	$V_{NON-INV} = V_{INV}$, IEAO = 3.75V	130	195	310	µ℧
Input Offset Voltage			±3	±15	mV
Open Loop Gain		60	75		dB
PSRR	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V	60	75		dB
Output Low			0.65	1	V
Output High		6.0	6.7		V
Source Current	ΔV_{IN} = ±0.5V, V_{OUT} = 6V	–30	–80		µA
Sink Current	ΔV_{IN} = ±0.5V, V_{OUT} = 1.5V	40	80		µA
OVP Comparator					
Threshold Voltage		2.6	2.7	2.8	V
Hysteresis		80	120	150	mV
I_{SENSE} Comparator					
Threshold Voltage		–0.8	–1.0	–1.15	V
Delay to Output			150	300	ns
ZV Sense Comparator					
Propagation Delay	100mV Overdrive			50	ns
Threshold Voltage		7.35	7.5	7.65	V
Input Capacitance			6		pF

Electrical Characteristics (Continued)

Unless otherwise specified, R_T = 52.3kΩ, C_T = 470pF, T_A = Operating Temperature Range (Note 1)

Parameter	Conditions	Min.	Typ.	Max.	Units
Gain Modulator					
Gain (Note 2)	I_{IAC} = 100mA, V_{VRMS} = 0V, V_{FB} = 0V	0.36	0.51	0.66	
	I_{IAC} = 50mA, V_{VRMS} = 1.2V, V_{FB} = 0V	1.20	1.72	2.24	
	I_{IAC} = 100µA, V_{VRMS} = 1.8V, V_{FB} = 0V	0.55	0.78	1.01	
	I_{IAC} = 100µA, V_{VRMS} = 3.3V, V_{FB} = 0V	0.14	0.20	0.26	
Bandwidth	I_{IAC} = 250µA		10		MHz
Output Voltage	V_{FB} = 0V, V_{VRMS} = 1.15V, I_{IAC} = 250µA	0.72	0.8	0.9	V
Oscillator					
Initial Accuracy	T_A = 25°C	74	80	87	kHz
Voltage Stability	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		1		%
Temperature Stability			2		%
Total Variation	Line, temperature	72		89	kHz
Ramp Valley to Peak Voltage			2.5		V
Dead Time		100	300	450	ns
C_T Discharge Current		4.5	7.5	9.5	mA
Reference					
Output Voltage	T_A = 25°C, I_{REF} = 1mA	7.4	7.5	7.6	V
Line Regulation	V_{CCZ} – 3V < V_{CC} < V_{CCZ} – 0.5V		2	10	mV
Load Regulation	1mA < I_{REF}, < 20mA		2	15	mV
Temperature Stability			0.4		%
Total Variation	Line, load, and temperature	7.35		7.65	V
Long Term Stability	T_j = 125°C, 1000 hours		5	25	mV
Short Circuit Current	V_{CC} < V_{CCZ} – 0.5V, V_{REF} = 0V	–15	–40	–100	mA
PFC Comparator					
Minimum Duty Cycle	V_{IEAO} > 6.7V			0	%
Maximum Duty Cycle	V_{IEAO} < 1.2V	90	95		%
MOSFET Driver Outputs					
Output Low Voltage	I_{OUT} = –20mA		0.4	1.0	V
	I_{OUT} = –100mA		1.5	3.5	V
	I_{OUT} = –10mA, V_{CC} = 8V		0.8	1.5	V
Output High Voltage	I_{OUT} = 20mA	9.5	10.3		V
	I_{OUT} = 100mA	9	10.3		V
Output Rise/Fall Time	C_L = 1000pF		40		ns
Undervoltage Lockout					
Threshold Voltage		V_{CCZ} – 0.9	V_{CCZ} – 0.6	V_{CCZ} – 0.2	V
Hysteresis		2.4	2.9	3.45	V

Electrical Characteristics (Continued)

Unless otherwise specified, R_T = 52.3kΩ, C_T = 470pF, T_A = Operating Temperature Range (Note 1)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply					
Shunt Voltage (V_{CCZ})	I_{CC} =25mA	12.8	13.5	14.2	V
Load Regulation	25mA < I_{CC} < 55mA		±150	±300	mV
Total Variation	Load and temperature	12.4		14.6	V
Start-up Current	V_{CC} < 12.3V		0.7	1.1	mA
Operating Current	V_{CC} = V_{CCZ} – 0.5V		22	28	mA

Notes

1. Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.
2. Gain = K x 5.3 V; K = ($I_{GAINMOD}$ – I_{OFFSET}) x I_{AC} x (V_{EAO} – 1.5)$^{-1}$.

Functional Description

Switching losses of wide input voltage range PFC boost converters increase dramatically as power levels increase above 200 watts. The use of zero-voltage switching (ZVS) techniques improves the efficiency of high power PFCs by significantly reducing the turn-on losses of the boost MOSFET. ZVS is accomplished by using a second, smaller MOSFET, together with a storage element (inductor) to convert the turn-on losses of the boost MOSFET into useful output power.

The basic function of the FAN4822 is to provide a power factor corrected, regulated DC bus voltage using continuous, average current-mode control. Like Micro Linear's family of PFC/PWM controllers, the FAN4822 employs leading-edge pulse width modulation to reduce system noise and permit frequency synchronization to a trailing edge PWM stage for the highest possible DC bus voltage bandwidth. For minimization of switching losses, circuitry has been incorporated to control the switching of the ZVS FET.

Theory of Operation

Figure 1 shows a simplified schematic of the output and control sections of a high power PFC circuit. Figure 2 shows the relationship of various waveforms in the circuit. Q1 functions as the main switching FET and Q2 provides the ZVS action. During each cycle, Q2 turns on before Q1, diverting the current in L1 away from D1 into L2. The current in L2 increases linearly until at t_2 it equals the current through L1. When these currents are equal, L1 ceases discharging current and is now charged through L2 and Q2. At time t_2, the drain voltage of Q1 begins to fall. The shape of the voltage waveform is sinusoidal due to the interaction of L2 and the combined parasitic capacitance of D1 and Q1 (or optional ZVS capacitor C_{ZVS}). At t_3, the voltage across Q1 is sufficiently low that the controller turns Q2 off and Q1 on. Q1 then behaves as an ordinary PFC switch, storing energy in the boost inductor L1. The energy stored in L2 is completely discharged into the boost capacitor via D2 during the Q1 off-time and the value of L2 must be selected for discontinuous-mode operation.

Component Selection

Q1 Turn-Off

Because the FAN4822 uses leading edge modulation, the PFC MOSFET (Q1) is always turned off at the end of each oscillator ramp cycle. For proper operation, the internal ZVS flip-flop must be reset every cycle during the oscillator discharge time. This is done by automatically resetting the ZVS comparator a short time after the drain voltage of the main Q has reached zero (refer to Figure 1 sense circuit). This sense circuit terminates the ZVS on time by sensing the main Q drain voltage reaching zero. It is then reset by way of a resistor pull-up to V_{CC} (R6). The advantage of this circuit is that the ZVS comparator is not reset at the main Q turn off which occurs at the end of the clock cycle. This avoids the potential for improper reset of the internal ZVS flip-flop.

Another concern is the proper operation of the ZVS comparator during discontinuous mode operation (DCM), which will occur at the cusps of the rectified AC waveform and at light loads. Due to the nature of the voltage seen at the drain of the main boost Q during DCM operation, the ZVS comparator can be fooled into forcing the ZVS Q on for the entire period. By adding a circuit which limits the maximum on time of the ZVS Q, this problem can be avoided. Q3 in Figure 1 provides this function.

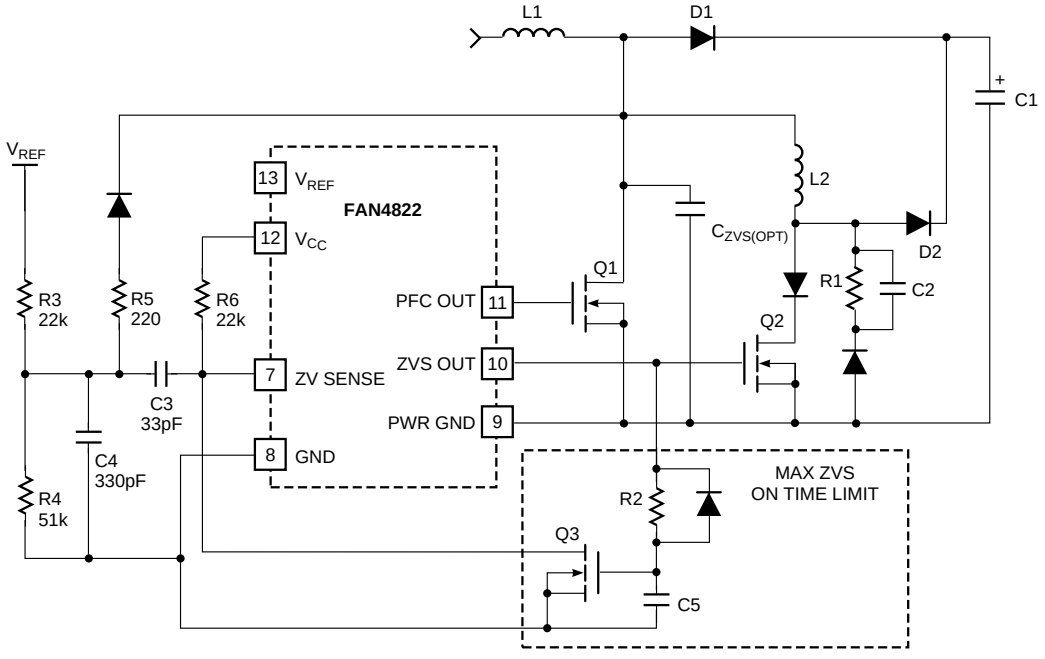


Figure 1. Simplified PFC/ZVS Schematic.

Q1 Turn-On

The turn-on event consists of the time it takes for the current through L2 to ramp to the L1 current plus the resonant event of L2 and the ZVS capacitor. The total event should occur in a minimum of 350–450ns, but can be longer at the risk of increasing the total harmonic distortion. Setting these times equal should minimize conducted and radiated emissions.

$$t_{Q1(OFF)} = t_{IL2} + t_{RES} = 400ns \quad (1)$$

Where I_{L2} is equal to I_{L1}.

The value of L2 is calculated to remain in discontinuous-mode:

$$L2 = \frac{V_{BUS} \times V_{RMS(MIN)} \times t_{IL2}}{\sqrt{2} \times P_{OUT}} \quad (2)$$

The resonant event occurs in 1/4 of a full sinusoidal cycle. For example, when a 1/4 cycle occurs in 200ns, the frequency is 1.25MHz.

$$f_{RES} = \frac{1}{2\pi\sqrt{L2 \times C_{ZVS}}} = \frac{1}{4 \times t_{RES}} \quad (3)$$

Rearranging and solving for L2:

$$L2 = \frac{4 \times t_{RES^2}}{\pi^2 \times C_{ZVS}} \quad (4)$$

The resonant capacitor (C_{ZVS}) value is found by setting equations 2 and 4 equal to each other and solving for C_{ZVS}.

$$C_{ZVS} = \frac{4 \times t_{RES^2} \times \sqrt{2 \times P_{OUT}}}{\pi^2 \times V_{BUS} \times V_{RMS(MIN)} \times t_{IL2}} \quad (5)$$

Application

Figure 3 displays a typical application circuit for a 500W ZVS PFC supply. Full design details are covered in application note 33, FAN4822 Power Factor Correction With Zero Voltage Resonant Switching.

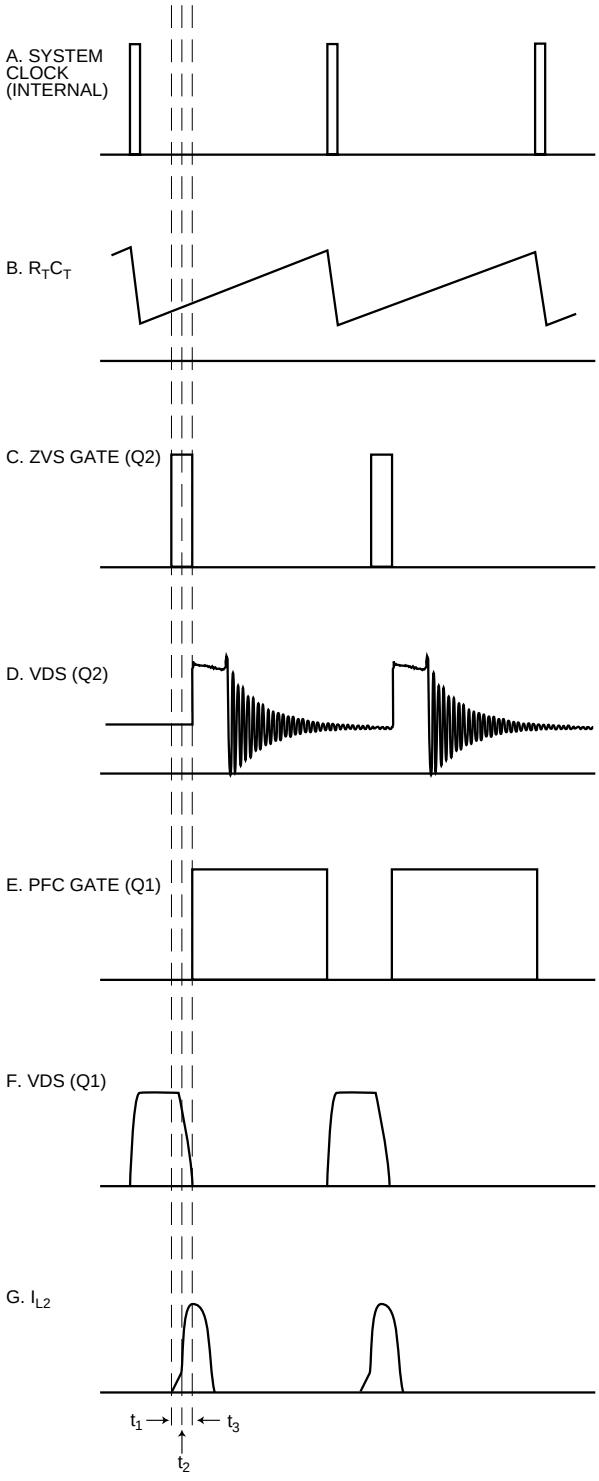


Figure 2. Timing Diagrams

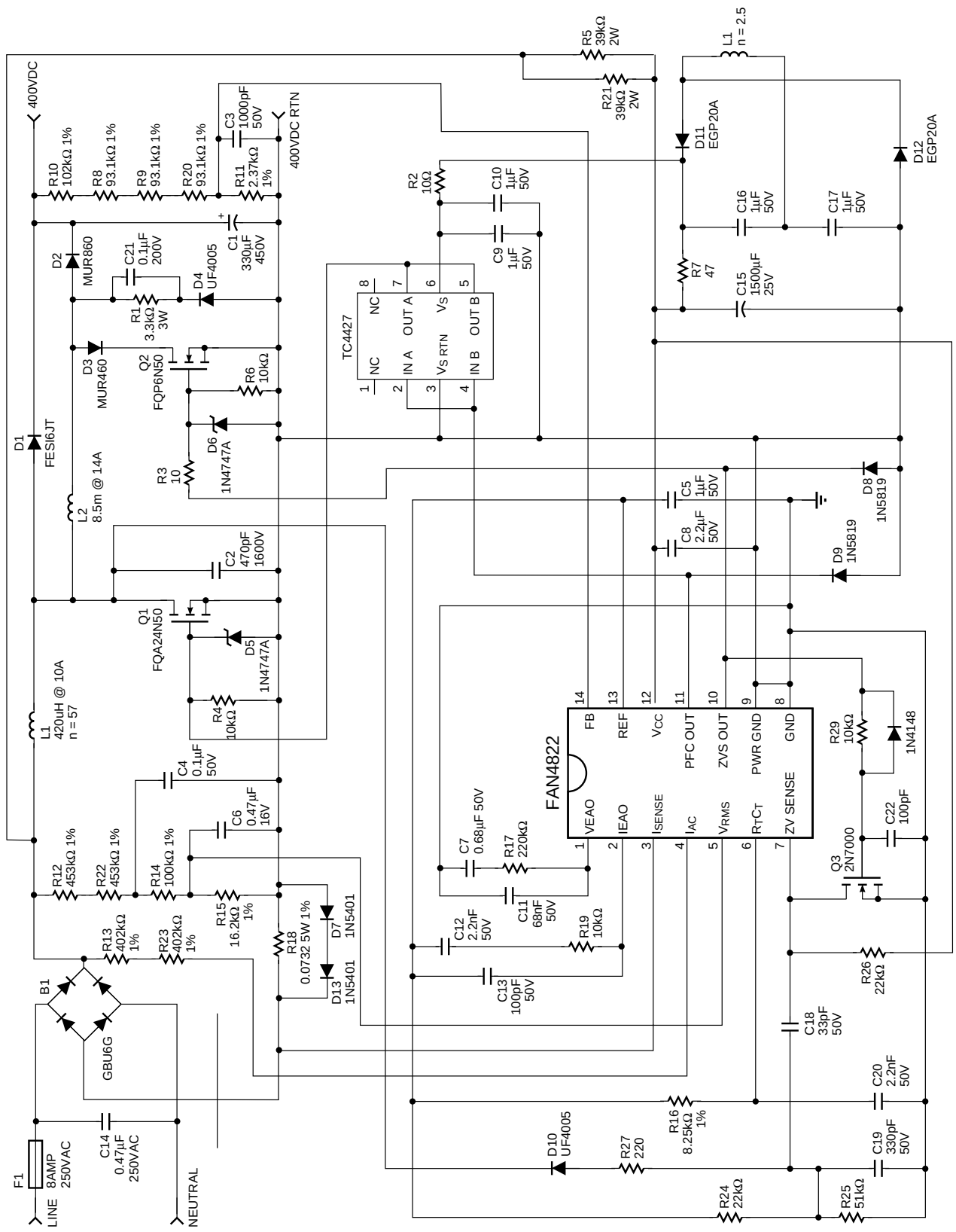
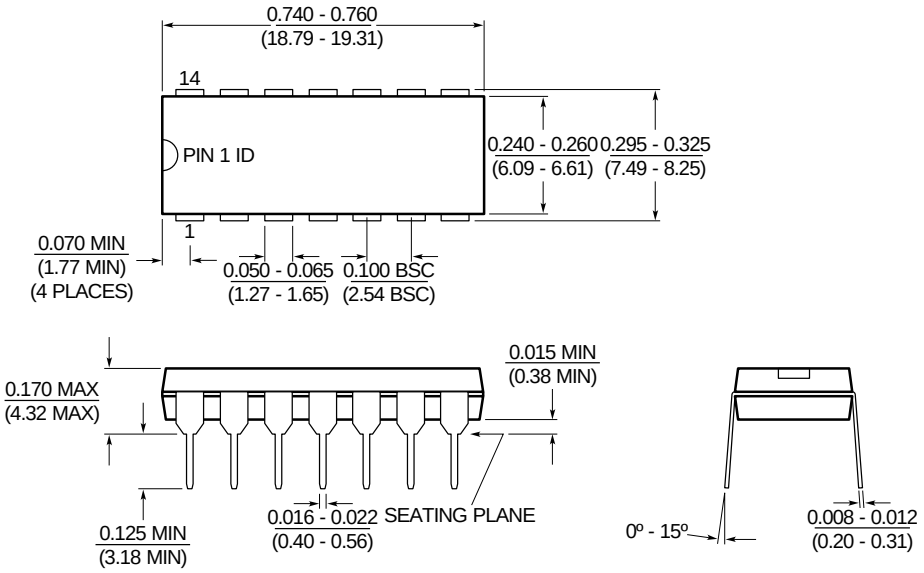


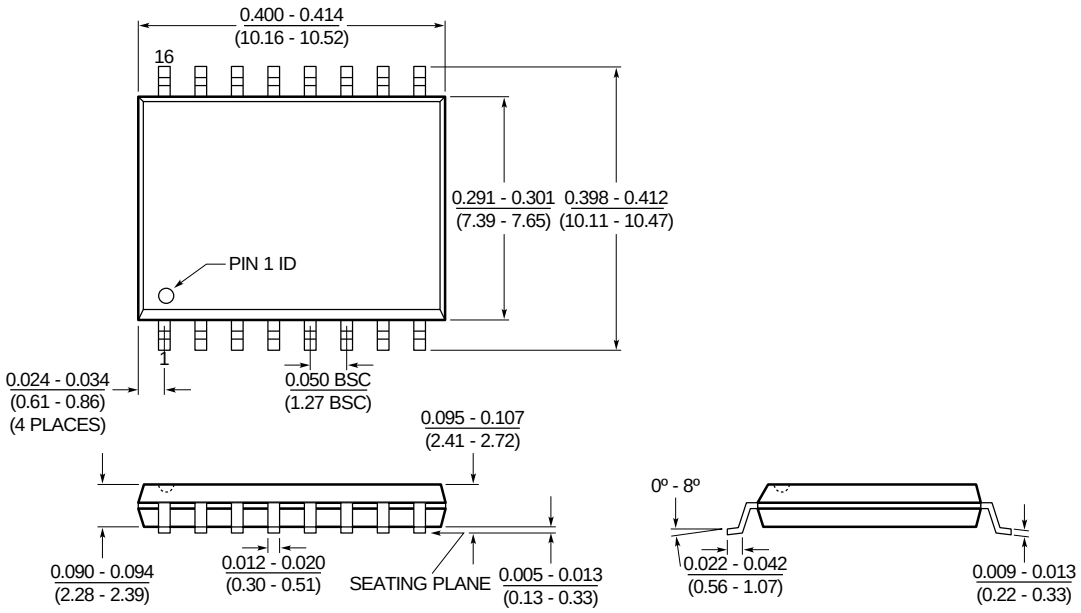
Figure 3. FAN4822 Schematic.

Mechanical Dimensions inches (millimeters)

Package: P14
14-Pin PDIP



Package: S16W
16-Pin Wide SOIC



Ordering Information

Part Number	PFC/PWM Frequency	Package
FAN4822IN	-40°C to 85°C	14-Pin PDIP (P14)
FAN4822IM	-40°C to 85°C	16-Pin Wide SOIC (S16W)