

FAN5070

High Performance Programmable Synchronous DC-DC Controller

Features

- Output programmable in 25mV steps from 1.05V to 1.825V using a dynamically programmable integrated 5-bit DAC
- Remote sense
- Programmable Active Droop™ up to 200mV
- Drives N-Channel MOSFETs
- Overcurrent protection using MOSFET sensing
- Overvoltage protection including startup
- 85% efficiency typical at full load
- Integrated Power Good and Enable/Soft Start functions
- Meets Intel VRM8.5 specifications using minimum number of external components
- 20 pin SOIC package

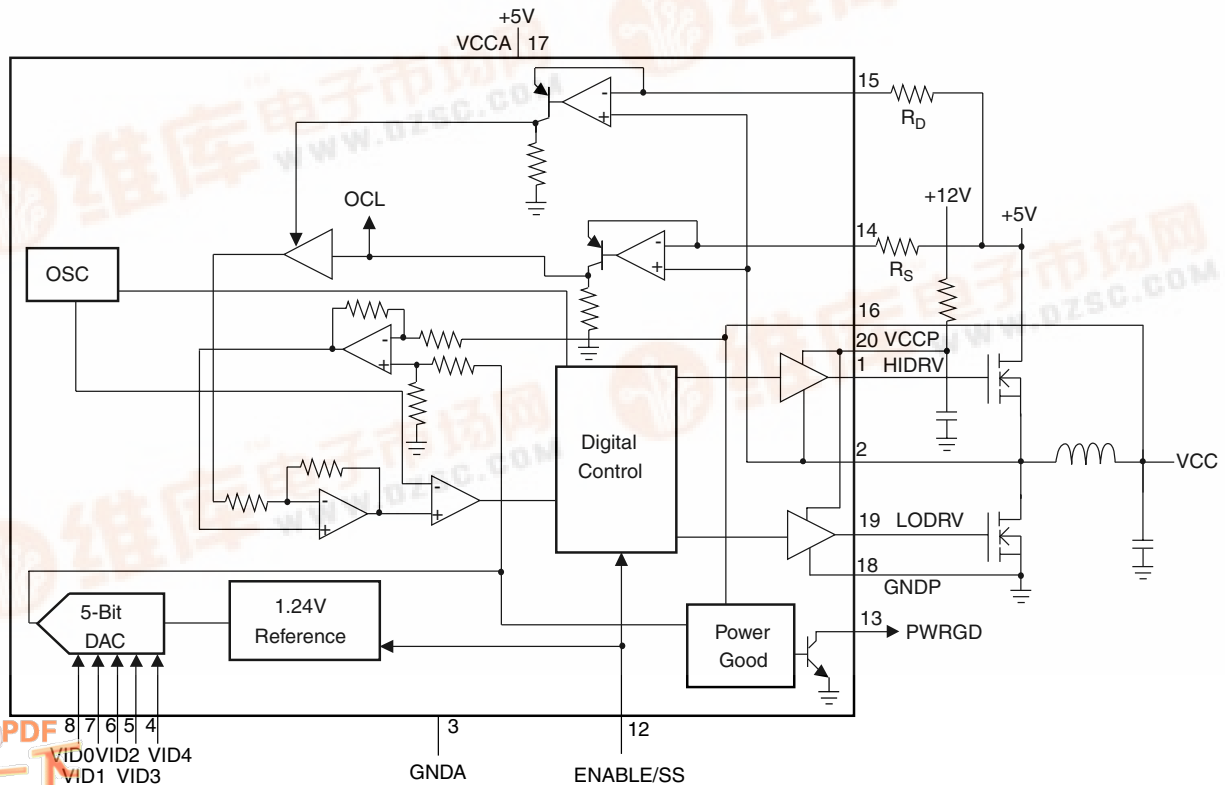
Applications

- Power supply for Pentium® III Platforms
- VRM for Pentium III processor
- Programmable power supply

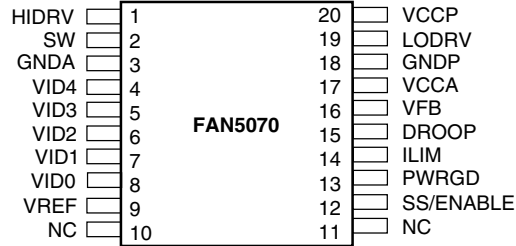
Description

The FAN5070 is a synchronous mode DC-DC controller IC which provides a highly accurate, programmable output voltage for platforms such as the Intel Pentium III, and provides a complete solution for all Intel VRM8.5 CPU applications, and for other high-performance processors. The FAN5070 features remote voltage sensing, independently adjustable current limit, and a proprietary wide-range Programmable Active Droop™ for optimal converter transient response and VRM8.5 compliance. The FAN5070 uses a 5-bit D/A converter to dynamically program the output voltage during operation from 1.05V to 1.825V in 25mV steps. The FAN5070 uses a high level of integration to deliver load currents in excess of 28A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range. An on-board precision low TC reference achieves 0.8% voltage regulation without expensive external components. The FAN5070 also offers integrated functions including open-collector Power Good, Output Enable/Soft Start and current limiting, and is available in a 20 pin SOIC package.

Block Diagram



Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	HIDRV	High Side FET Driver. Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be <0.5".
2	SW	High Side Driver Source and Low Side Driver Drain Switching Node. Together with DROOP and ILIM pins allows FET sensing for V_{CC} current.
3	GNDA	Analog Ground. Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
4-8	VID4-0	Voltage Identification Code Inputs. These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1.
9	VREF	DAC Output for Test Only. Do not load externally.
10, 11	NC	NC. No Connect.
12	ENABLE/SS	Output Enable. A logic LOW on this pin will disable all outputs. An internal current source allows for open collector control. This pin also doubles as soft start for all outputs.
13	PWRGD	Power Good Flag. An open collector output that will be logic LOW if any output voltage is not within $\pm 14\%$ of the nominal output voltage setpoint.
14	ILIM	V_{CC} Current Feedback. Pin 11 is used in conjunction with pin 2 as the input for the V_{CC} current feedback control loop. Layout of these traces is critical to system performance. See Application Information for details.
15	DROOP	Drop Set. Use this pin to set magnitude of active droop.
16	VFB	V_{CC} Voltage Feedback. Pin 13 is used as the input for the V_{CC} voltage feedback control loop. See Application Information for details regarding correct layout.
17	VCCA	Analog V_{CC}. Connect to system 5V supply and decouple with a 0.1 μ F ceramic capacitor.
18	GNDA	Power Ground. Return pin for high currents flowing in pin 17 (V_{CCP}).
19	LODRV	V_{CC} Low Side FET Driver. Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be <0.5".
20	VCCP	Power V_{CC}. For all FET drivers. Connect to system 12V supply through a 33 Ω , and decouple with a 1 μ F ceramic capacitor.

Absolute Maximum Ratings

Supply Voltage V_{CCP} to GND	15V
Supply Voltage V_{CCA} to GND	13.5V
Voltage Identification Code Inputs, VID0-VID4	VCCA
All Other Pins	13.5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C
Thermal Resistance Junction-to-case, Θ_{JA}	75°C/W

Note 1: Component mounted on demo board in free air.

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage V_{CCA}		4.50	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temperature		0		70	°C
Output Driver Supply, V_{CCP}		10.8	12	13.2	V

Electrical Specifications

($V_{CCA} = 5V$, $V_{CCP} = 12V$, $V_{OUT} = 1.425V$, and $T_A = +25^\circ C$ using circuits in Figure 1, unless otherwise noted.)

The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions	Min.	Typ.	Max.	Units	
Output Voltage	See Table I	• 1.05		1.825	V	
Output Current			28		A	
Initial Voltage Setpoint	$I_{LOAD} = 0.8A$, $V_{VID} = 1.425V$	1.453	1.465	1.477	V	
Output Temperature Drift	$T_A = 0$ to $70^\circ C$, $V_{VID} = 1.425V$	•	-6		mV	
Line Regulation	$V_{IN} = 4.75V$ to $5.25V$	•	+10		mV/V	
Internal Droop Impedance ³	$I_{LOAD} = 0.8A$ to $30A$		13.0	14.4	15.8	K Ω
Maximum Programmable Droop		• 200			mV	
Output Ripple	20MHz BW, $I_{LOAD} = 28A$		20		mVpk	
Total Output Variation, Steady State ¹	$V_{VID} = 1.425V^3$	• 1.360		1.490	V	
Total Output Variation, Transient ²	$I_{LOAD} = 0.8A$ to I_{max} , $V_{VID} = 1.425V$	• 1.335		1.515	V	
Short Circuit Detect Current		• 45	50	60	μA	
Efficiency	$I_{LOAD} = 18A$, $V_{VID} = 1.425V$		83		%	
Output Driver Rise & Fall Time	See Figure 3		50		nsec	
Output Driver Deadtime	See Figure 3		50		nsec	
Duty Cycle			0	100	%	
5V UVLO		• 3.76	4	4.24	V	
12V UVLO		• 7.65	8.5	9.35	V	
Oscillator Frequency		• 255	300	345	kHz	
PWRGD Threshold ⁴ Switcher	Logic HIGH [$V_{VID} + 85mV$] Logic LOW [$V_{VID} - 155mV$]	• 88 • 80		112 120	%	
PWRGD Delay Switcher	HIGH \rightarrow LOW		6		μsec	
PWRGD Hysteresis Switcher			25		mV	

Notes:

1. Steady State Voltage Regulation includes Initial Voltage Setpoint, Droop, Output Ripple and Output Temperature Drift and is measured at the converter's VFB sense point.
2. As measured at the converter's VFB sense point. For motherboard applications, the PCB layout should exhibit no more than 0.5mΩ trace resistance between the converter's output capacitors and the CPU. Remote sensing should be used for optimal performance.
3. Using the VFB pin for remote sensing of the converter's output at the load, and the appropriate droop, the converter will be in compliance with Intel's VRM 8.5 specification. If Intel specifications on maximum plane resistance from the converter's output capacitors to the CPU are met, the specifications at the capacitors will also be met.

Table 1. Output Voltage Programming Codes for FAN5070

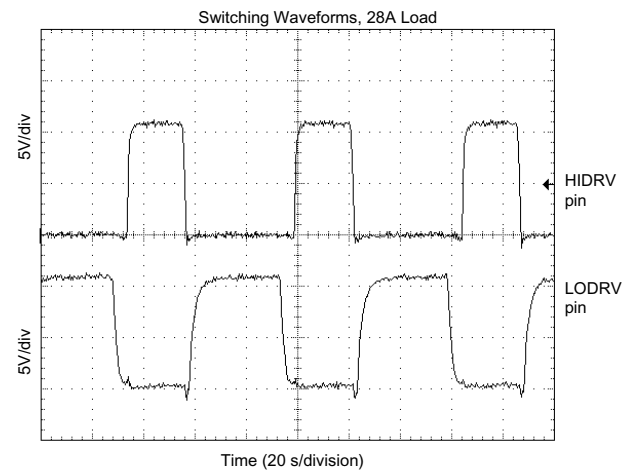
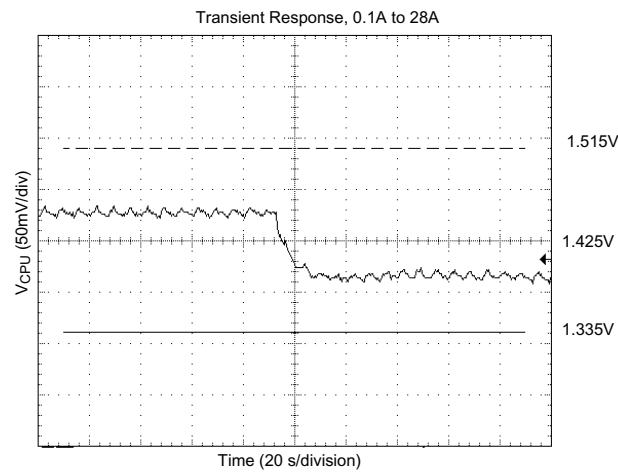
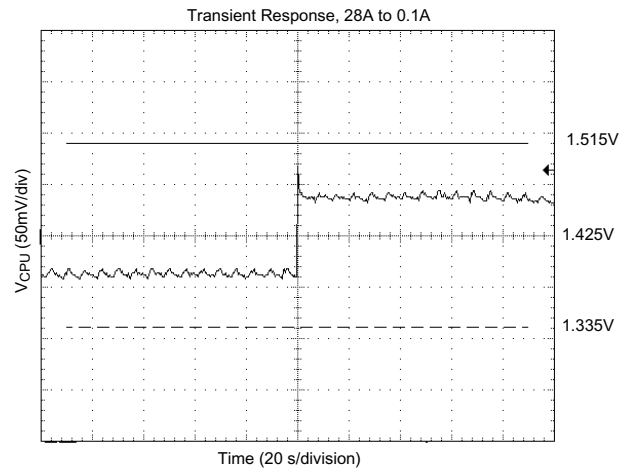
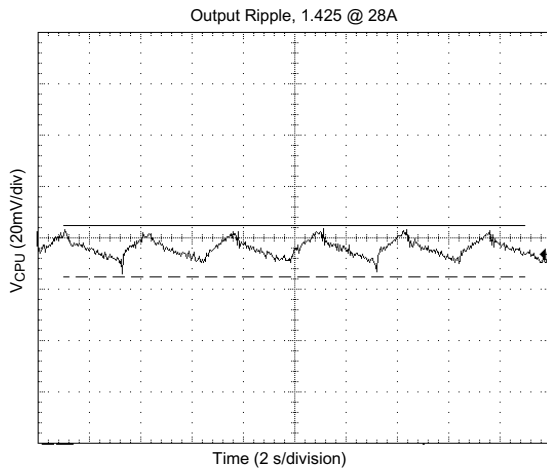
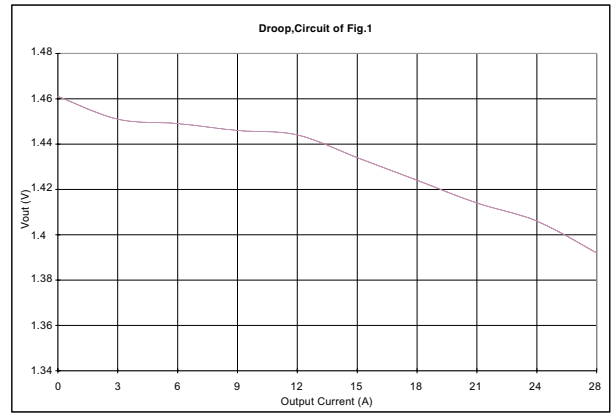
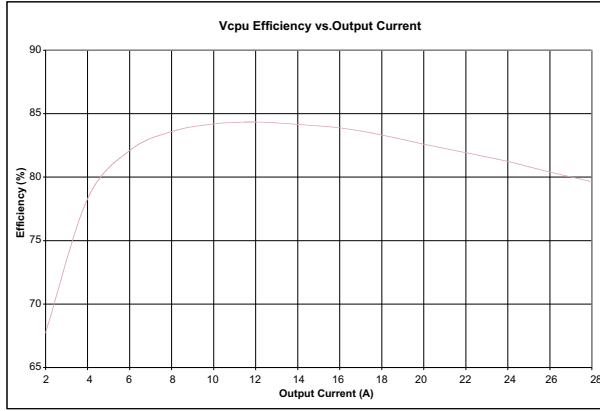
VID25mV	VID3	VID2	VID1	VID0	Nominal V _{OUT}
0	0	1	0	0	1.050V
1	0	1	0	0	1.075V
0	0	0	1	1	1.100V
1	0	0	1	1	1.125V
0	0	0	1	0	1.150V
1	0	0	1	0	1.175V
0	0	0	0	1	1.200V
1	0	0	0	1	1.225V
0	0	0	0	0	1.250V
1	0	0	0	0	1.275V
0	1	1	1	1	1.300V
1	1	1	1	1	1.325V
0	1	1	1	0	1.350V
1	1	1	1	0	1.375V
0	1	1	0	1	1.400V
1	1	1	0	1	1.425V
0	1	1	0	0	1.450V
1	1	1	0	0	1.475V
0	1	0	1	1	1.500V
1	1	0	1	1	1.525V
0	1	0	1	0	1.550V
1	1	0	1	0	1.575V
0	1	0	0	1	1.600V
1	1	0	0	1	1.625V
0	1	0	0	0	1.650V
1	1	0	0	0	1.675V
0	0	1	1	1	1.700V
1	0	1	1	1	1.725V
0	0	1	1	0	1.750V
1	0	1	1	0	1.775V
0	0	1	0	1	1.800V
1	0	1	0	1	1.825V

Note:

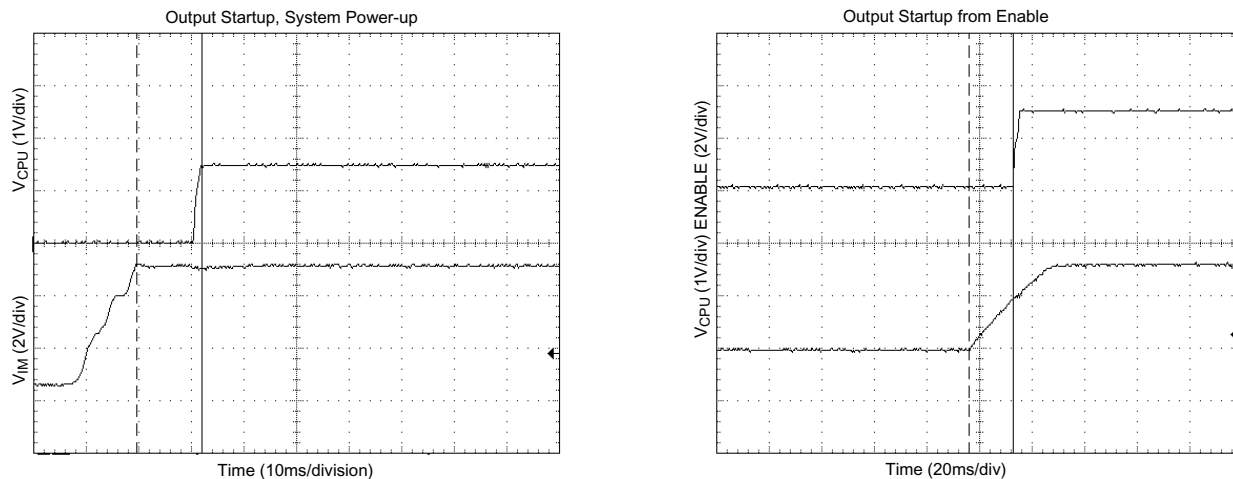
1. 0 = processor pin is tied to GND.
1 = processor pin is pulled up to 3.3V.

Typical Operating Characteristics

($V_{CCA} = 5V$, $V_{CCP} = 12V$, and $T_A = +25^\circ C$ using circuit in Figure 1, unless otherwise noted.)



Typical Operating Characteristics (continued)



Application Circuit

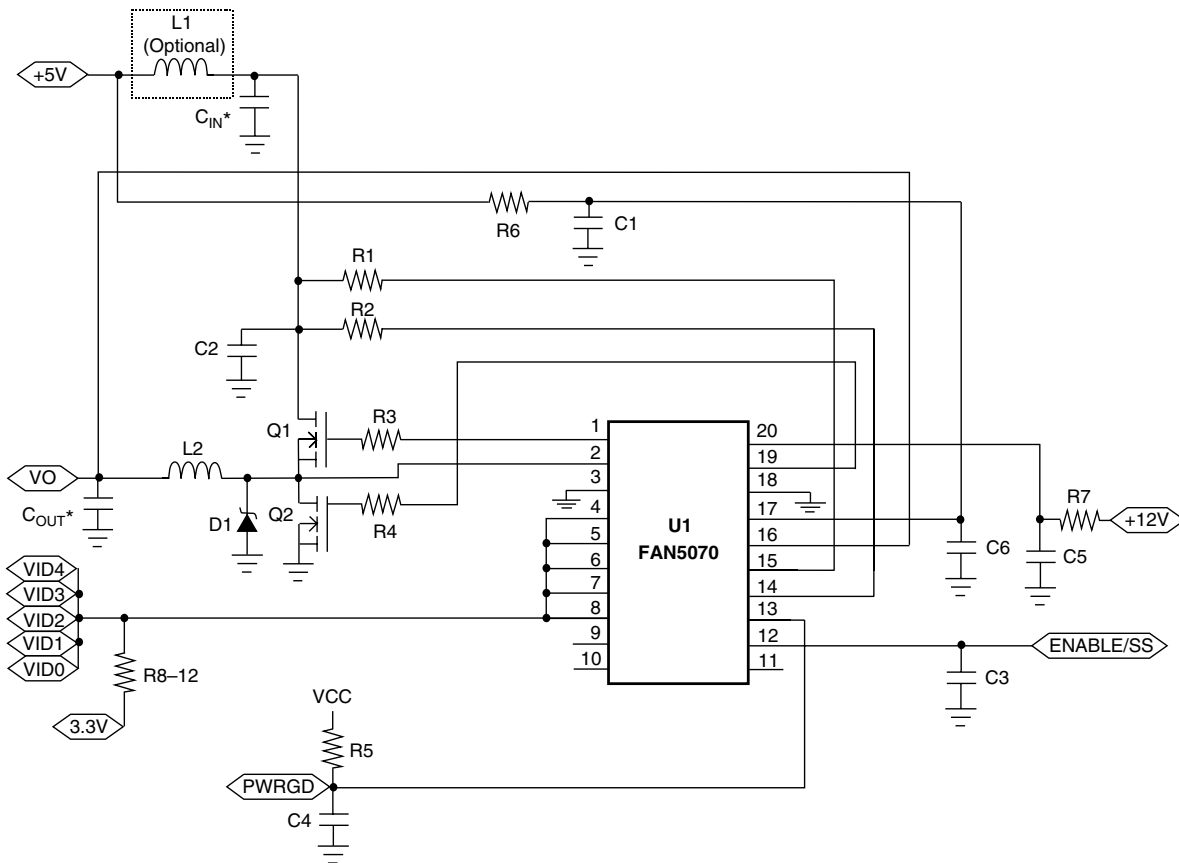


Figure 1. Application Circuit for VRM8.5 Motherboards
(Worst Case Analyzed! See Appendix for Details)

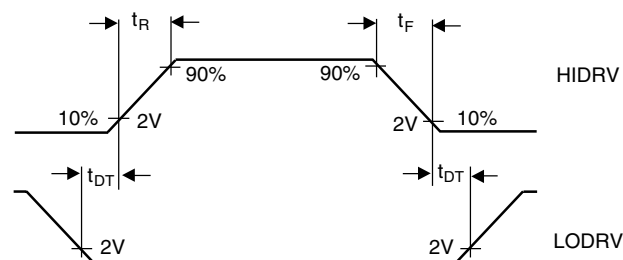
Table 3. FAN5070 Application Bill of Materials for Intel VRM8.5 Motherboards

(Components based on Worst Case Analysis—See Appendix for Details)

Reference	Manufacturer Part #	Quantity	Description	Requirements/Comments
C1	AVX TAJB475M010R5	1	4.7 μ F, 10V Capacitor	
C2, C5	Panasonic ECU-V1C105ZFX	2	1 μ F, 16V Capacitor	
C3-4, C6	Panasonic ECU-V1H104ZFX	3	100nF, 50V Capacitor	
C _{IN}	Rubycon 16ZL1000M	4	1000 μ F, 16V Electrolytic	I _{RMS} = 2.3A
C _{OUT}	Rubycon 6.3ZL1500M	8	1500 μ F, 6.3V Electrolytic	ESR \leq 23m Ω
D1	Motorola MBRD835L	1	8A Schottky Diode	
L1	Any	Optional	1.3 μ H, 10A Inductor	DCR ~ 6m Ω See Note 1.
L2	Coiltronics HC2-1R0	1	1.0 μ H, 34A Inductor	DCR ~ 1m Ω
Q1	Fairchild FDD6690A	2	N-Channel MOSFET	R _{DS(ON)} = 17m Ω @ V _{GS} = 4.5V See Note 2.
Q2	Fairchild FDD6680A	2	N-Channel MOSFET	R _{DS(ON)} = 9.5m Ω @ V _{GS} = 4.5V See Note 2.
R1	Any	1	8.66K Ω	
R2	Any	1	27.4K Ω	
R3-4	Any	2	4.7 Ω	
R5, R8-12	Any	6	10K Ω	
R6-7	Any	2	10 Ω	
U1	Fairchild FAN5070M	1	DC/DC Controller	

Notes:

- Inductor L1 is recommended to isolate the 5V input supply from noise generated by the MOSFET switching, and to comply with Intel di/dt requirements. L1 may be omitted if desired.
- For 30A designs using the TO-220 MOSFETs, heatsinks with thermal resistance $\Theta_{SA} < 20^{\circ}\text{C/W}$ should be used. For designs using the TO-263 MOSFETs, adequate copper area should be used. For details and a spreadsheet on MOSFET selections, refer to Applications Bulletins AB-8 and AB-15.

Test Parameters**Figure 2. Output Drive Timing Diagram**

Application Information

The FAN5070 Controller

The FAN5070 is a programmable synchronous DC-DC controller IC. When designed around the appropriate external components, the FAN5070 can be configured to deliver more than 28A of output current, as appropriate for Intel's VRM8.5, and other processors. The FAN5070 functions as a fixed frequency PWM step down regulator.

Main Control Loop

Refer to the FAN5070 Block Diagram on page 1. The FAN5070 implements "summing mode control," which is different from both classical voltage-mode and current-mode control. It provides superior performance to either by allowing a large converter bandwidth over a wide range of output loads.

The control loop of the regulator contains two main sections: the analog control block and the digital control block. The analog section consists of signal conditioning amplifiers feeding into a comparator which provides the input to the digital control block. The signal conditioning section accepts input from the DROOP (current feedback) and VFB (voltage feedback) pins and sets up two controlling signal paths. The first, the voltage control path, amplifies the difference between the VFB signal and the reference voltage from the DAC and presents the output to one of the summing amplifier inputs. The second, current control path, takes the difference between the DROOP and SW pins when the high-side MOSFET is on, reproducing the voltage across the MOSFET and thus the input current; it presents the resulting signal to another input of the summing amplifier. These two signals are then summed together. This output is then presented to a comparator looking at the oscillator ramp, which provides the main PWM control signal to the digital control block.

The digital control block takes the analog comparator input and the main clock signal from the oscillator to provide the appropriate pulses to the HIDRV and LODRV output pins. These two outputs control the external power MOSFETs.

There is an additional comparator in the analog control section whose function is to set the point at which the FAN5070 current limit comparator disables the output drive signals to the external power MOSFETs.

High Current Output Drivers

The FAN5070 contains two identical high current output drivers that utilize high speed bipolar transistors in a push-pull configuration. The drivers' power and ground are separated from the chip's power and ground for switching noise immunity. The power supply pin, V_{CCP} , is supplied from an external 12V source through a series resistor. The resulting voltage is sufficient to provide the gate to source drive to the external MOSFETs required in order to achieve a low $R_{DS,ON}$.

Internal Voltage Reference

The reference included in the FAN5070 is a precision band-gap voltage reference. Its internal resistors are precisely trimmed to provide a near zero temperature coefficient (TC). Based on the reference is the output from an integrated 5-bit DAC.

In the FAN5070, the DAC monitors the 5 voltage identification pins, VID0-4, and scales the voltage from 1.050V to 1.825V in 25mV steps according to Table I.

Power Good (PWRGD)

The FAN5070 Power Good function is designed in accordance with VRM8.5 and DC-DC converter specifications and provides a continuous voltage monitor on the VFB pin. The circuit compares the VFB signal to the VREF voltage and outputs an active-low interrupt signal to the CPU should be more than +14% from ($V_{VID} + 80mV$), or less than -14% from ($V_{VID} - 120mV$). The Power Good flag provides no other control function to the FAN5070.

Output Enable/Soft Start (ENABLE/SS)

The FAN5070 will accept an open collector/TTL signal for controlling the output voltage. The low state disables the output voltage. When disabled, the PWRGD output is in the low state.

Even if an enable is not required in the circuit, this pin should have attached a capacitor (typically 100nF) to soft-start the switching.

Over-Voltage Protection

The FAN5070 continuously monitors the output voltage for protection against over-voltage conditions. If the voltage at the VFB pin exceeds approximately 2.5V, an OVP circuit forces the low-side MOSFET on, over-riding all other conditions. The OVP circuit remains active, and the low-side MOSFET remains on, until the VFB voltage drops below approximately 2.1V. The OVP circuit is functional even during startup; thus, protection is provided even during startup with a shorted high-side MOSFET.

Oscillator

The FAN5070 oscillator section uses a fixed frequency of operation of 300KHz.

Design Considerations and Component Selection

Additional information on design and component selection may be found in Fairchild's Application Note 57.

MOSFET Selection

This application requires N-channel Logic Level Enhancement Mode Field Effect Transistors. Desired characteristics are as follows:

- Low Static Drain-Source On-Resistance, $R_{DS,ON} < 20m\Omega$ (lower is better)
- Low gate drive voltage, $V_{GS} = 4.5V$ rated
- Power package with low Thermal Resistance
- Drain-Source voltage rating $> 15V$.

The on-resistance ($R_{DS,ON}$) is the primary parameter for MOSFET selection. The on-resistance determines the power dissipation within the MOSFET and therefore significantly affects the efficiency of the DC-DC Converter. For details and a spreadsheet on MOSFET selection, refer to Applications Bulletin AB-8.

Inductor Selection

Choosing the value of the inductor is a trade-off between allowable ripple voltage and required transient response. The system designer can choose any value within the allowed minimum to maximum range in order to either minimize ripple or maximize transient performance. The first order equation (close approximation) for minimum inductance is:

$$L_{min} = \frac{(V_{in} - V_{out})}{f} \times \frac{V_{out}}{V_{in}} \times \frac{ESR}{V_{ripple}}$$

where:

V_{in} = Input Power Supply

V_{out} = Output Voltage

f = DC/DC converter switching frequency

ESR = Equivalent series resistance of all output capacitors in parallel

V_{ripple} = Maximum peak to peak output ripple voltage budget.

The first order equation for maximum allowed inductance is:

$$L_{max} = 2C_o \frac{(V_{in} - V_{out}) D_m V_{tb}}{I_{pp}^2}$$

where:

C_o = The total output capacitance

I_{pp} = Maximum to minimum load transient current

V_{tb} = The output voltage tolerance budget allocated to load transient

D_m = Maximum duty cycle for the DC/DC converter (usually 95%).

Some margin should be maintained away from both L_{min} and L_{max} . Adding margin by increasing L almost always adds expense since all the variables are predetermined by system performance except for C_o , which must be increased to increase L . Adding margin by decreasing L can be done by purchasing capacitors with lower ESR. The FAN5070 provides significant cost savings for the newer CPU systems that typically run at high supply current.

FAN5070 Short Circuit Current Characteristics

The FAN5070 protects against output short circuit on the core supply by latching off both the high-side and low-side MOSFETs. The FAN5070 short circuit current characteristic includes a hysteresis function that prevents the DC-DC converter from oscillating in the event of a short circuit. The short circuit limit is set with the R_S resistor, as given by the formula

$$R_S = \frac{I_{SC} * R_{DS, on}}{I_{Detect}}$$

with $I_{Detect} \approx 50\mu A$, I_{SC} the desired current limit, and $R_{DS, on}$ the high-side MOSFET's on resistance. Remember to make the R_S large enough to include the effects of initial tolerance and temperature variation on the MOSFET's $R_{DS, on}$. Alternatively, use of a sense resistor in series with the source of the MOSFET, as shown in Figure 6, eliminates this source of inaccuracy in the current limit.

As an example, Figure 3 shows the typical characteristic of the DC-DC converter circuit with two FDD6690A high-side MOSFETs ($R_{DS} = 17m\Omega$ maximum at $25^\circ C * 1.25$ at $75^\circ C = 21.25m\Omega$ each for a total of $10.6m\Omega$) and a $6.19K\Omega R_S$.

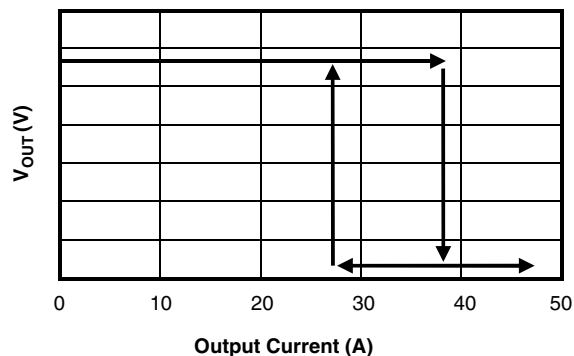


Figure 3. FAN5070 Short Circuit Characteristic

The converter exhibits a normal load regulation characteristic until the voltage across the MOSFET exceeds the internal short circuit threshold of $50\mu A * 6.2K\Omega = 310mV$, which occurs at $310mV/10.6m\Omega = 29A$. [Note that this current limit level can be as high as $310mV/6.5m\Omega = 48A$, if the MOSFET has typical $R_{DS, on}$ rather than maximum, and is at $25^\circ C$. This is the reason for using the external sense resistor.] At this point, the internal comparator trips and signals the

controller to reduce the converter's duty cycle to approximately 20%. This causes a drastic reduction in the output voltage as the load regulation collapses into the short circuit control mode. With a $4\text{m}\Omega$ output short, the voltage is reduced to $29\text{A} * 4\text{m}\Omega = 116\text{mV}$. The output voltage does not return to its nominal value until the output current is reduced to a value within the safe operating range for the DC-DC converter.

Schottky Diode Selection

The application circuits of Figure 1 shows a Schottky diode, D1, which is used as a free-wheeling diode to assure that the body-diode in Q2 does not conduct when the upper MOSFET is turning off and the lower MOSFET is turning on. It is undesirable for this diode to conduct because its high forward voltage drop and long reverse recovery time degrades efficiency, and so the Schottky provides a shunt path for the current. Since this time duration is very short, the selection criterion for the diode is that the forward voltage of the Schottky at the output current should be less than the forward voltage of the MOSFET's body diode.

Output Filter Capacitors

The output bulk capacitors of a converter help determine its output ripple voltage and its transient response. It has already been seen in the section on selecting an inductor that the ESR helps set the minimum inductance, and the capacitance value helps set the maximum inductance. For most converters, however, the number of capacitors required is determined by the transient response and the output ripple voltage, and these are determined by the ESR and not the capacitance value. That is, in order to achieve the necessary ESR to meet the transient and ripple requirements, the capacitance value required is already very large.

The most commonly used choice for output bulk capacitors is aluminum electrolytics, because of their low cost and low ESR. The only type of aluminum capacitor used should be those that have an ESR rated at 100kHz. Consult Application Bulletin AB-14 for detailed information on output capacitor selection.

The output capacitance should also include a number of small value ceramic capacitors placed as close as possible to the processor; $0.1\mu\text{F}$ and $0.01\mu\text{F}$ are recommended values.

Input Filter

The DC-DC converter design may include an input inductor between the system +5V supply and the converter input as shown in Figure 5. This inductor serves to isolate the +5V supply from the noise in the switching portion of the DC-DC converter, and to limit the inrush current into the input capacitors during power up. A value of $2.5\mu\text{H}$ is recommended.

It is necessary to have some low ESR aluminum electrolytic capacitors at the input to the converter. These capacitors

deliver current when the high side MOSFET switches on. Figure 4 shows $3 * 1000\mu\text{F}$, but the exact number required will vary with the speed and type of the processor. Capacitor ripple current rating is a function of temperature, and so the manufacturer should be contacted to find out the ripple current rating at the expected operational temperature. For details on the design of an input filter, refer to Applications Bulletin AB-15.

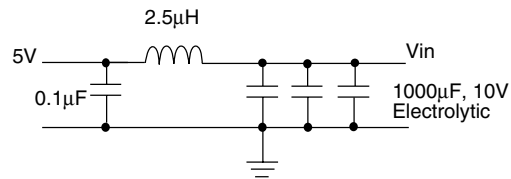


Figure 4. Input Filter

Programmable Active Droop™

The FAN5070 includes Programmable Active Droop™: as the output current increases, the output voltage drops, and the amount of this drop is user adjustable. This is done in order to allow maximum headroom for transient response of the converter. The current is typically sensed by measuring the voltage across the $R_{DS,on}$ of the high-side MOSFET during its on time, as shown in Figures 1 and 2.

To program the amount of droop, use the formula

$$R_D = \frac{14.4\text{K}\Omega * I_{\text{max}} * R_{\text{sense}}}{V_{\text{Droop}} * 9}$$

where I_{max} is the current at which the droop occurs, and R_{sense} is the resistance of the current sensor, either the source resistor or the high-side MOSFET's on-resistance. For example, to get 120mV of droop with a maximum output current of 30A and a $10\text{m}\Omega$ sense resistor, use $R_D = 14.4\text{K}\Omega * 30\text{A} * 10\text{m}\Omega / (120\text{mV} * 9) = 4\text{K}\Omega$. The value of the product $I_{\text{max}} * R_{\text{sense}}$ must be $\leq 600\text{mV}$ for proper functioning of the droop circuit. If this product is exceeded, a lower resistance MOSFET must be used. Further details on use of the Programmable Active Droop™ may be found in Applications Bulletin AB-24.

Remote Sense

The FAN5070 offers remote sense of the output voltage to minimize the output capacitor requirements of the converter. It is highly recommended that the remote sense pin, Pin 20, be tied directly to the processor power pins, so that the effects of power plane impedance are eliminated. Further details on use of the remote sense feature of the FAN5070 may be found in Applications Bulletin AB-24.

PCB Layout Guidelines

- Placement of the MOSFETs relative to the FAN5070 is critical. Place the MOSFETs such that the trace length of the HIDRV and LODRV pins of the FAN5070 to the FET gates is minimized. A long lead length on these pins will cause high amounts of ringing due to the inductance of the trace and the gate capacitance of the FET. This noise radiates throughout the board, and, because it is switching at such a high voltage and frequency, it is very difficult to suppress.
- In general, all of the noisy switching lines should be kept away from the quiet analog section of the FAN5070. That is, traces that connect to pins 1, 2, 16, and 17 (HIDRV, SW, LODRV and V_{CCP}) should be kept far away from the traces that connect to pins 3, 13 and 14.
- Place the 0.1 μ F decoupling capacitors as close to the FAN5070 pins as possible. Extra lead length on these reduces their ability to suppress noise.
- Each V_{CC} and GND pin should have its own via to the appropriate plane. This helps provide isolation between pins.
- Place the MOSFETs, inductor, and Schottky as close together as possible for the same reasons as in the first bullet above. Place the input bulk capacitors as close to the drains of the high side MOSFETs as possible. In addition, placement of a 0.1 μ F decoupling cap right on the drain of each high side MOSFET helps to suppress some of the high frequency switching noise on the input of the DC-DC converter.
- Place the output bulk capacitors as close to the CPU as possible to optimize their ability to supply instantaneous current to the load in the event of a current transient. Additional space between the output capacitors and the CPU will allow the parasitic resistance of the board traces to degrade the DC-DC converter's performance under severe load transient conditions, causing higher voltage deviation. For more detailed information regarding capacitor placement, refer to Application Bulletin AB-5.
- A PC Board Layout Checklist is available from Fairchild Applications. Ask for Application Bulletin AB-11.

Additional Information

For additional information contact your local Fairchild Semiconductor representative, or visit us at our web site www.fairchildsemi.com.

Appendix

Worst-Case Formulae for the Calculation of C_{in} , C_{out} , R_5 , R_7 and R_{offset} (Circuits similar to Figure 1 only)

The following formulae design the FAN5070 for worst-case operation, including initial tolerance and temperature dependence of all of the IC parameters (initial setpoint, reference tolerance and tempco, internal droop impedance, current sensor gain), the initial tolerance and temperature dependence of the MOSFET, and the ESR of the capacitors. The following information must be provided:

V_{S+} , the value of the positive static voltage limit;

$|V_{S-}|$, the absolute value of the negative static voltage limit;

V_{T+} , the value of the positive transient voltage limit;

$|V_{T-}|$, the absolute value of the negative transient voltage limit;

I_O , the maximum output current;

V_{nom} , the nominal output voltage;

V_{in} , the input voltage (typically 5V);

I_{rms} , the ripple current rating of the input capacitors, per cap (2A for the Sanyo parts shown in this data sheet);

R_D , the resistance of the current sensor (usually the MOSFET);

ΔR_D , the tolerance of the current sensor (usually about 67% for MOSFET sensing, including temperature); and

ESR, the ESR of the output capacitors, per cap (44m Ω for the Sanyo parts shown in this data sheet).

$$C_{in} = \frac{I_O * \sqrt{\frac{V_{nom}}{V_{in}} - \left(\frac{V_{nom}}{V_{in}}\right)^2}}{I_{rms}}$$

$$R_{offset} = \frac{V_{S+} - .014 * V_{nom} - .029}{.029 * V_{nom}} * 1K\Omega$$

$$R_7 = \frac{I_O * R_D * (1 + \Delta R_D)}{45 * 10^{-6}}$$

$$R_5 = \frac{14400 * I_O * R_D * (1 + \Delta R_D) * 1.1}{18 * (V_{S+} + |V_{S-}| - .024 * V_{nom})}$$

Number of capacitors needed for C_{OUT} = the greater of:

$$X = \frac{ESR * I_O}{|V_{T-}| + V_{S+} - .024 * V_{nom}}$$

or

$$Y = \frac{ESR * I_O}{V_{T+} - V_{S+} + \frac{14400 * I_O * R_D}{18 * R_5 * 1.1}}$$

Example: Suppose that the static limits are +89mV/-79mV, transient limits are ± 134 mV, current I is 14.2A, and the nominal voltage is 2.000V, using MOSFET current sensing. We have $V_{S+} = 0.089$, $|V_{S-}| = 0.079$, $V_{T+} = |V_{T-}| = 0.134$, $I_O = 14.2$, $V_{nom} = 2.000$, and $\Delta R_D = 1.67$. We calculate:

$$C_{in} = \frac{14.2 * \sqrt{\frac{2.000}{5} - \left(\frac{2.000}{5}\right)^2}}{2} = 3.47 \Rightarrow 4 \text{ caps}$$

$$R_{offset} = \frac{0.089 - .014 * 2.000 - .029}{0.029 + 2.000} * 1000 = 15.8\Omega$$

$$R_7 = \frac{14.2 * 0.020 * (1 + 0.67)}{45 * 10^{-6}} = 10.5K\Omega$$

$$R_5 = \frac{14400 * 14.2 * 0.020 * (1 + 0.67) * 1.1}{18 * (0.089 + 0.079 - .024 * 2.000)} = 3.48K\Omega$$

$$X = \frac{0.044 * 14.2}{0.134 + 0.089 - .024 * 2.00} = 3.57$$

$$Y = \frac{0.044 * 14.2}{0.134 - 0.089 + \frac{14400 * 14.2 * 0.020}{18 * 3640 * 1.1}} = 6.14$$

Since $Y > X$, we choose Y, and round up to find we need 7 capacitors for C_{OUT} .

A detailed explanation of this calculation may be found in Applications Bulletin AB-24.

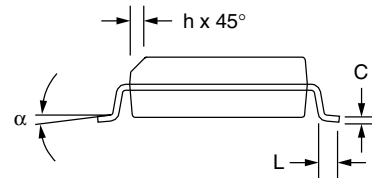
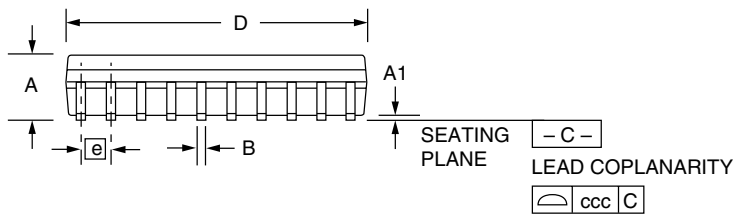
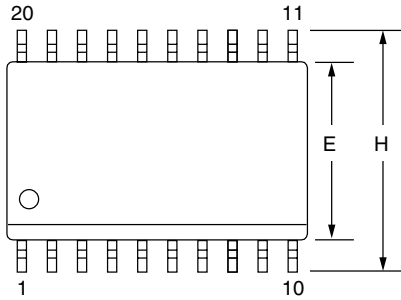
Mechanical Dimensions

20 Lead SOIC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



Ordering Information

Product Number	Description	Package
FAN5070M	VRM8.5	20 pin SOIC

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