FAIRCHILD SEMICONDUCTOR®

October 2005

# FAN5109
# Dual Bootstrapped 12V MOSFET Driver

## Features

- Drives N-channel High-Side and Low-Side MOSFETs in a Synchronous Buck Configuration
- Enhanced Upgrade to FAN5009
- Direct Interface to FAN5019B/FAN5182 and other compatible PWM Controllers
- 12V High-Side and 12V Low-Side Drive
- Internal Adaptive "Shoot-Through" Protection
- Fast Rise and Fall times
- Switching Frequency above 500kHz
- $\overline{OD}$ input for Output Disable – allows for synchronization with PWM Controller
- SOIC-8 Package

## Applications

- Multi-phase VRM/VRD Regulators for Microprocessor Power
- High Current/High Frequency DC/DC Converters
- High Power Modular Supplies

## General Description

The FAN5109 is a high-frequency driver, specifically designed to drive N-Channel power MOSFETs in a synchronous-rectified buck converter. This driver, combined with a Fairchild Multi-Phase PWM controller and power MOSFETs, form a complete core voltage regulator solution for advanced microprocessors.

The FAN5109 drives the upper and lower MOSFET gates of a synchronous buck regulator up to $12V_{GS}$. The FAN5109's output drivers can efficiently switch power MOSFETs at frequencies above 500kHz. The circuit's adaptive shoot-through protection prevents the MOSFETs from conducting simultaneously.

The FAN5109 is rated for operation from 0°C to +85°C and is available in a low-cost SOIC-8 package.

## Ordering Information

| Part Number | Temperature Range | Pb-Free | Package | Packing | Qty/Reel |
|---|---|---|---|---|---|
| FAN5109MX | 0°C to 85°C | Yes | SOIC-8 | Tape and Reel | 2500 |

**Note:** Contact Fairchild Sales for availability of leaded parts.

## Typical Application

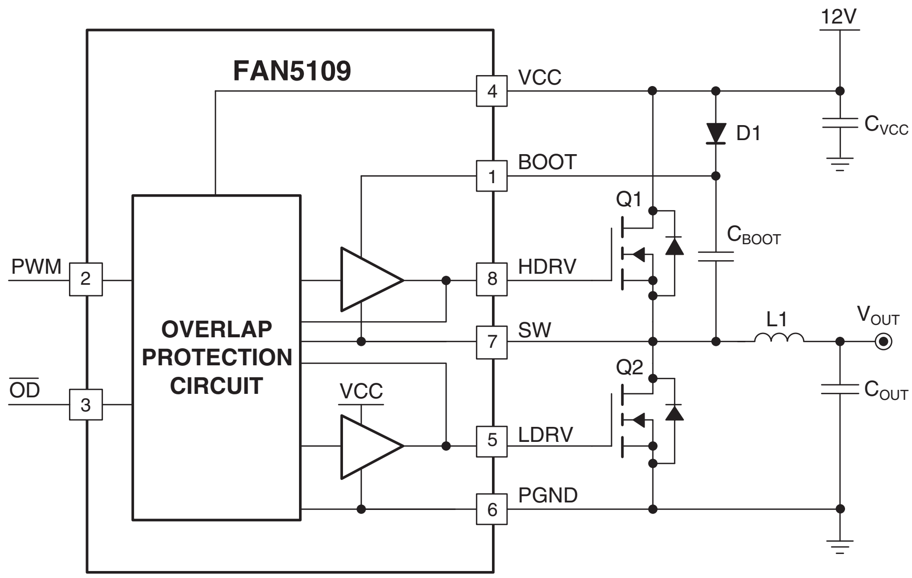



**Figure 1. Typical Application**

## Pin Configuration

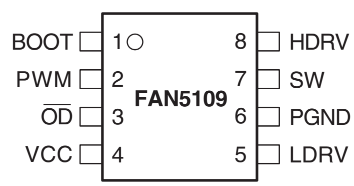



**Figure 2. 8-Pin SOIC Package**

# Pin Definitions

| Pin # | Pin Name | Pin Function Description |
|---|---|---|
| 1 | BOOT | **Bootstrap Supply Input.** Provides voltage supply to the high-side MOSFET driver. Connect to bootstrap capacitor and diode. |
| 2 | PWM | **PWM Signal Input.** Accepts a logic-level PWM signal from the controller. |
| 3 | $\overline{OD}$ | **Output Disable.** When low, this pin disables FET switching (HDRV and LDRV are held low). |
| 4 | VCC | **Power Input**. +12V bias power. Bypass with a 1µF ceramic capacitor. |
| 5 | LDRV | **Low Side Gate Drive Output.** Connect to the gate of the low-side power MOSFET(s). |
| 6 | PGND | **Power Ground.** Connect directly to the source of low-side MOSFET(s) and $C_{VCC.}$ |
| 7 | SW | **Switch Node Input**. Connect as shown in Figure 1. SW provides return for the high-side bootstrapped driver and acts as a sense point for the adaptive shoot-thru protection. |
| 8 | HDRV | **High Side Gate Drive Output**. Connect to the gate of the high-side power MOSFET(s). |

## Functional Block Diagram

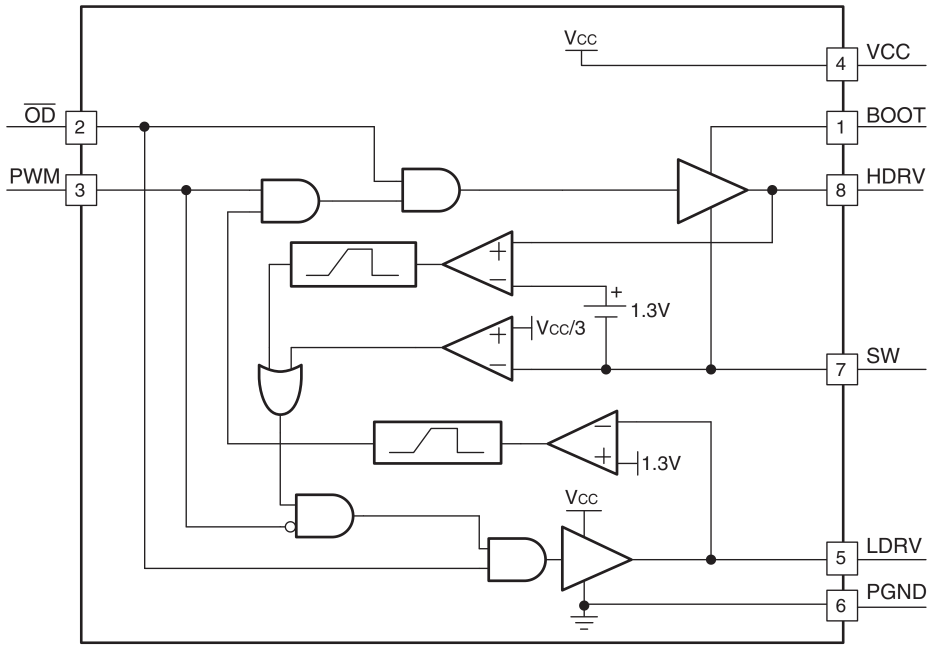



**Figure 3. Functional Block Diagram**

## Absolute Maximum Ratings

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually, not in combination. Unless otherwise specified, voltages are referenced to PGND.

| Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|
| VCC to PGND | | –0.3 | 15 | V |
| PWM and $\overline{OD}$ pins | | –0.3 | 5.5 | V |
| SW to PGND | Continuous | –1 | 15 | V |
| | Transient ( t=100nsec, F ≤ 500kHz) | –5(1) | 25 | V |
| BOOT to SW | | –0.3 | 15 | V |
| BOOT to PGND | Continuous | –0.3 | 30 | V |
| | Transient ( t=100nsec, F ≤ 500kHz) | | 38(1) | V |
| HDRV | | $V_{SW}$–1 | $V_{BOOT}$+0.3 | V |
| LDRV | Continuous | –0.5 | $V_{CC}$ | V |
| | Transient ( t=200nsec) | –2(1) | $V_{CC}$+0.3 | V |

**Notes:**

1. For transient derating beyond the levels indicated, refer to the graphs on page 9.

## Thermal Information

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Junction Temperature ($T_J$) | 0 | | 150 | °C |
| Storage Temperature | –65 | | 150 | °C |
| Lead Soldering Temperature, 10 seconds | | | 300 | °C |
| Vapor Phase, 60 seconds | | | 215 | °C |
| Infrared, 15 seconds | | | 220 | °C |
| Power Dissipation ($P_D$) $T_A$ = 25°C | | | 715 | mW |
| Thermal Resistance, SO8 – Junction to Case $\theta_{JC}$ | | 40 | | °C/W |
| Thermal Resistance, SO8 – Junction to Ambient $\theta_{JA}$ | | 140 | | °C/W |

## Recommended Operating Conditions

| Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply Voltage $V_{CC}$ | $V_{CC}$ to PGND | 10 | 12 | 13.5 | V |
| Ambient Temperature ($T_A$) | | 0 | | 85 | °C |
| Junction Temperature ($T_J$) | | 0 | | 125 | °C |

## Electrical Specifications

$V_{CC}$ = 12V, and $T_A$ = 25°C using the circuit in Figure 4 unless otherwise noted. The • denotes specifications which apply over the full operating temperature range.

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Input Supply** | | | | | | | |
| VCC Voltage Range | $V_{CC}$ | | • | 6.4 | 12 | 13.5 | V |
| VCC Current | $I_{CC}$ | $\overline{OD}$ = 0V | • | | 2.5 | 4 | mA |
| **$\overline{OD}$ Input** | | | | | | | |
| Input High Voltage | $V_{IH\ (\overline{OD})}$ | | • | 2.5 | | | V |
| Input Low Voltage | $V_{IL\ (\overline{OD})}$ | | • | | | 0.8 | V |
| Input Hysteresis | | | • | | 550 | | mV |
| Input Current | $I_{\overline{OD}}$ | $\overline{OD}$ = 3.0V | • | –300 | | +300 | nA |
| Propagation Delay[2] | $t_{pdl(\overline{OD})}$ | See Figure 5 | | | 25 | 40 | ns |
| | $t_{pdh(\overline{OD})}$ | | | | 15 | 30 | ns |
| **PWM Input** | | | | | | | |
| Input High Voltage | $V_{IH(PWM)}$ | | • | 3.5 | | | V |
| Input Low Voltage | $V_{IL(PWM)}$ | | • | | | 0.8 | V |
| Input Current | $I_{IL(PWM)}$ | | • | -1 | | +1 | µA |
| **High-Side Driver** | | | | | | | |
| Output Resistance, Sourcing | $R_{HUP}$ | $V_{BOOT} – V_{SW}$ = 12V | | | 2.5 | 3.3 | Ω |
| Source Current[2] | | $V_{DS}$ = -10V | | | 2.0 | | A |
| Output Resistance, Sinking | $R_{HDN}$ | $V_{BOOT} – V_{SW}$ = 12V | | | 1.1 | 1.5 | Ω |
| Sink Current[2] | | $V_{DS}$ = 10V | | | 3.0 | | A |
| Transition Times[2,4] | $t_{R(HDRV)}$ | Figure 4 | | | 25 | 40 | ns |
| | $t_{F(HDRV)}$ | | | | 15 | 25 | ns |
| Propagation Delay[2,3] | $t_{pdh(HDRV)}$ | See Figure 6 | | | 40 | 55 | ns |
| | $t_{pdl(HDRV)}$ | | | | 25 | 40 | ns |
| **Low-Side Driver** | | | | | | | |
| Output Resistance, Sourcing | $R_{LUP}$ | | | | 2.0 | 2.6 | Ω |
| Source Current[2] | | $V_{DS}$ = -10V | | | 2.7 | | A |
| Output Resistance, Sinking | $R_{LDN}$ | | | | 0.9 | 1.2 | Ω |
| Sink Current[2] | | $V_{DS}$ = 10V | | | 3.5 | | A |
| Transition Times[2,4] | $t_{R(LDRV)}$ | Figure 4 | | | 20 | 30 | ns |
| | $t_{F(LDRV)}$ | | | | 15 | 25 | ns |
| Propagation Delay[2,3] | $t_{pdh(LDRV)}$ | See Figure 6 | | | 20 | 30 | ns |
| | $t_{pdl(LDRV)}$ | | | | 15 | 25 | ns |
| | $t_{pdh(LDF)}$ | See Adaptive Gate Drive Circuit description (page 10) | | | 160 | | ns |

**Notes:**
1. All limits at operating temperature extremes are guaranteed by design, characterization and statistical quality control.
2. Specifications guaranteed by design/characterization (not production tested).
3. For propagation delays, “tpdh” refers to low-to-high signal transition and “tpdl” refers to high-to-low signal transition.
4. Transition times are defined for 10% and 90% of DC values.

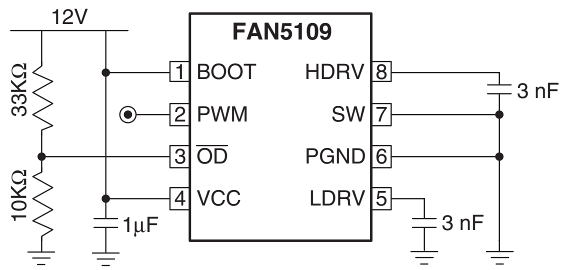



**Figure 4. Test Circuit**

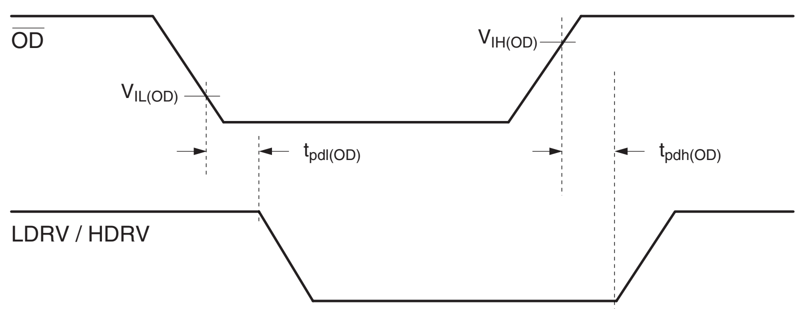



**Figure 5. Output Disable Timing**

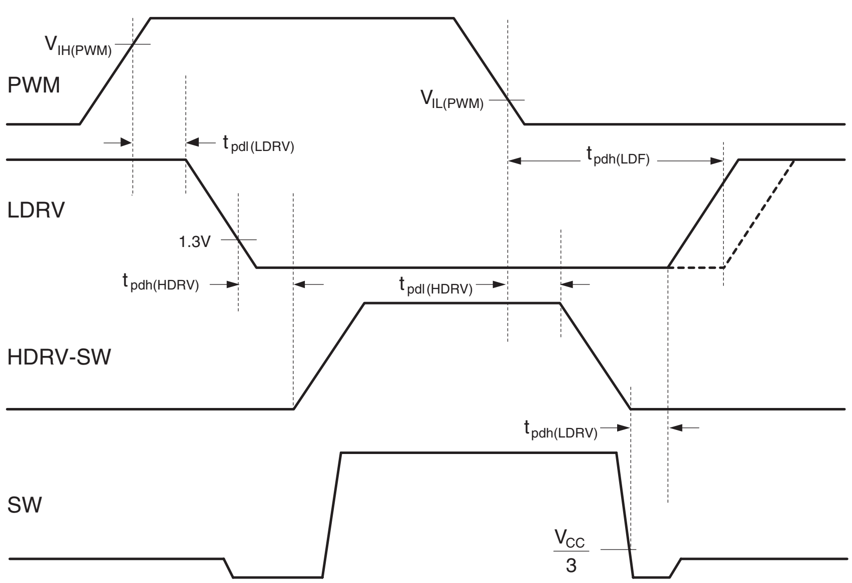
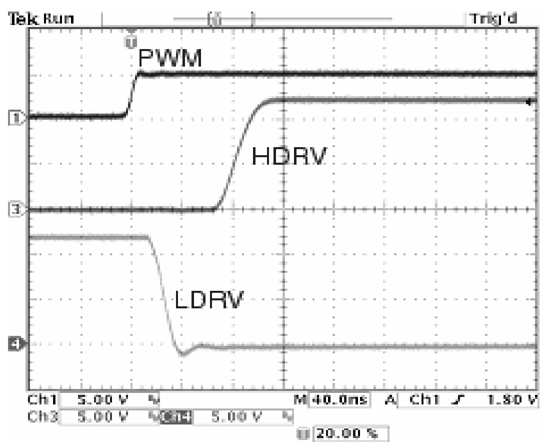
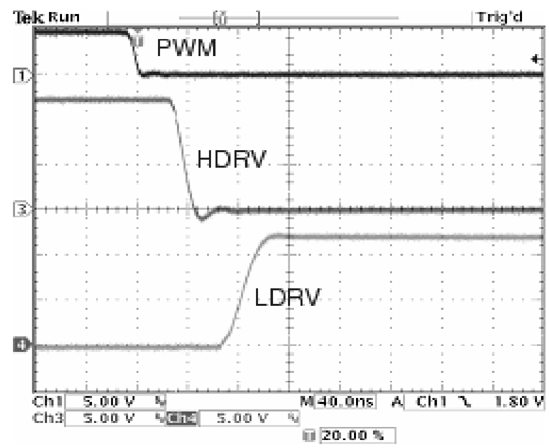



**Figure 6. Adaptive Gate Drive Timing**

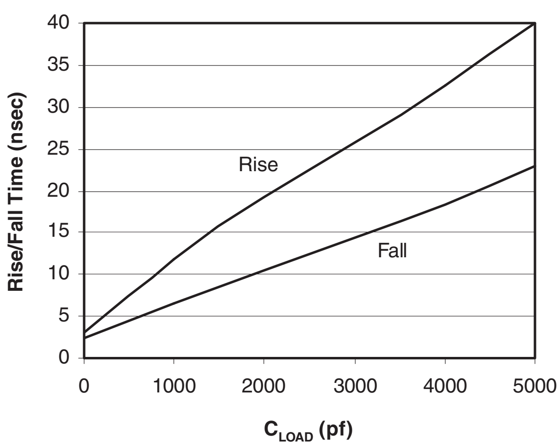
## Typical Characteristics



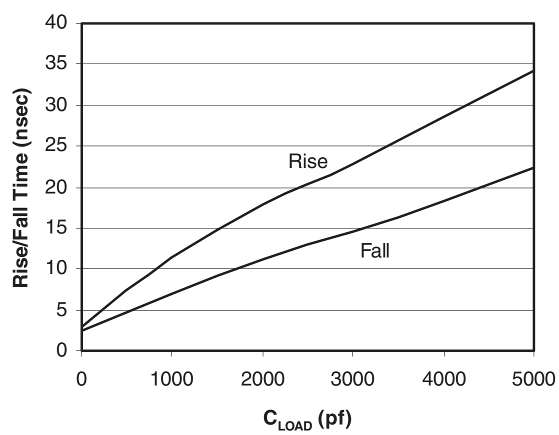

**Gate Drive Rise and Fall Times (1)**



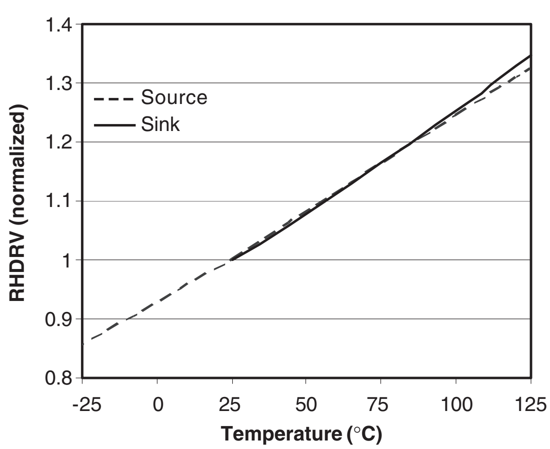

**Gate Drive Rise and Fall Times (2)**



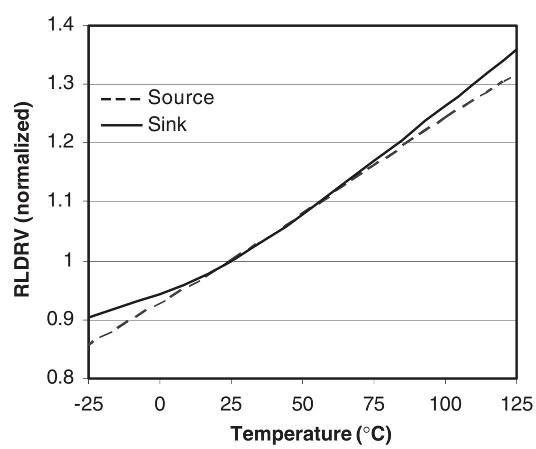

**HDRV Rise/Fall Times vs. $C_{LOAD}$**




**LDRV Rise/Fall Times vs. $C_{LOAD}$**

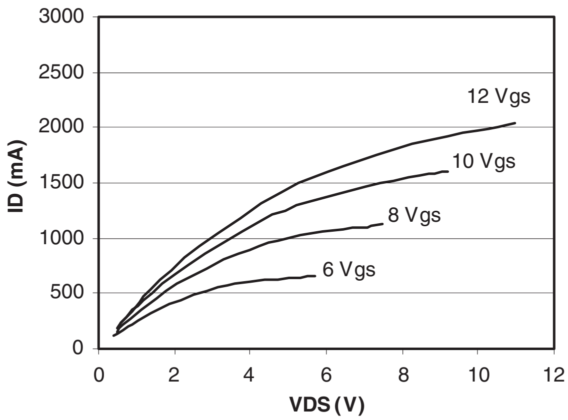



**HDRV Normalized Impedance vs. Temperature**

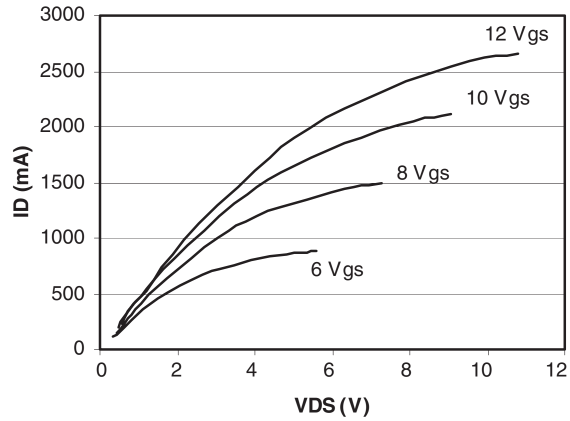



**LDRV Normalized Impedance vs. Temperature**

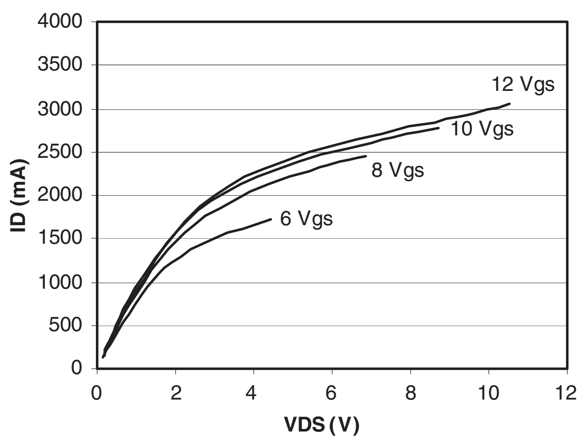
## Typical Performance Characteristics (continued)



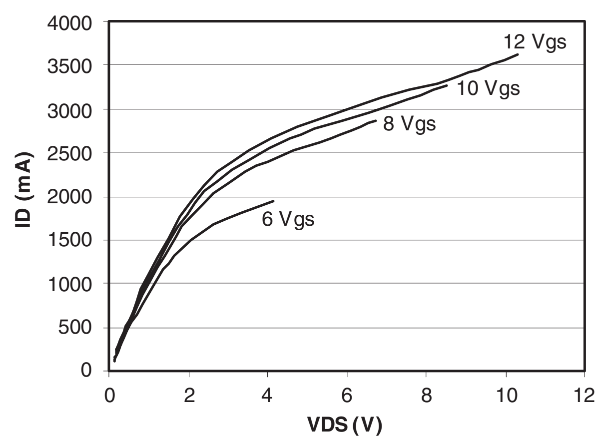

**HDRV Pull-Up (Sourcing)**




**LDRV Pull-Up (Sourcing)**

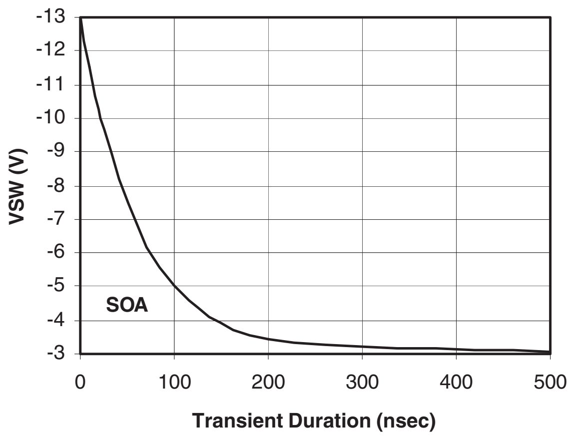



**HDRV Pull-Down (Sinking)**

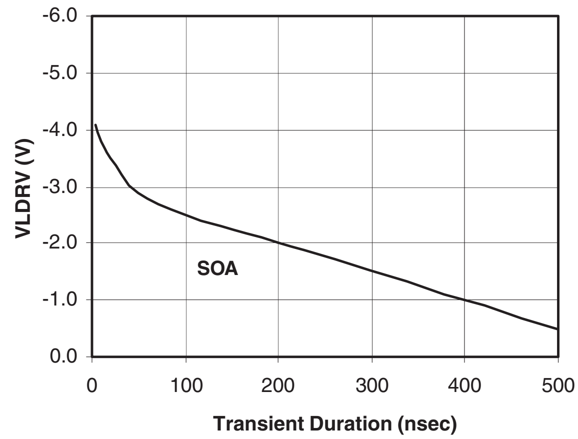



**LDRV Pull-Down (Sinking)**

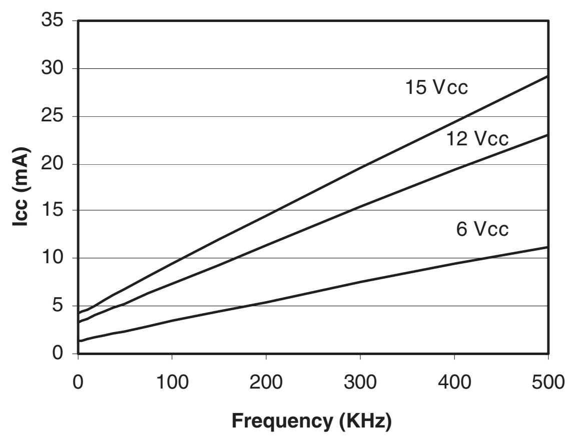
## Typical Performance Characteristics (continued)




**Negative SW Voltage Transient**




**Negative LDRV Voltage Transient**




**Operating Current vs. Frequency**

$I_{CC}$ [mA] = $V_{CC}$ (0.26 + 3.38 $F_{SW}$) where $F_{SW}$ is in MHz

## Circuit Description

The FAN5109 is a driver optimized for driving N-channel MOSFETs in a synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs.

For a more detailed description of the FAN5109 and its features, refer to the Typical Application Diagram (Figure 1) and Functional Block Diagram (Figure 3).

### Low-Side Driver

The FAN5109's low-side driver (LDRV) is designed to drive ground referenced low $R_{DS(on)}$ N-channel MOSFETs. The bias for LDRV is internally connected between $V_{CC}$ and PGND. When the driver is enabled, the driver's output is 180° out of phase with the PWM input. When the FAN5109 is disabled ($\overline{OD}$ = 0V), LDRV is held low.

### High-Side Driver

The FAN5109's high-side driver (HDRV) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit, consisting of an external diode and bootstrap capacitor ($C_{BOOT}$) .

During start-up, SW is held at PGND, allowing $C_{BOOT}$ to charge to $V_{CC}$ through the diode. When the PWM input goes high, HDRV will begin to charge the high-side MOSFET's gate (Q1). During this transition, charge is transferred from $C_{BOOT}$ to Q1's gate. As Q1 turns on, SW rises to $V_{IN}$, forcing the BOOT pin to $V_{IN} + V_{C(BOOT)}$, which provides sufficient $V_{GS}$ enhancement for Q1.

To complete the switching cycle, Q1 is turned off by pulling HDRV to SW. $C_{BOOT}$ is then recharged to $V_{CC}$ when SW falls to PGND.

HDRV output is in phase with the PWM input. When the driver is disabled, the high-side gate is held low.

### Adaptive Gate Drive Circuit

The FAN5109 embodies an advanced design that ensures minimum MOSFET dead-time while eliminating potential shoot-through (cross-conduction) currents. It senses the state of the MOSFETs and adjusts the gate drive, adaptively, to ensure they do not conduct simultaneously. Refer to "Gate Drive Rise and Fall Times" waveforms on page 7 for the relevant timing information.

To prevent overlap during the low-to-high switching transition (Q2 OFF to Q1 ON), the adaptive circuitry monitors the voltage at the LDRV pin. When the PWM signal goes HIGH, Q2 will begin to turn OFF after some propagation delay as defined by $t_{pdl(LDRV)}$ parameter. Once the LDRV pin is discharged below ~1.3V, Q1 begins to turn ON after adaptive delay $t_{pdh(HDRV)}$.

To preclude overlap during the high-to-low transition (Q1 OFF to Q2 ON), the adaptive circuitry monitors the voltage at the SW pin. When the PWM signal goes LOW, Q1 will begin to turn OFF after some propagation delay ($t_{pdl(HDRV)}$). Once the SW pin falls below ~$V_{CC}$/3, Q2 begins to turn ON after an adaptive delay $t_{pdh(LDRV)}$.

Additionally, $V_{GS}$ of Q1 is monitored. When $V_{GS(Q1)}$ is discharged below ~1.3V, a secondary adaptive delay is initiated, which results in Q2 being driven ON after $t_{pdh(LDF)}$, regardless of the SW state. This function is implemented to ensure $C_{BOOT}$ is recharged after each switching cycle, particularly for cases where the power convertor is sinking current and the SW voltage does not fall below the $V_{CC}$/3 adaptive threshold. Secondary delay $t_{pdh(LDF)}$ is longer than $t_{pdh(LDRV)}$.

## Application Information

### Supply Capacitor Selection

For the supply input ($V_{CC}$) of the FAN5109, a local ceramic bypass capacitor is recommended to reduce the noise and to supply the peak current. Use at least a 1µF, X7R or X5R capacitor. Keep this capacitor close to the FAN5109's $V_{CC}$ and PGND pins.

### Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor ($C_{BOOT}$) and an external diode, as shown in Figure 1. These components should be selected after the high-side MOSFET has been chosen. The required capacitance is determined using the following equation:

$$C_{BOOT} = \frac{Q_G}{\Delta V_{BOOT}} \quad (1)$$

where $Q_G$ is the total gate charge of the high-side MOSFET, and $\Delta V_{BOOT}$ is the voltage droop allowed on the high-side MOSFET drive. For example, the $Q_G$ of the FDD6696 MOSFET is about 35nC @ $12V_{GS}$. For an allowed droop of ~300mV, the required bootstrap capacitance is 100nF. A good quality ceramic capacitor must be used.

The average diode forward current, $I_{F(AVG)}$, can be estimated by:

$$I_{F(AVG)} = Q_{GATE} \times F_{SW} \quad (2)$$

where $F_{SW}$ is the switching frequency of the controller.

The peak surge current rating of the diode should be checked in-circuit, since this is dependent on the equivalent impedance of the entire bootstrap circuit, including the PCB traces.

### Layout Considerations

Use the following general guidelines when designing printed circuit boards (see Figure 7 on the next page):

1. Trace out the high-current paths and use short, wide (>25 mil) traces to make these connections.
2. Connect the PGND pin of the FAN5109 as close as possible to the source of the lower MOSFET.

3. The $V_{CC}$ bypass capacitor should be located as close as possible to $V_{CC}$ and PGND pins.
4. Use vias to other layers when possible to maximize thermal conduction away from the IC.

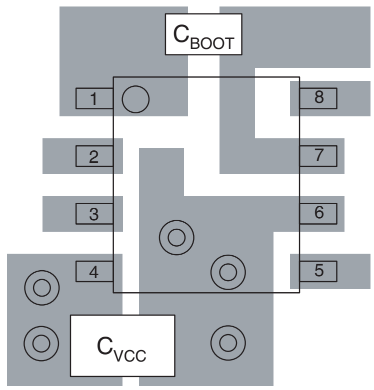



**Figure 7. Recommended layout for SOIC-8 package (not to scale)**

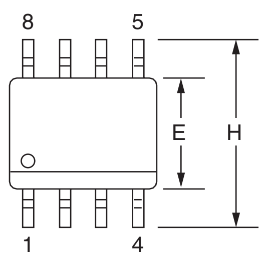
## Mechanical Dimensions

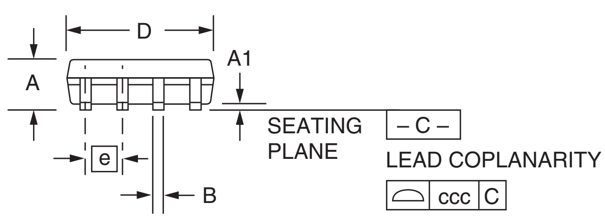
### 0.150, 8 Lead SOIC Package

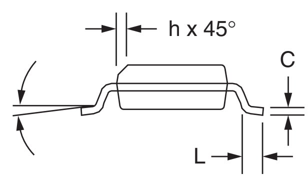
| Symbol | Inches | | Millimeters | | Notes |
|---|---|---|---|---|---|
| | Min. | Max. | Min. | Max. | |
| A | .053 | .069 | 1.35 | 1.75 | |
| A1 | .004 | .010 | 0.10 | 0.25 | |
| B | .013 | .020 | 0.33 | 0.51 | |
| C | .0075 | .010 | 0.20 | 0.25 | 5 |
| D | .189 | .197 | 4.80 | 5.00 | 2 |
| E | .150 | .158 | 3.81 | 4.01 | 2 |
| e | .050 BSC | | 1.27 BSC | | |
| H | .228 | .244 | 5.79 | 6.20 | |
| h | .010 | .020 | 0.25 | 0.50 | |
| L | .016 | .050 | 0.40 | 1.27 | 3 |
| N | 8 | | 8 | | 6 |
| | 0° | 8° | 0° | 8° | |
| ccc | – | .004 | – | 0.10 | |

**Notes:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.



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SuperSOT™-6
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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
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