FAIRCHILD SEMICONDUCTOR®

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FAN7033MP

2W Stereo Power Amplifier with Fixed Gain

Features

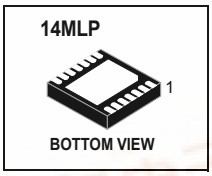
- 1.9W$_{RMS}$ and 2.45W$_{RMS}$ Power Per Each Channel Into 4Ω Load With Less Than 1% and 10% THD+N, Respectively
- Internally Fixed Gain : 21.6dB(Av=12)
- Low Quiescent Current : Typical 5.5mA@5V
- Low Shutdown Current : Typical 0.04μA@5V
- Fully Differential Input, Which Immunes the Common Mode Noise
- Active Low Shutdown Logic
- Guaranteed Stability Under No Load Condition
- Very Small Volume and Thermally Enhanced Surface-Mount 14MLP Package(4mm*4mm)

Typical Applications

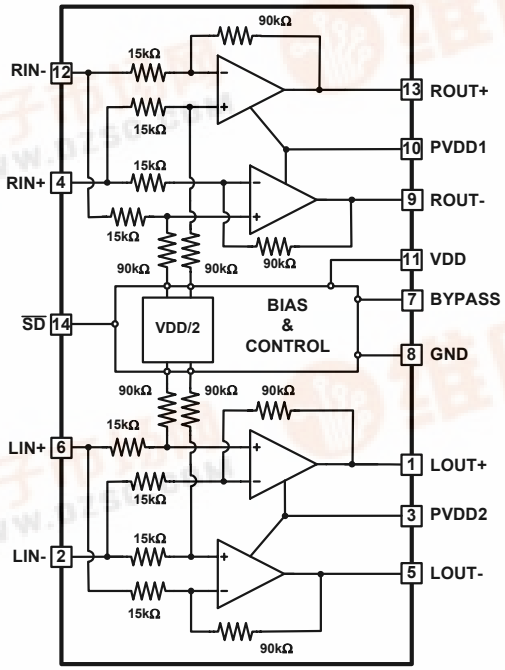
- Cellular Phones
- Notebook Computer
- Desktop Computer

Description

The FAN7033MP is a dual fully differential power amplifier in a thermally enhanced 14-pin MLP package. When delivering 1.9W of continuous RMS power into 4Ω speaker at 5V supply, the FAN7033MP has less than 1% of THD+N over the entire audible frequency range, 20Hz to 20kHz. To save power consumption in the portable applications, the FAN7033MP provides shutdown function. Setting the shutdown pin to ground level, the FAN7033MP falls into shutdown mode and consumes less than 4μA over all supply voltage range, 2.7V to 5.5V. Additional components such as resistors for gain setting and bootstrap capacitors are not needed, making the FAN7033MP well suited for portable sound systems and other hand-held sound equipments. Target applications include the cellular phones, notebook, desktop computers, etc.

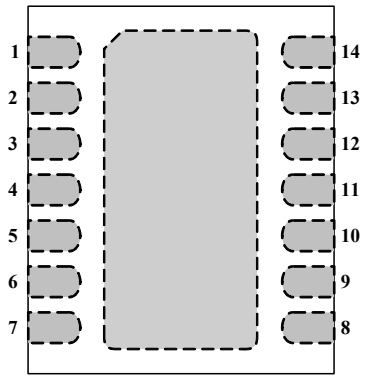


Internal Block Diagram

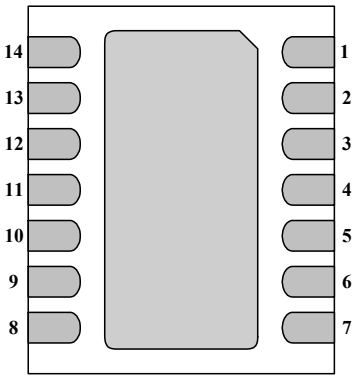


Rev. 1.0.0

Pin Assignments



TOP VIEW



BOTTOM VIEW

Pin Descriptions

Pin No	Symbol	I/O	Decription
1	LOUT+	O	Left Channel (+) Output
2	LIN-	I	Left Channel (-) Input
3**	PVDD2	I	Left Channel Power Supply Voltage
4	RIN+	I	Right Channel (+) Input
5	LOUT-	O	Left Channel (-) Output
6	LIN+	I	Left Channel (+) Input
7	BYPASS	O	Bypass Capacitor Connect
8*	GND	-	Ground
9	ROUT-	O	Right Channel (-) Output
10**	PVDD1	I	Right Channel Power Supply Voltage
11**	VDD	I	Power Supply Voltage
12	RIN-	I	Right Channel (-) Input
13	ROUT+	O	Right Channel (+) Output
14	$\overline{SD}$	I	Shutdown Logic Low $\overline{SD}$=VDD: Device Enable $\overline{SD}$=GND: Device Shutdown

* Pin8(GND) and Exposed PAD are internally tied together.
**For the best performance, VDD, PVDD1 and PVDD2 must be the same voltage level(strongly recommend).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Remark
Maximum Supply Voltage	VDDmax	6.0V	V	
Power Dissipation	P_D	Internally Limited	W	
Operating Temperature	T_{OPG}	-40 ~ +85	°C	
Storage Temperature	T_{STG}	-65 ~ +150	°C	
Junction Temperature	T_{Jmax}	150	°C	
Thermal Resistance (Junction to Ambient)	Rthja*	38	°C/W	Multi-Layer
		145		Single-Layer
ESD Rating (Human Body Model)		2000	V	
ESD Rating (Machine Model)		300	V	

* Rthja was derived using the JEDEC boards.

Operating Rating

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	2.7	-	5.5	V

Electrical Characteristics

(V_{DD} = 5.0V, Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Offset Voltage	V_{OFF}	RL=4Ω, Av=21.6dB	-25	-	25	mV
Supply Current	I_{DD}	No Input, No Load	-	5.5	10	mA
Shutdown Current	I_{SD}	SD = GND	-	0.04	4	μA
Output Power	P_O	THD+N =1%, RL = 4Ω, f = 1kHz	-	1.9	-	W
		THD+N =1%, RL = 8Ω, f = 1kHz	-	1.25	-	W
Total Harmonic Distortion + Noise	THD+N	P_O = 1W, RL=4Ω, f = 20kHz	-	0.6	-	%
Power Supply Rejection Ratio	PSRR	C_{byp} = 1μF, RL=4Ω, BTL Mode, ΔVDD=500mVpp, f = 1kHz	38	68	-	dB
Output Noise Voltage	VN	Input=GND, RL=4Ω, f=1kHz	-	-120	-	dBv

Electrical Characteristics

(V_{DD} = 3.3 V, Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Offset Voltage	V_{OFF}	RL=4Ω, Av=21.6dB	-25	-	25	mV
Supply Current	I_{DD}	No Input, No Load	-	4.5	8	mA
Shutdown Current	I_{SD}	SD = GND	-	0.04	4	μA
Output Power	P_O	THD+N =1%, RL = 4Ω, f = 1kHz	-	0.75	-	W
		THD+N =1%, RL = 8Ω, f = 1kHz	-	0.53	-	W
Total Harmonic Distortion + Noise	THD+N	P_O = 1W, RL=4Ω, f = 20kHz	-	0.75	-	%
Power Supply Rejection Ratio	PSRR	C_{byp} = 1μF, RL=4Ω, BTL Mode, ΔVDD=330mVpp, f = 1kHz	38	68	-	dB
Output Noise Voltage	VN	Input=GND, RL=4Ω, f=1kHz	-	-120	-	dBv

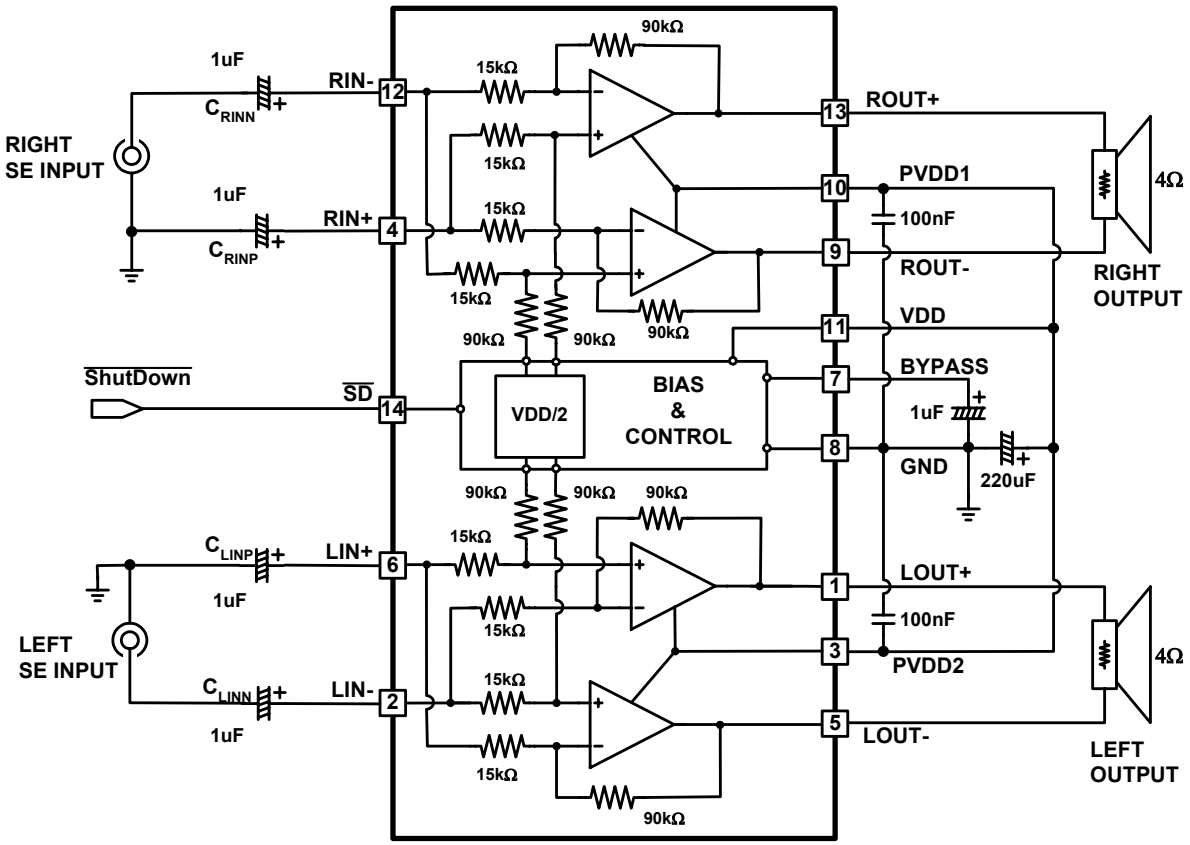
Electrical Characteristics

(V_{DD} = 2.7 V, Ta = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Offset Voltage	V_{OFF}	RL=4Ω, Av=21.6dB	-25	-	25	mV
Supply Current	I_{DD}	No Input, No Load	-	4.1	7	mA
Shutdown Current	I_{SD}	SD = GND	-	0.04	4	μA
Output Power	P_O	THD+N =1%, RL = 4Ω, f = 1kHz	-	0.45	-	W
		THD+N =1%, RL = 8Ω, f = 1kHz	-	0.32	-	W
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W, RL=4Ω, f = 20kHz	-	0.9	-	%
Power Supply Rejection Ratio	PSRR	C_{byp} = 1μF, RL=4Ω, BTL Mode, ΔVDD=270mVpp, f = 1kHz	36	62	-	dB
Output Noise Voltage	VN	Input=GND, RL=4Ω, f=1kHz	-	-120	-	dBv

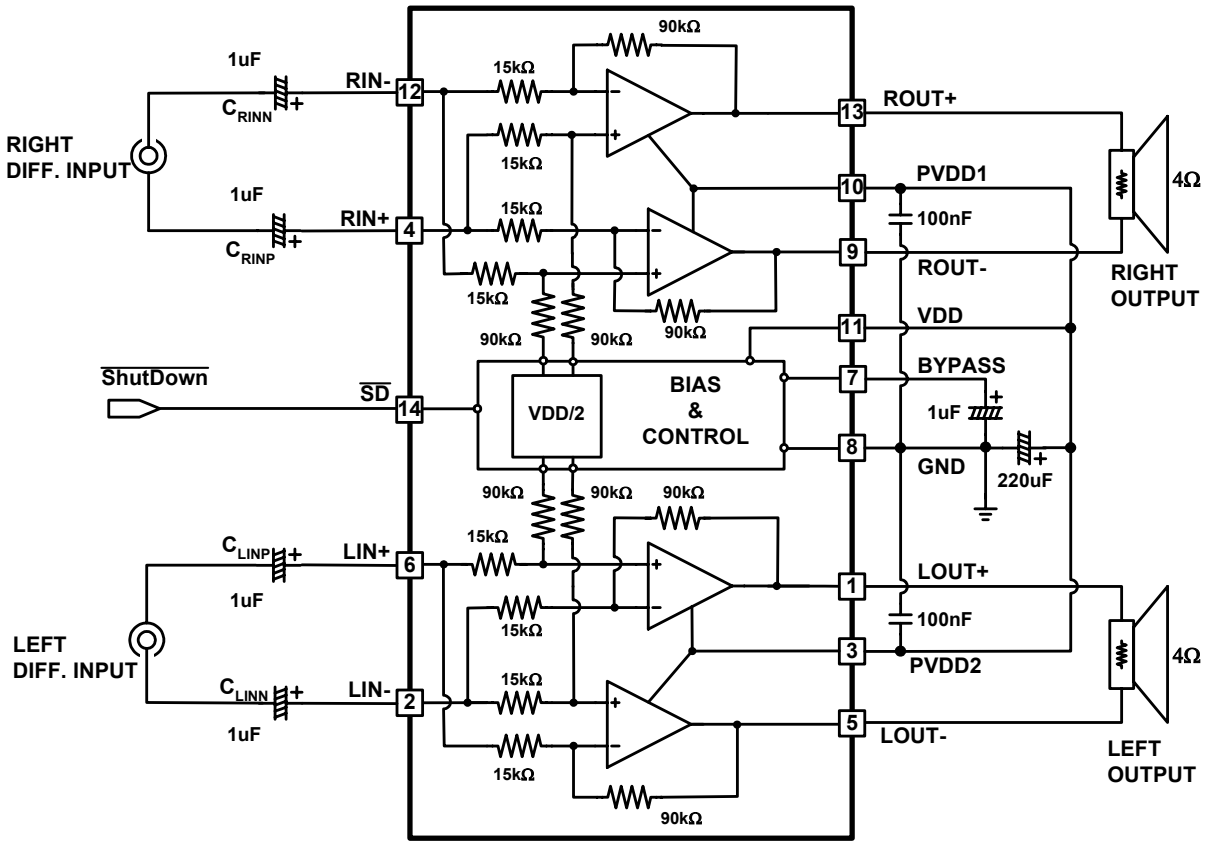
Typical Application Circuits

Single-Ended Input



Typical Application Circuits (continued)

Differential Input



Performance Characteristics : Differential Input

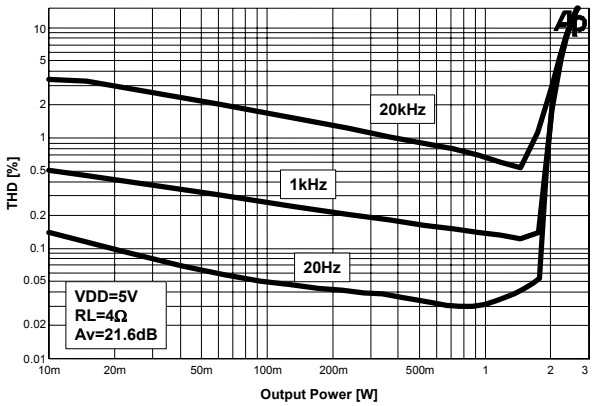


Figure 1. THD+N vs. Output Power

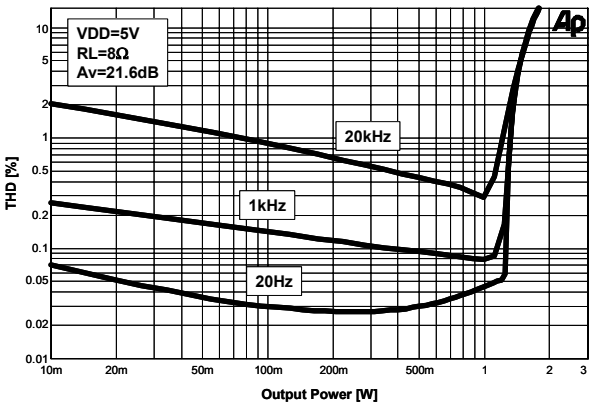


Figure 2. THD+N vs. Output Power

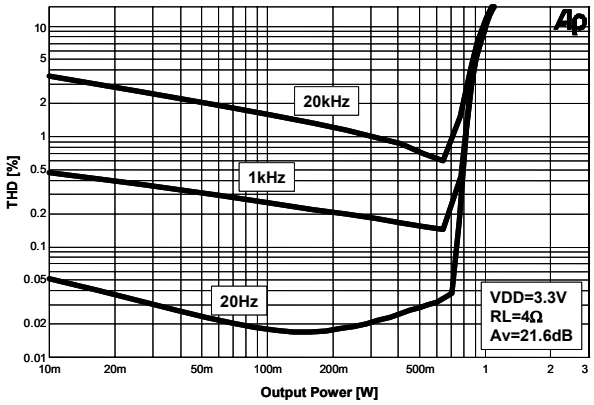


Figure 3. THD+N vs. Output Power

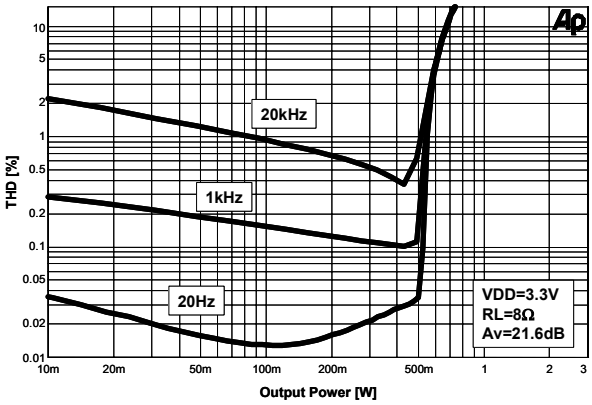


Figure 4. THD+N vs. Output Power

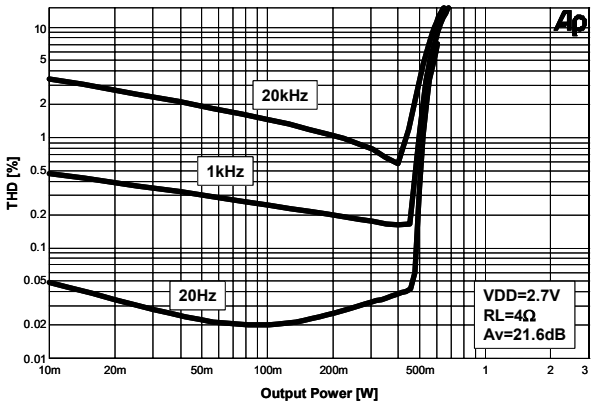


Figure 5. THD+N vs. Output Power

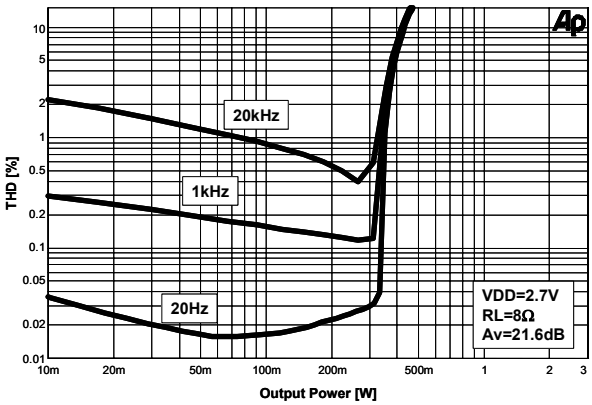


Figure 6. THD+N vs. Output Power

Performance Characteristics(Continued)

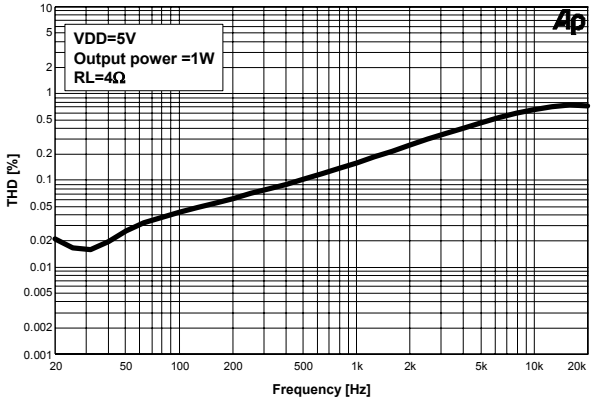


Figure 7. THD+N vs. Frequency

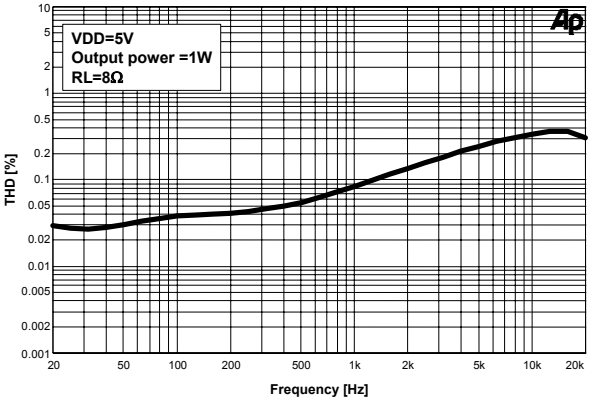


Figure 8. THD+N vs. Frequency

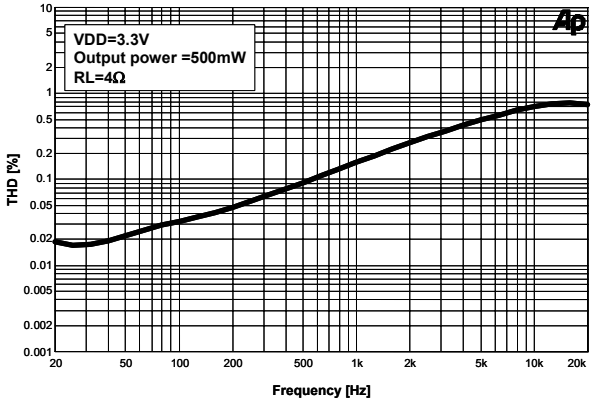


Figure 9. THD+N vs. Frequency

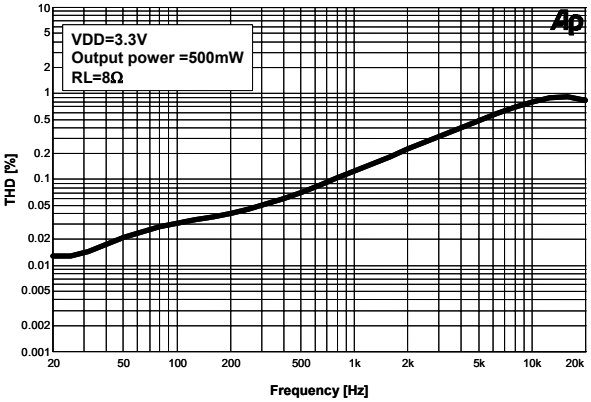


Figure 10. THD+N vs. Frequency

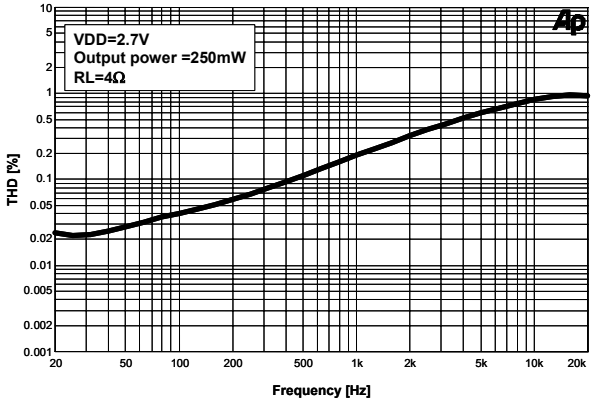


Figure 11. THD+N vs. Frequency

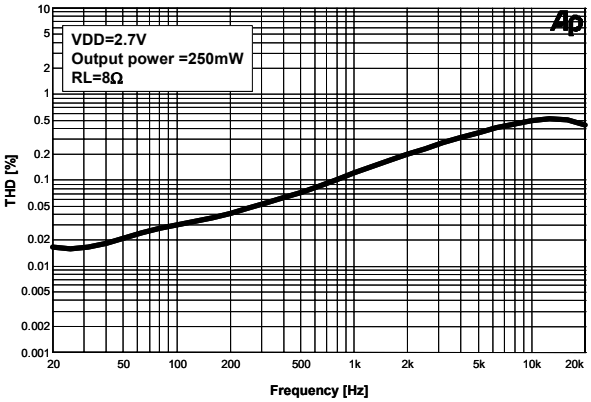


Figure 12. THD+N vs. Frequency

Performance Characteristics(Continued)

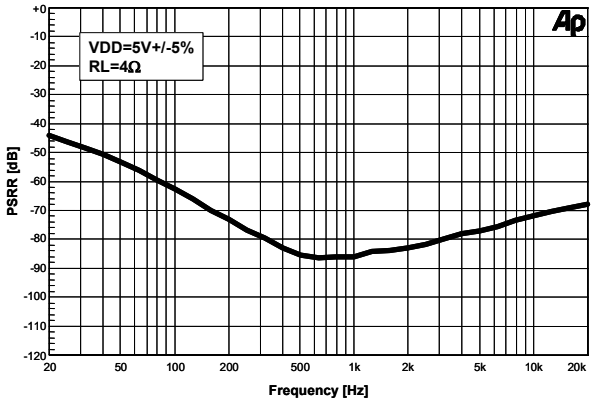


Figure 13. PSRR vs. Frequency

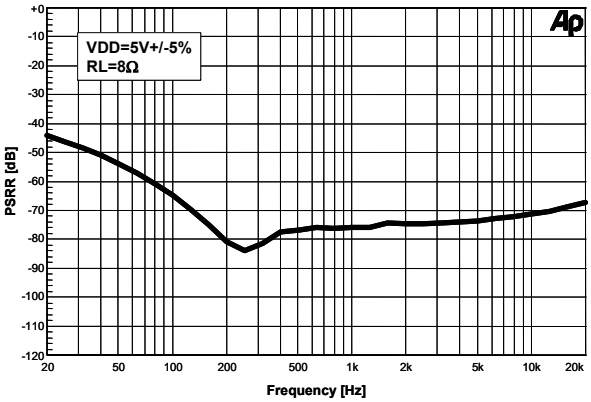


Figure 14. PSRR vs. Frequency

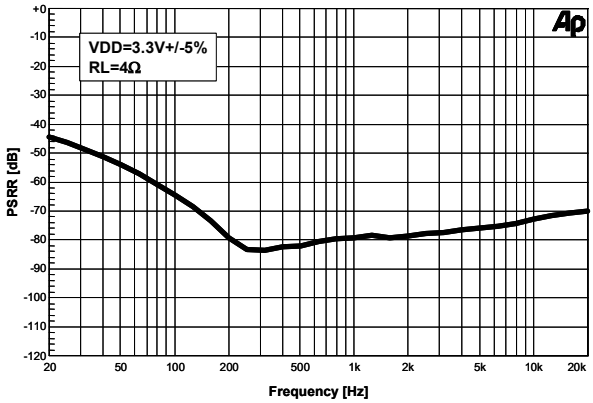


Figure 15. PSRR vs. Frequency

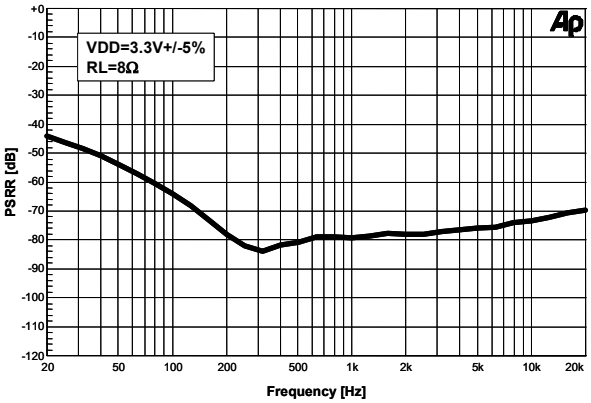


Figure 16. PSRR vs. Frequency

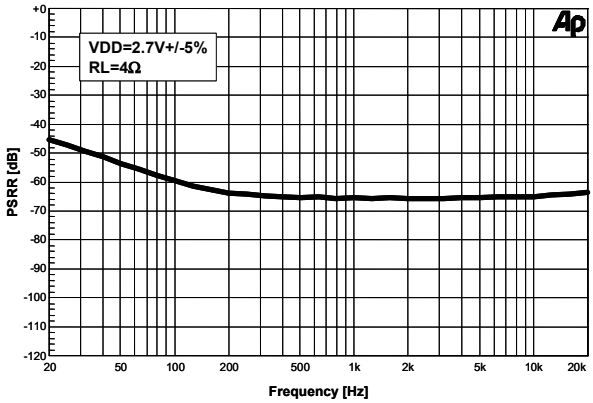


Figure 17. PSRR vs. Frequency

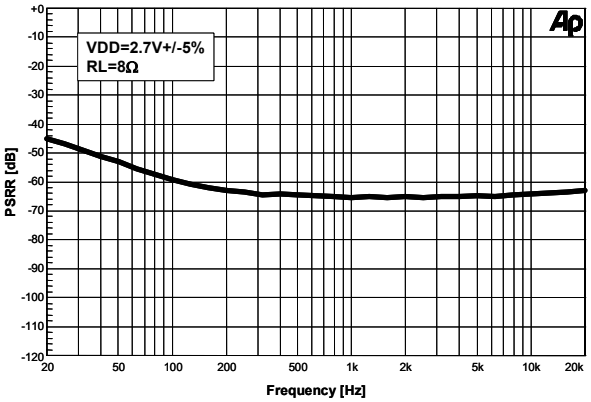


Figure 18. PSRR vs. Frequency

Performance Characteristics(Continued)

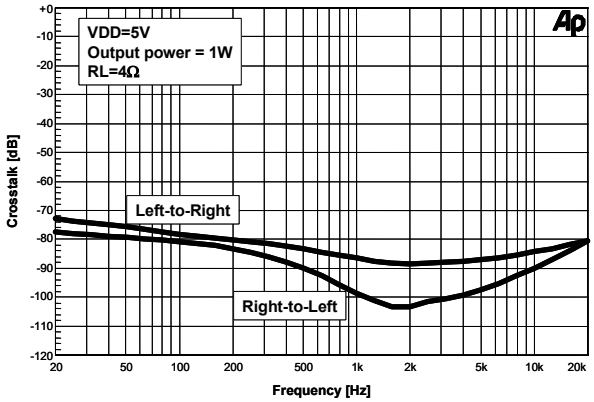


Figure 19. Crosstalk vs. Frequency

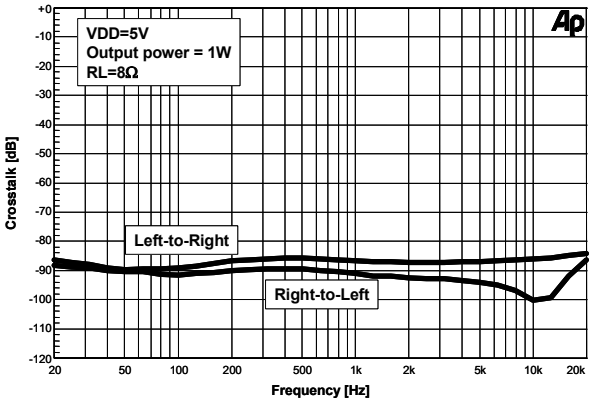


Figure 20. Crosstalk vs. Frequency

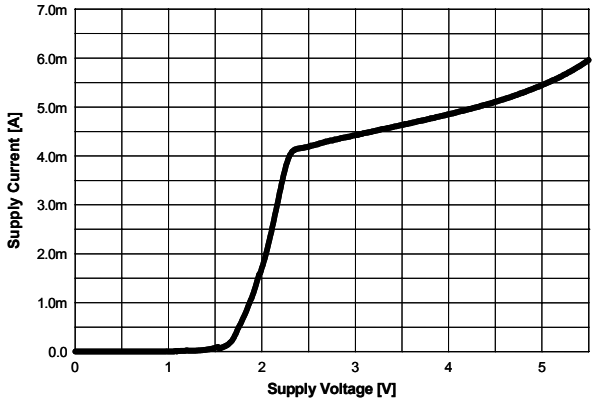


Figure 21. Supply Current vs. Supply Voltage

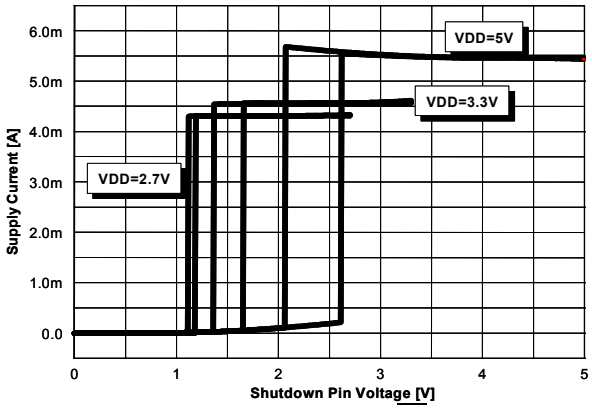


Figure 22. Supply Currrent vs. $\overline{SD}$ Voltage

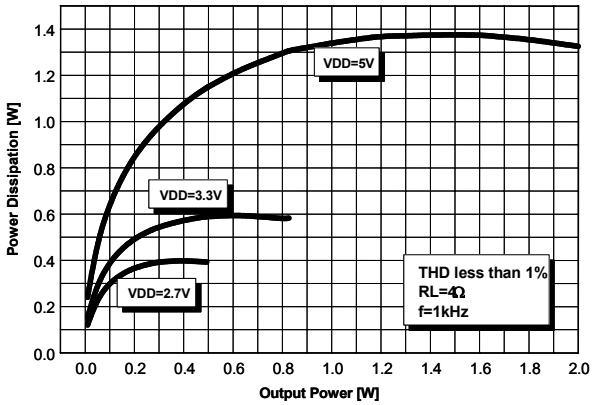


Figure 23. Power Dissipation vs. Output Power

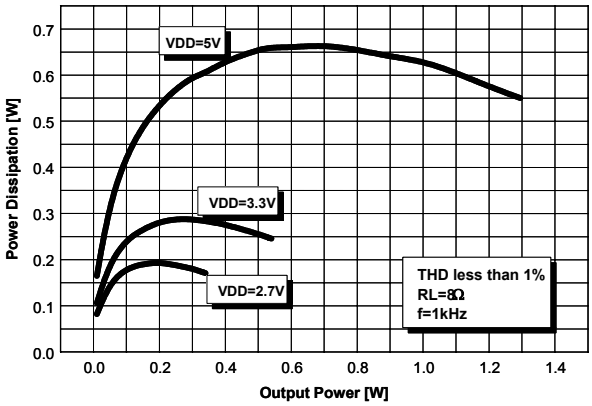


Figure 24. Power Dissipation vs. Output Power

Performance Characteristics(Continued)

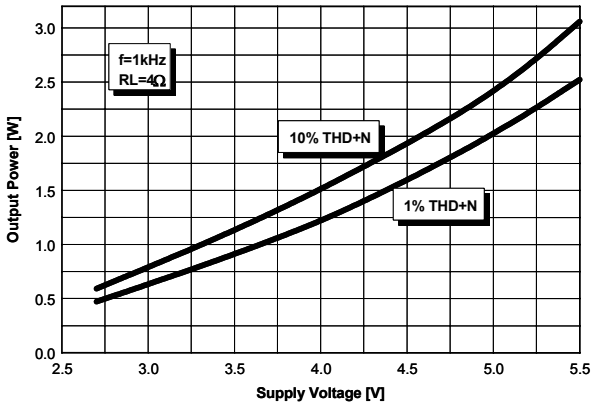


Figure 25. Output Power vs. Supply Voltage

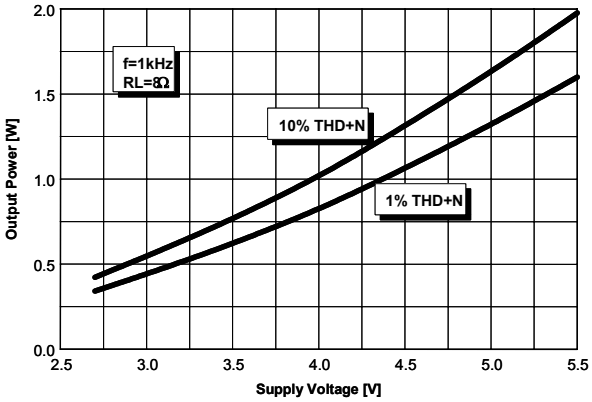


Figure 26. Output Power vs. Supply Voltage

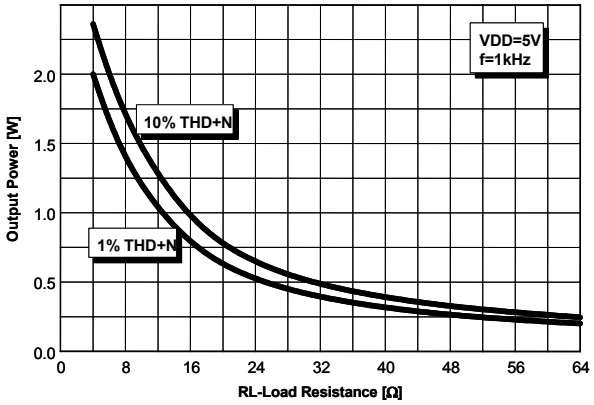


Figure 27. Output Power vs. Output Load

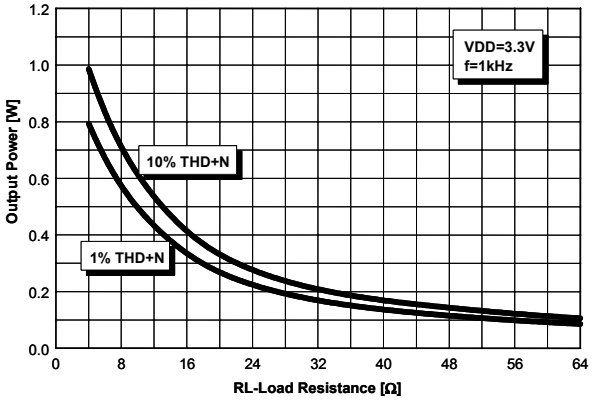


Figure 28. Output Power vs. Output Load

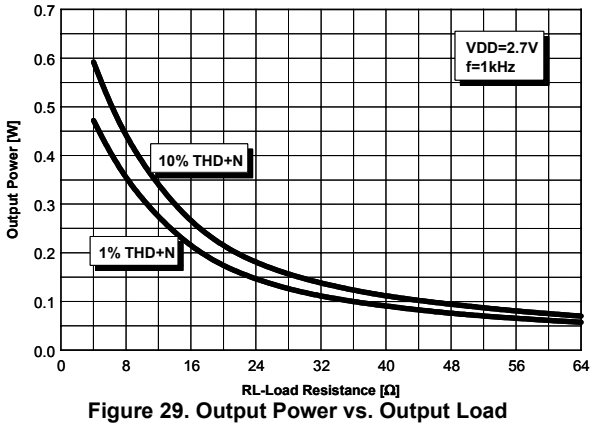


Figure 29. Output Power vs. Output Load

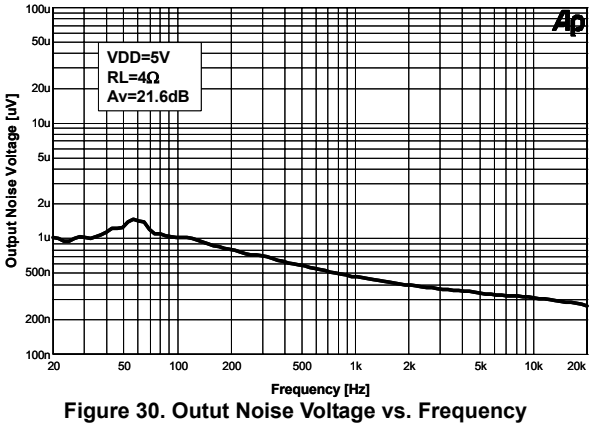


Figure 30. Outut Noise Voltage vs. Frequency

Performance Characteristics : Single-Ended Input

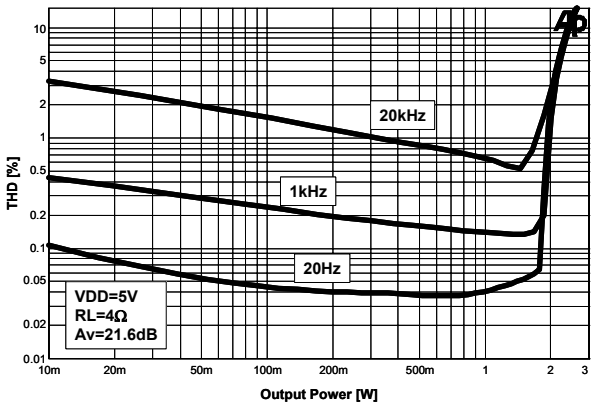


Figure 33. THD+N vs. Output Power

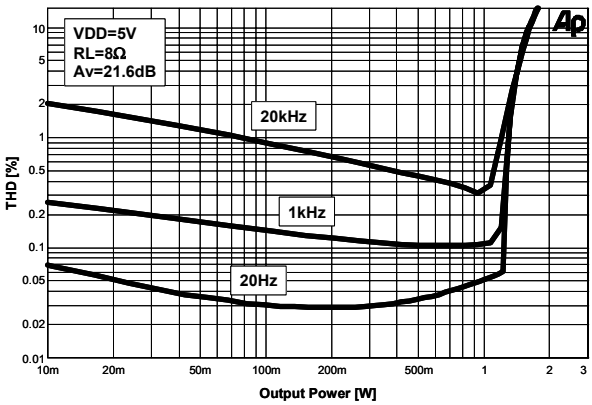


Figure 34. THD+N vs. Output Power

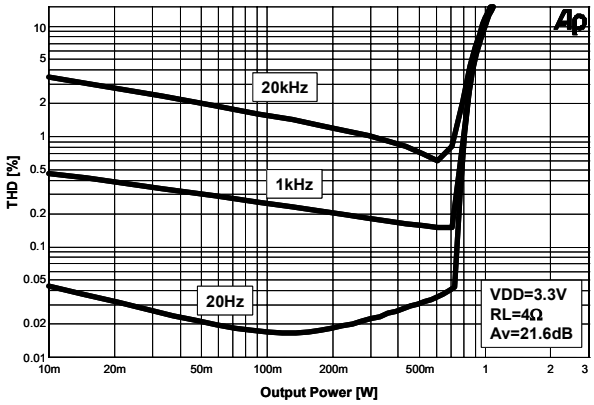


Figure 35. THD+N vs. Output Power

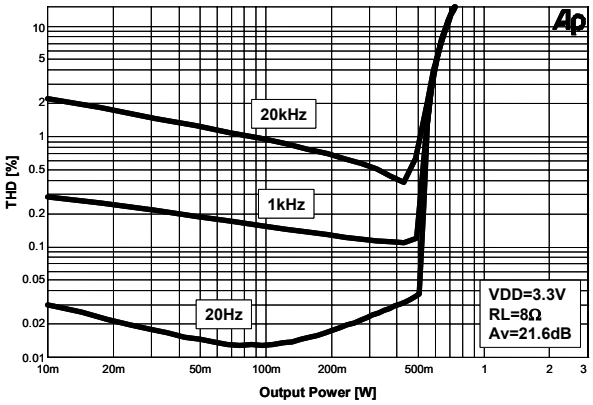


Figure 36. THD+N vs. Output Power

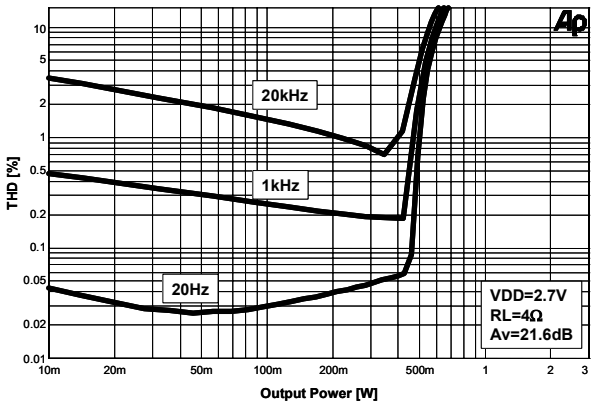


Figure 37. THD+N vs. Output Power

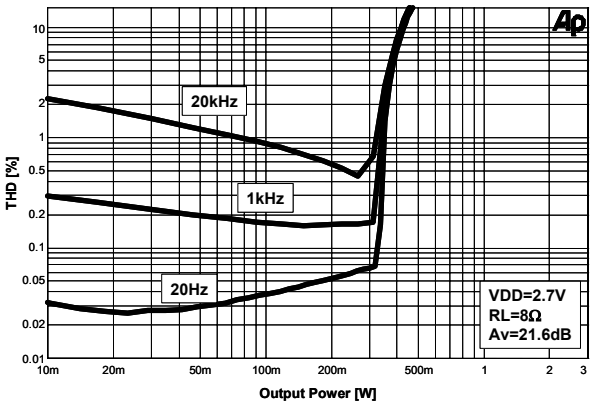


Figure 38. THD+N vs. Output Power

Performance Characteristics(Continued)

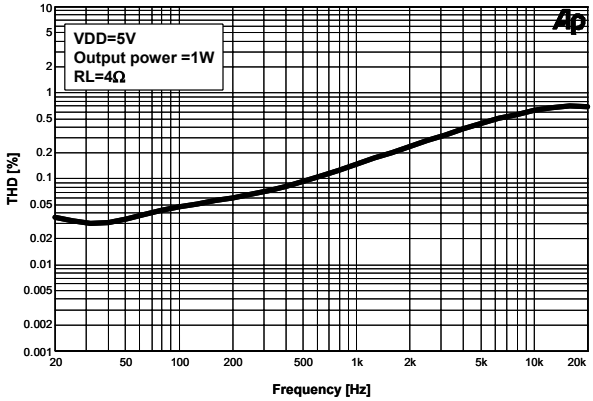


Figure 39. THD+N vs. Frequency

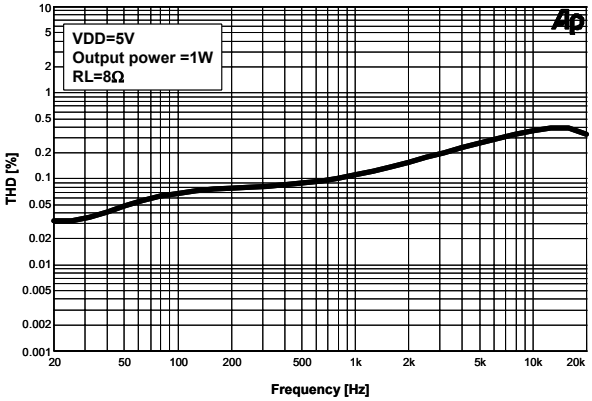


Figure 40. THD+N vs. Frequency

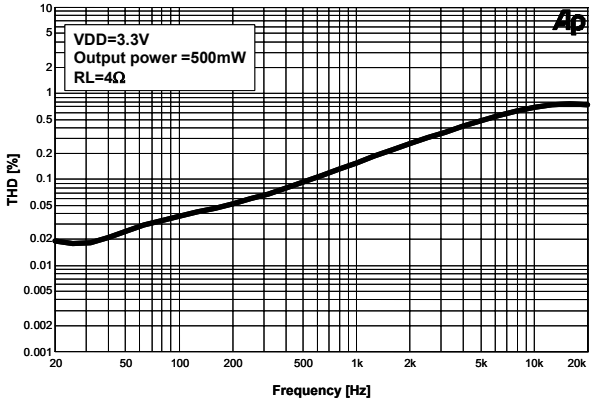


Figure 41. THD+N vs. Frequency

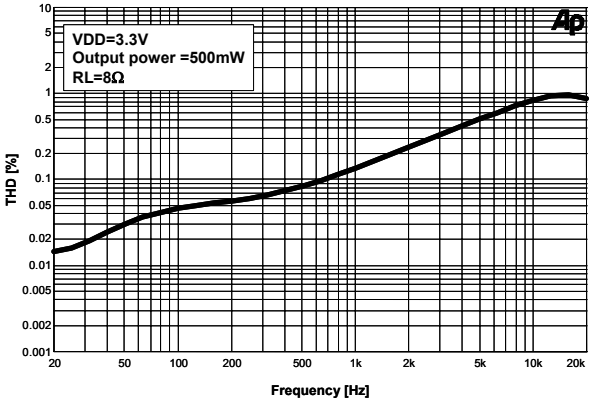


Figure 42. THD+N vs. Frequency

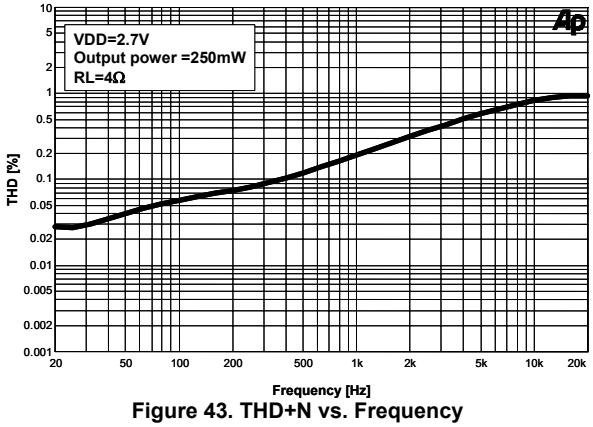


Figure 43. THD+N vs. Frequency

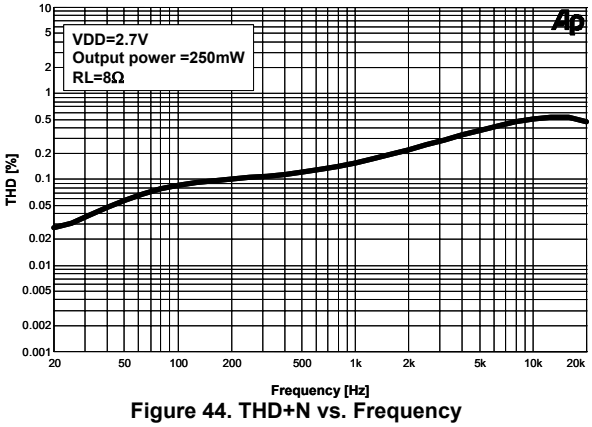


Figure 44. THD+N vs. Frequency

Performance Characteristics(continued)

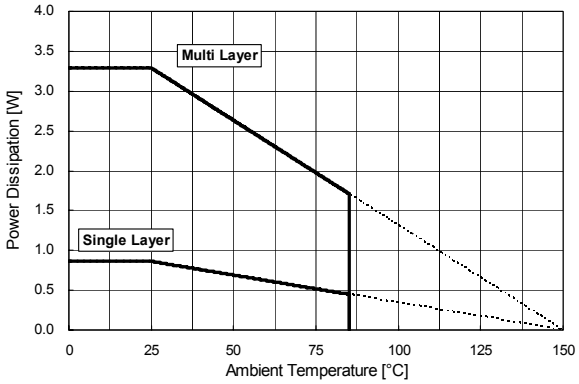


Figure 45. Power Derating Curve

Notes :
- Single Layer(JESD51-3) :
  Thermal Vias : 0
  Board Size : 76.2mm*114.3mm*1.57mm(JESD51-3)
  Copper Thickness : 2.0oz
  Copper Coverage : Top Layer : Traces + Metalization Area(3.34mm*2.24mm)
- Multi Layer(JESD51-7) :
  Thermal Vias : 6
  Board Size : 76.2mm*114.3mm*1.6mm(JESD51-7)
  Copper Thickness : 2.0oz/1.0oz/1.0oz
  Copper Coverage : Top Layer : Traces + Metalization Area(3.34mm*2.24mm)
  Middle Layers(Power/Ground Planes) : 74.2mm*74.2mm
- JESD51-3 : Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages(Single Layer)
- JESD51-7 : High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages(Multi Layers)
- JESD51-2 : Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection(Still Air)

Applications Information

Functional Description

The FAN7033MP is a stereo power amplifier capable of delivering 1.9W continuous RMS(Root Mean Square) power into 4Ω load with 1% THD(Total Harmonic Distortion). At 10% THD, the FAN7033MP can deliver above 2W into 4Ω load. The FAN7033MP has 5 supply input pins. Three among them are used for positive supply and the rest of them is for the ground. Three positive supply input pins : pin3(PVDD2), pin10(PVDD1) and pin11(VDD) must be tied together. To improve the cross-talk between cannels, these pins are not connected internally. Therefore, these pins must be externally connected on the PCB. Pin 8 and the exposed pad are allocated to ground. Thus, the exposed pad must be connected to the ground.
The FAN7033MP is provided with differential inputs. These inputs increase the common-mode noise immunity. Furthermore, differential configuration in the input section helps to decrease total harmonic distortion and pop noise that occurs when shutdown is released. When only single input is available, the distortion performance is slightly degraded.
To save the standby power consumption, the FAN7033MP provides shutdown function. Putting pin14(SD) to be low, the chip falls into shutdown mode. At this mode, it consumes micro power at the room temperature of 25°C and this power consumption is only due to the leakage current of the chip. This leakage current is the strong function of the temperature. Thus at the high ambient temperature, the shutdown current slightly increases. The logic threshold of shutdown pin lies nearby VDD/2. So, the logic threshold level does not follow TTL logic level. Thus, when the users want to control the chip according to the TTL logic level, some kinds of logic-level-changing circuit may be needed.

Operation of the Amplifier

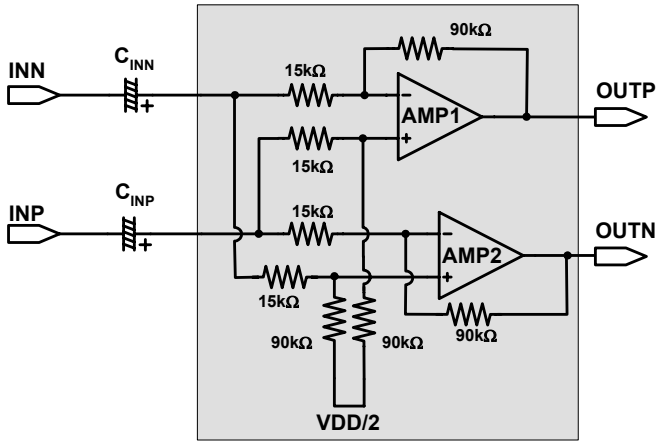


Figure 1. Configuration of Power Amplifier

Figure 1 shows the configuration of the single channel BTL(Bridge-Tied Load) power amplifier. To make the differential input configuration, the FAN7033MP uses several resistor networks as depicted in figure 1. For the input resistor, 15kΩ is used. This resistor converts the input voltage signal to the current signal. The converted current signal flows to the feedback resistor. For FAN7033MP, the feedback resistance is six times larger than input resistance. Thus, the gain is 12(about 21.6dB). For the 5V supply, the input signal has 0.83Vpeak voltage swing makes 10Vpp output swing. The exact gain formula is given by

$$OUTP - OUTN = 12(INP - INN) \quad (1)$$

As shown in equation (1), for the single-ended input case, the gain is also preserved. However, to get the same output swing with the differential input case, the input swing must be double comparing with the differential input swing.

PCB Layout and Supply Regulation

Metal trace resistance between the BTL output and the parasitic resistance of the power supply line both heavily

affect the output power. In order to obtain the maximum power depicted in the performance characteristics figures, outputs, power, and ground lines need wide metal trace. The parasitic resistance of the power line increases ripple noise and degrades the THD and PSRR performance. To reduce such unwanted effect, a large capacitor must be connected between V_{DD} pin and GND pin as close as possible. To improve power supply regulation performance, use a capacitor with low ESR.

Power Supply Bypassing

Selection of a proper power supply bypassing capacitor is critical to obtaining lower noise as well as higher power supply rejection. Larger capacitors may help to increase immunity to the supply noise. However, considering economical design, attaching 10μF electrolytic capacitor or tantalum capacitor with 0.1μF ceramic capacitor as close as possible to the VDD pins are enough to get a good supply noise rejection.

Selection of Input Capacitor

The input capacitors CINN and CINP block the DC voltage also low frequency input signal. Thus, these capacitors act as a high pass filter. When there are DC level differences between input source and the amplifier, these capacitors block DC voltage and make easy connection. However, these capacitors limit the low frequency input signal. Thus to cover the full audio frequency range, the values of these are very important. The input impedance and the capacitance of these capacitors stand for the low frequency characteristics and -3dB frequency is

$$f_L = \frac{1}{2\pi \cdot Zin \cdot C} \quad (2)$$

Where Zin is the input equivalent impedance and C is the capacitance of the input capacitor.
For FAN7033MP, the input has several resistors and these resistors determine the input impedance. In the normal condition, (-) input of the amplifier looks like a voltage source since the negative feedback topology makes (-) input virtually be the AC ground. Thus, resistance between the negative input of the amplifier and input pin is 15kΩ. The resistance toward (+) input is the summation of 15kΩ and 90kΩ. Thus total input impedance is

$$Zin = 15k\Omega \parallel (15k\Omega + 90k\Omega) = 13.125k\Omega \quad (3)$$

Considering f_L=20Hz(the lowest frequency of the audio freqeuncy range), it is possible to get the capacitance value from equation(2) and (3) as follow:

$$Cin = \frac{1}{2\pi \cdot Zin \cdot f_L} = 0.606uF \quad (4)$$

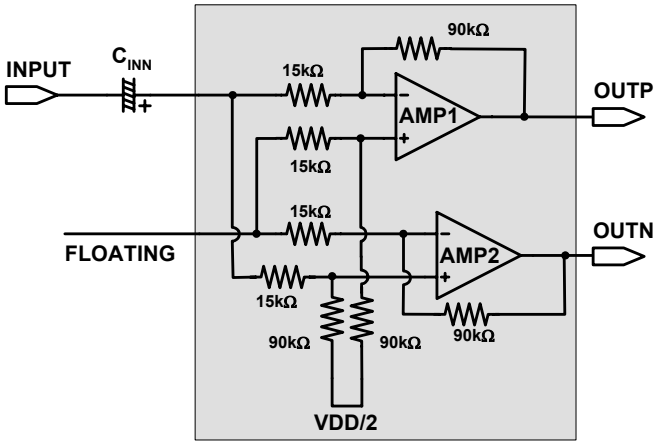
Thus, Cin must be higher than 0.606uF. In the application note, 1uF is chosen by considering input impedance variation during the chip fabrication.
When using a capacitor which has the polarity, customers must carefully connect the capacitor. The input DC level of the FAN7033MP is a half of VDD. Thus, if the DC level of a source is higher than VDD/2, the positive lead of the capacitor must be faced toward the source.

Shutdown Mode

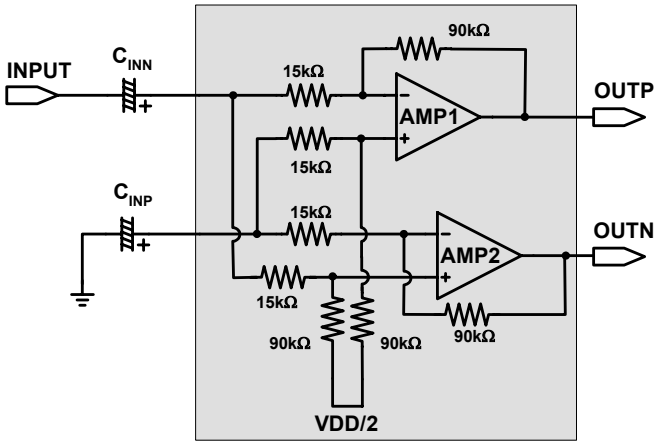
In order to reduce power consumption while not in use, the FAN7033MP contains a shutdown pin to externally turn-off bias circuitry. This shutdown feature turns the amplifier off when a logic low is placed on the shutdown pin. The trigger point between a logic low and logic high level is typically half-supply. It is best to switch between ground and supply to provide maximum device performance. By switching the shutdown pin to VDD , the FAN7033MP supply current draw will be minimized in idle mode. In either case, the shutdown pin should be tied to a definite voltages to avoid unwanted state changes.
In many appplications, a microcontroller or microprocessor output is used to control the shutdown circuitry which provides a quick, smooth transition into shutdown. Another solution is to use a single-pole, single-throw switch in conjunction with an external pull-down resistor. When the switch is closed, the shutdown pin is connected to VDD and enables the amplifier. If the switch is open, then the external pull-down resistor will disable the FAN7033MP. This scheme guarantees that the shutdown pin will not float thus preventing unwanted state changes.

Single-Ended Input

For the case, a source does not provide the fully differential signal, the residual input must be well treated.



Case (A) : Residual Input Pin Floating



Case (B) : AC Coupling to Ground

Case(A) : For this case, input is left alone without any treatment, that is, input pin is floating. Even the pin is floating, the BTL amplifier works and drives load. However, this configuration might cause unwanted noise at the output signal. Furthemore, floated configuration decreases PSRR(Power Supply Rejection Ratio) and increase POP noise.
Case(B) : Case(B) is strongly recommended. This configuration increases PSRR and decreases POP noise as well. Of cource, to get the best performance, CINP must be the same value with CINN.

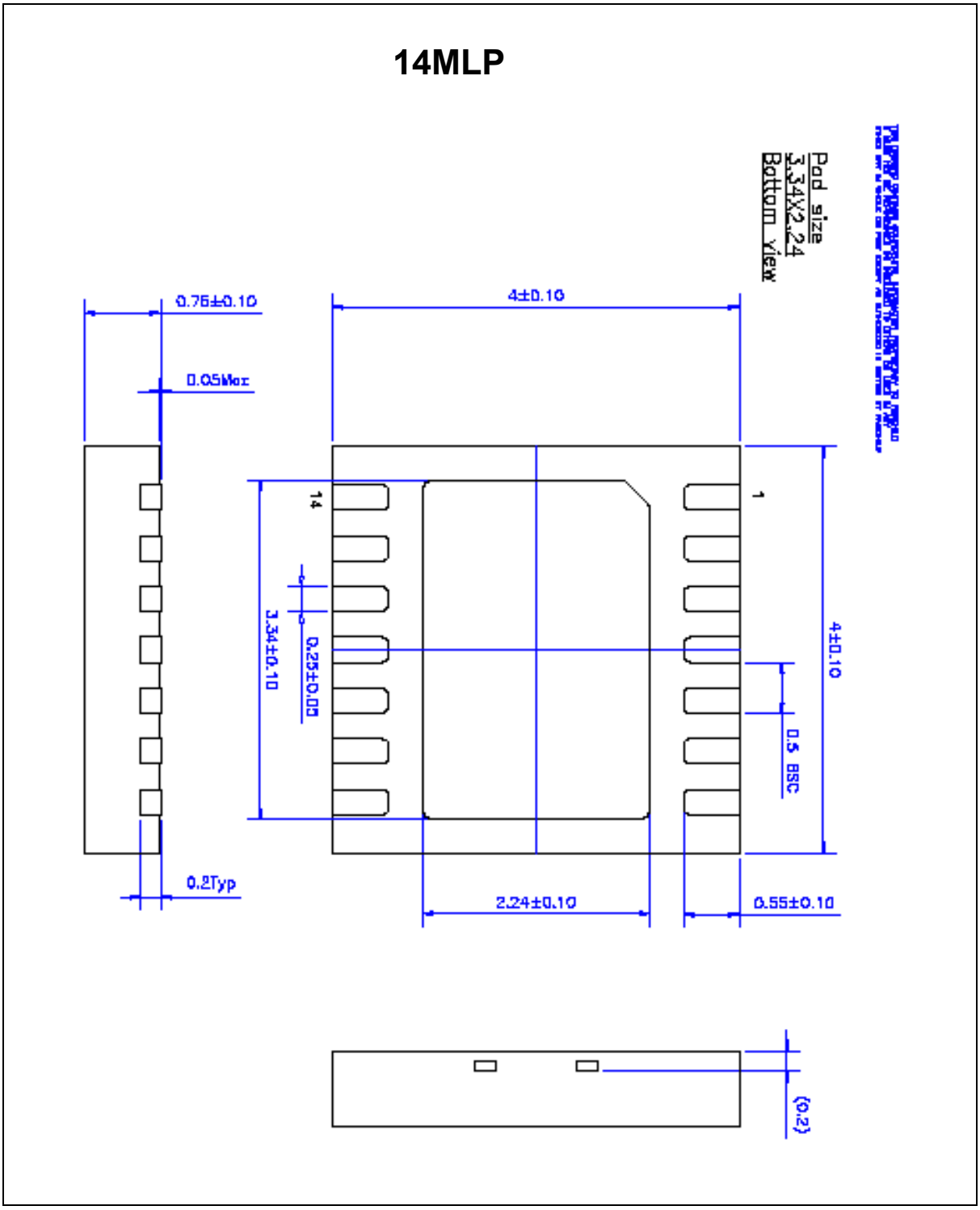
THD+N(Total Harmonic Distortion plus Noise)

THD+N stands for linearity and output noise of the amplifier as well. The FAN7033MP has the circuit for enhancing THD. In spite of that, to get low THD+N, users should follow the recommendation:
(1) Use fully differential input configuration : A fully differential input makes low THD at output. Thus, for a single-ended input case, THD+N slightly increaes.
(2) Do not miss C_{BYP}. C_{BYP} helps to increase PSRR. Thus, using this capacitor, it is possible to increase noise immunity from the supply line.
(3) Do not miss C_{SUP}. Voltage fluctuation in supply line increases THD. Thus, such voltage fluctuation must be reduced to get low THD by connecting this capacitor between all VDD pins and the ground as closely as possible.

Mechanical Dimensions

Package

Dimensions in millimeters



Ordering Information

Device	Package	Operating Temperature
FAN7033MP	14MLP	-40°C ~ +85°C

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