

FAN8033

6-Channel Motor Drive IC

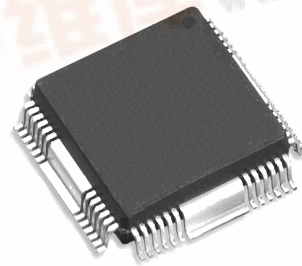
Features

- 4-CH balanced transformerless (BTL) driver
- 2-CH (forward-reverse) control DC motor driver
- Operating supply voltage (4.5V ~ 16V)
- Built-in thermal shut down circuit (TSD)
- Built-in under voltage lockout circuit (UVLO)
- Built-in over voltage protection circuit (OVP)
- Built-in mute circuit (CH1, CH2, CH3 and CH4)
- Built-in normal op-amp
- Built-in 5V regulator with reset

Description

The FAN8033 is a monolithic integrated circuit suitable for a 6-ch motor driver which drives the tracking actuator, focus actuator, sled motor, tray motor, change motor and spindle motor of the CDP/CAR-CD systems.

48-QFPH-1414



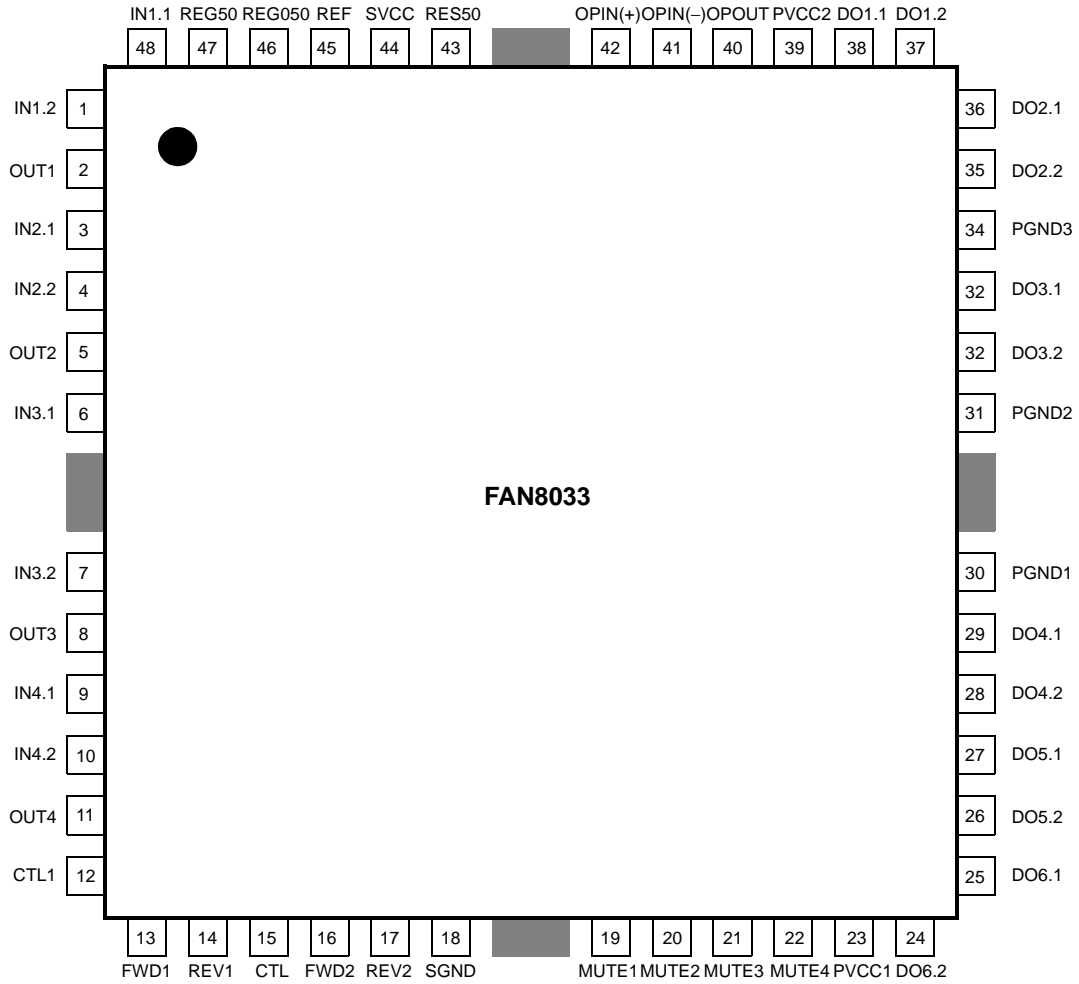
Typical Applications

- Compact disk player (CDP) with tray and changer
- Video compact disk player (VCD) with tray and changer
- Automotive compact disk player (CDP) with tray and changer
- Other compact disk media

Ordering Information

| Device | Package | Operating Temp. |
|---------|--------------|-----------------|
| FAN8033 | 48-QFPH-1414 | -35°C ~ +85°C |

Pin Assignments



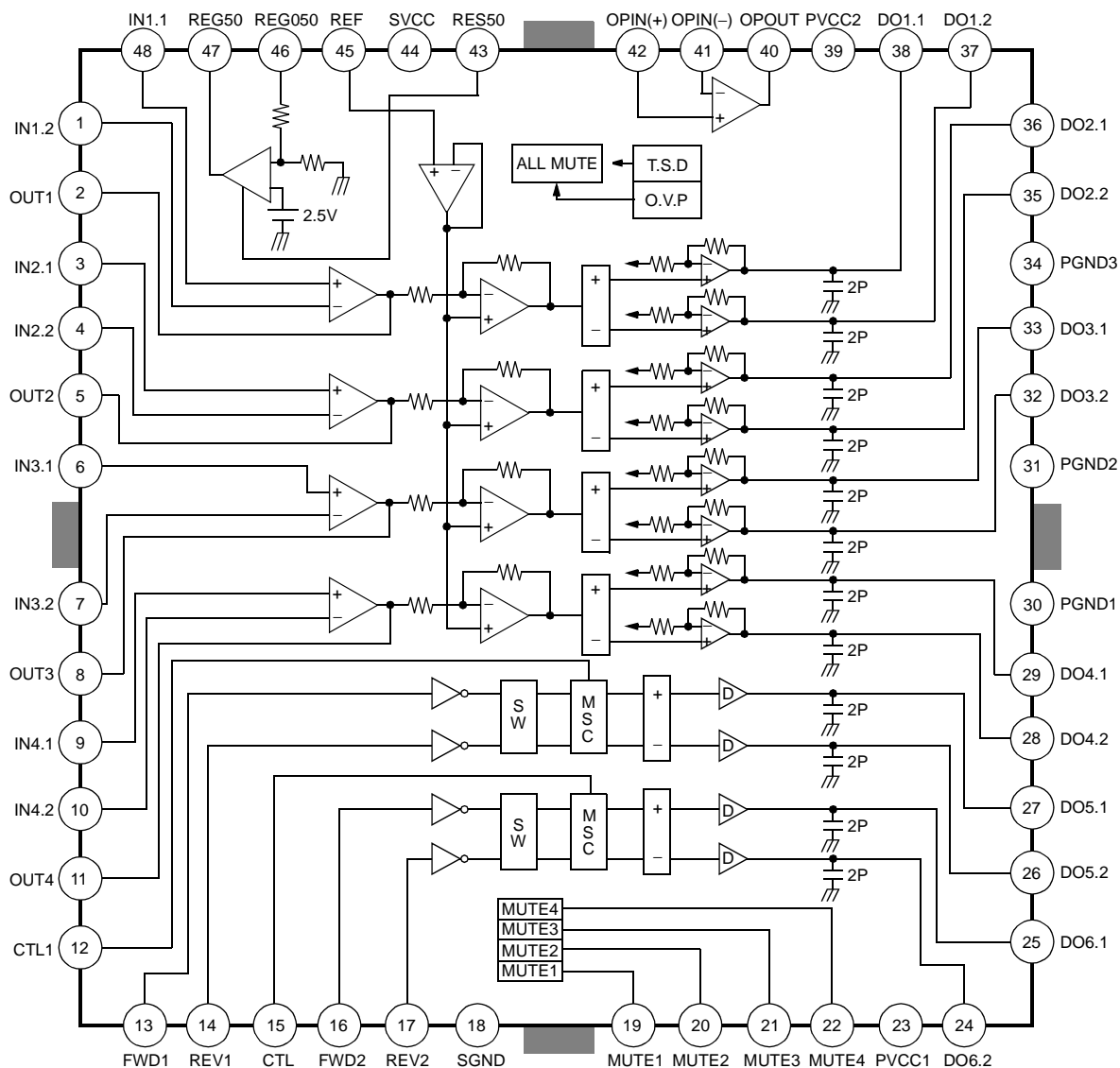
Pin Definitions

| Pin Number | Pin Name | I/O | Pin Function Description |
|------------|----------|-----|---|
| 1 | IN1.2 | I | CH 1 op-amp input (-) |
| 2 | OUT1 | O | CH 1 op-amp output |
| 3 | IN2.1 | I | CH 2 op-amp input (+) |
| 4 | IN2.2 | I | CH 2 op-amp input (-) |
| 5 | OUT2 | O | CH 2 op-amp output |
| 6 | IN3.1 | I | CH 3 op-amp input (+) |
| 7 | IN3.2 | I | CH 3 op-amp input (-) |
| 8 | OUT3 | O | CH 3 op-amp output |
| 9 | IN4.1 | I | CH 4 op-amp input (+) |
| 10 | IN4.2 | I | CH 4 op-amp input (-) |
| 11 | OUT4 | O | CH 4 op-amp output |
| 12 | CTL1 | I | CH 5 motor speed control |
| 13 | FWD1 | I | CH 5 forward input |
| 14 | REW1 | I | CH 5 reverse input |
| 15 | CTL2 | I | CH 6 motor speed control |
| 16 | FWD2 | I | CH 6 forward input |
| 17 | REW2 | I | CH 6 reverse input |
| 18 | SGND | - | Signal ground |
| 19 | MUTE1 | I | CH 1 mute |
| 20 | MUTE2 | I | CH 2 mute |
| 21 | MUTE3 | I | CH 3 mute |
| 22 | MUTE4 | I | CH 4 mute |
| 23 | PVCC1 | - | Power supply voltage (For CH 5, CH 6) |
| 24 | DO6.2 | O | CH 6 drive output |
| 25 | DO6.1 | O | CH 6 drive output |
| 26 | DO5.2 | O | CH 5 drive output |
| 27 | DO5.1 | O | CH 5 drive output |
| 28 | DO4.2 | O | CH 4 drive output |
| 29 | DO4.1 | O | CH 4 drive output |
| 30 | PGND | - | Power ground |
| 31 | PGND | - | Power ground |
| 32 | DO3.2 | O | CH 3 drive output |
| 33 | DO3.1 | O | CH 3 drive output |
| 34 | PGND | - | Power ground |
| 35 | DO2.2 | O | CH 2 drive output |
| 36 | DO2.1 | O | CH 2 drive output |
| 37 | DO1.2 | O | CH 1 drive output |
| 38 | DO1.1 | O | CH 1 drive output |
| 39 | PVCC2 | - | Power supply voltage (For CH 1, CH 2, CH 3, CH 4) |
| 40 | OPOUT | O | Opamp output |

Pin Definitions (Continued)

| Pin Number | Pin Name | I/O | Pin Function Description |
|------------|----------|-----|--------------------------|
| 41 | OPIN(-) | I | Opamp input (-) |
| 42 | OPIN(+) | I | Opamp input (+) |
| 43 | RES50 | I | Regulator 5V reset |
| 44 | SVCC | - | Signal supply voltage |
| 45 | REF | I | Bias voltage input |
| 46 | REG050 | O | Regulator 5V output |
| 47 | REG50 | O | Regulator output |
| 48 | IN1.1 | I | CH 1 opamp input (+) |

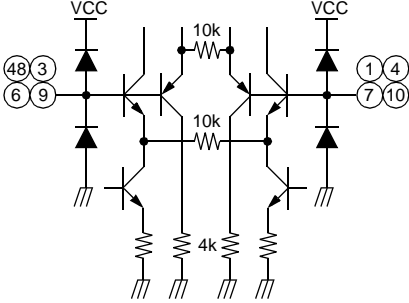
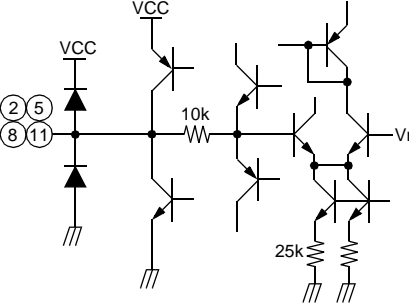
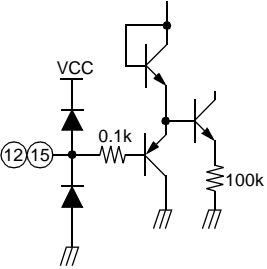
Internal Block Diagram



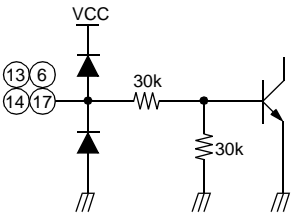
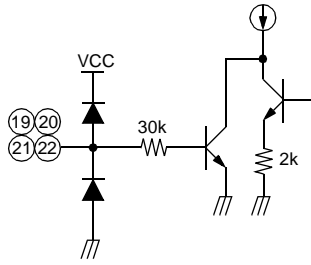
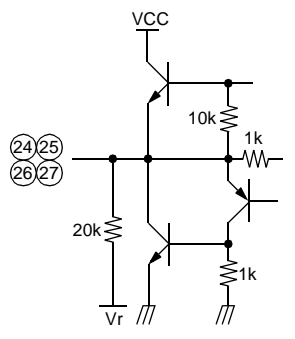
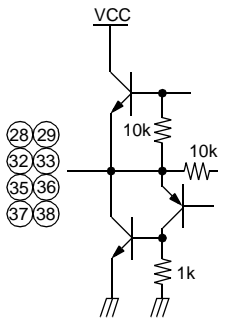
Notes:

1. SW = Logic switch
2. MSC = Motor speed control
3. D = Output driver

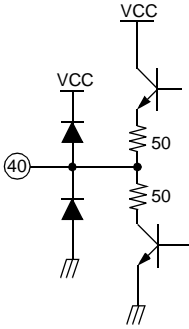
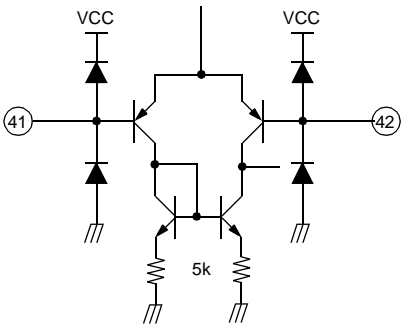
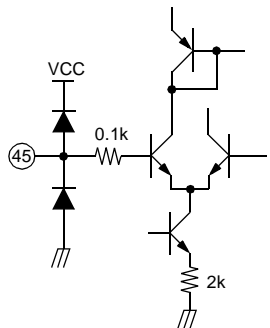
Equivalent Circuit

| Description | Pin No. | Internal circuit |
|-------------------------------|----------------------------|--|
| Input OPIN (+) OPIN (-) | 48, 3, 6, 9 1, 4, 7, 10 |  |
| Input opout | 2, 5, 8, 11 |  |
| CTL | 12, 15 |  |

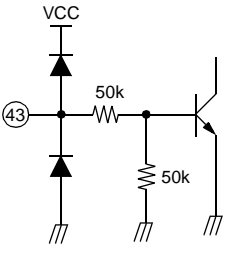
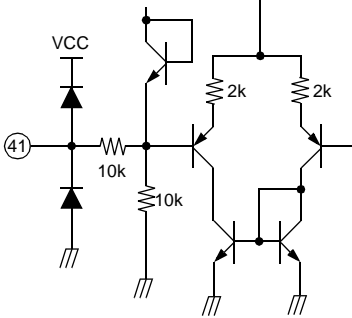
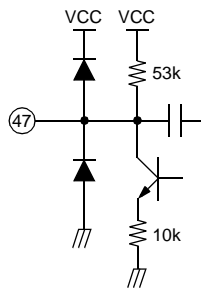
Equivalent Circuit (Continued)

| Description | Pin No. | Internal circuit |
|---------------------------------------|--------------------------------------|--|
| Logic drive FWD input REV input | 13, 16 14, 17 |  |
| CH mute | 19, 20 21, 22 |  |
| Logic drive output | 24, 25 26, 27 |  |
| 4-CH drive output | 28, 29 32, 33 35, 36 37, 38 |  |

Equivalent Circuit (Continued)

| Description | Pin No. | Internal circuit |
|---------------------------|----------|--|
| Normal opout | 40 |  |
| Normal OPIN(+) OPIN(-) | 42 41 |  |
| Ref | 45 |  |

Equivalent Circuit (Continued)

| Description | Pin No. | Internal circuit |
|-------------|---------|--|
| RES50 | 43 |  |
| REG050 | 46 |  |
| REG50 | 47 |  |

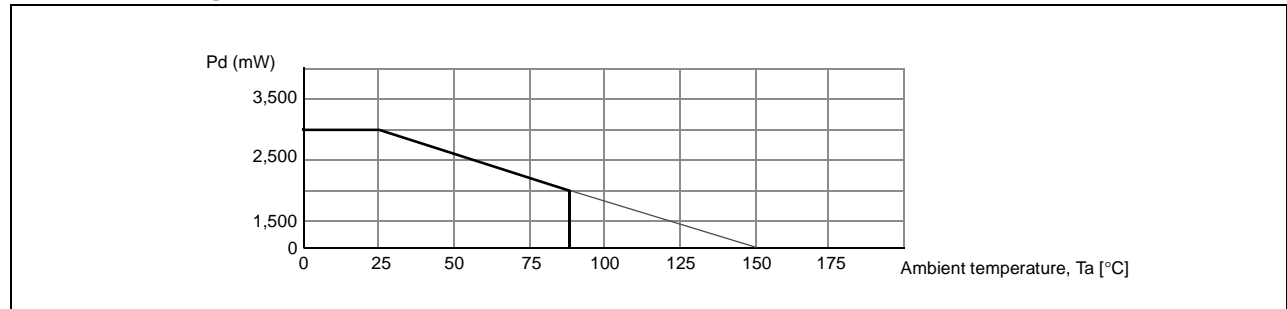
Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Value | Unit |
|------------------------|--------|-------------------|------|
| Maximum supply voltage | VCC | 18 | V |
| Power dissipation | PD | 3 ^{note} | W |
| Operating temperature | TOPR | -35 ~ +85 | °C |
| Storage temperature | TSTG | -55 ~ +150 | °C |
| Maximum output current | IOMAX | 1 | A |

NOTE:

1. When mounted on 70mm × 70mm × 1.6mm PCB.
2. Power dissipation reduces 16mW / °C for using above Ta=25°C.
3. Do not exceed Pd and SOA.

Power Dissipation Curve



Recommended Operating Conditions (Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--------------------------|--------|------|------|------|------|
| Operating supply voltage | VCC | 4.5 | - | 16 | V |

Electrical Characteristics

(SVCC=PVCC1=PVCC2=8V, Ta=25°C, unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|-----------------------------|-----------|------------------------------|------|------|------|-------|
| Quiescent circuit current | ICC | under no-load | 9 | 12 | 16 | mA |
| All mute on current | IMUTE ALL | Pin 45=GND | - | 6 | 10 | mA |
| All mute on voltage | VMON ALL | Pin 45=Variation | - | - | 0.5 | V |
| All mute off voltage | VMOFF ALL | Pin 45=Variation | 2 | - | - | V |
| CH mute on voltage | VMON CH | Pin 19, 20, 21, 22=Variation | 2 | - | - | V |
| CH mute off voltage | VMOFF CH | Pin 19, 20, 21, 22=Variation | - | - | 0.5 | V |
| DRIVER PART (RL=8Ω) | | | | | | |
| Input offset voltage | VIO | - | -20 | - | +20 | mV |
| Output offset voltage | VOO | VIN=2.5V | -50 | - | +50 | mV |
| Maximum output voltage 1 | VOM1 | VCC=8V, RL=8Ω | 4.0 | 5.5 | - | V |
| Maximum output voltage 2 | VOM2 | VCC=13V, RL=24Ω | 7 | 9 | - | V |
| Closed-loop voltage gain | AVF | VIN=0.1VRMS | 9 | 10.5 | 12 | dB |
| Ripple rejection ratio | RR | VIN=0.1VRMS, f=120kHz | - | 50 | - | dB |
| Slew rate | SR | Square, Vout=2Vp-p, f=120kHz | - | 0.8 | - | V/μs |
| NORMAL OPAMP PART | | | | | | |
| Input offset voltage | VOF1 | - | -10 | - | +10 | mV |
| Input bias current | IB1 | - | - | - | 300 | nA |
| High level output voltage | VOH1 | RL=50Ω | 6 | 6.8 | - | V |
| Low level output voltage | VOL1 | RL=50Ω | - | 1.0 | 1.8 | V |
| Output sink current | ISINK1 | VIN=-75dB, f=1kHz | 10 | 40 | - | mA |
| Output source current | ISOURCE1 | VIN=-20dB, f=120kHz | 10 | 40 | - | mA |
| Open loop voltage gain | GVO1 | Square, Vout=2Vp-p, f=120kHz | - | 75 | - | dB |
| Ripple rejection ratio | RR1 | VIN=-20dB, f=1kHz | - | 65 | - | dB |
| Slew rate | SR1 | - | - | 1 | - | V/μs |
| Common mode rejection ratio | CMRR1 | - | - | 80 | - | dB |

Electrical Characteristics (Continued)

(SVCC=PVCC1=PVCC2=8V, Ta=25°C, unless otherwise specified)

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|---|----------------------|---|------|------|------|-------|
| INPUT OPAMP PART | | | | | | |
| Input offset voltage | V _{OF2} | - | -10 | - | +10 | mV |
| Input bias current | I _{B2} | - | - | - | 400 | nA |
| High level output voltage | V _{OH2} | - | 7 | 7.7 | - | V |
| Low level output voltage | V _{OL2} | - | - | 0.2 | 0.5 | V |
| Output sink current | I _{SINK2} | - | 500 | 800 | - | μA |
| Output source current | I _{SOURCE2} | - | 500 | 800 | - | μA |
| Open loop voltage gain | G _{VO2} | V _{IN} =-75dB, f=1kHz | - | 80 | - | dB |
| Slew rate | SR ₂ | Square, V _{out} =2Vp-p, f=120kHz | - | 1 | - | V/μs |
| Common mode rejection ratio | CMRR ₂ | V _{IN} =-20dB, f=1kHz | - | 80 | - | dB |
| 5V REGULATOR PART | | | | | | |
| Regulator output voltage | V _{reg} | I _L =100mA | 4.75 | 5 | 5.25 | V |
| Load regulation | ΔV _{R1} | I _L =0→200mA | -40 | 0 | +10 | mV |
| Line regulation | ΔV _{CC} | I _L =200mA, V _{CC} =6V→9V | -20 | 0 | +30 | mV |
| Reset on voltage | Reson | - | - | - | 0.5 | V |
| Reset off voltage | Resoff | - | 2 | - | - | V |
| TRAY, CHANGER DRIVER PART (R _L =45Ω) | | | | | | |
| Input high level voltage | V _{IH} | - | 2 | - | - | V |
| Input low level voltage | V _{IL} | - | - | - | 0.5 | V |
| Output voltage 1 | V _{O1} | V _{CC} =8V, V _{CTL} =3.5V | 5.2 | 6.0 | 6.8 | V |
| Output voltage 2 | V _{O2} | V _{CC} =13V, V _{CTL} =4.5V | 7.5 | 8.5 | 9.5 | V |
| Output load regulation | ΔV _{R1} | - | - | 300 | 700 | mV |
| Output offset voltage 1 | V _{OO1} | V _{IN} =5V, 5V | -10 | - | +10 | mV |
| Output offset voltage 2 | V _{OO2} | V _{IN} =0V, 0V | -10 | - | +10 | mV |

Application Information

1. REFERENCE INPUT

Pin 45 (REF) can use the reference Input pin .

- Reference input
In the case of the reference input pin, you must keep the applied voltage range between 2[V] and 6.5[V] at $V_{CC} = 8[V]$.

2. SEPARATED CHANNEL MUTE FUNCTION

These pins are used for individual channel mute operation.

- When the mute pins (pin19, 20, 21 and 22) are high level, the mute circuits are activated so that the output circuit is muted.
- When the voltage of the mute pins (pin19, 20, 21 and 22) are low level, the mute circuit is stopped and output circuits operate normally.
- If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuits are muted.
 - Mute 1 (pin 19)-CH1 mute control input pin.
 - Mute 2 (pin 20)-CH2 mute control input pin.
 - Mute 3 (pin 21)-CH3 mute control input pin.
 - Mute 4 (pin 22)-CH4 mute control input pin.

3. PROTECTION FUNCTION

- Thermal shutdown (TSD)
If the chip temperature rises above 175°C, then the thermal shutdown (TSD) circuit is activated and the output circuit is will be mute. The TSD circuit is temperature hysteresis 25°C.
- Under voltage lockout (UVLO) and over voltage protection (OVP)
It is designed to mute-operate the internal bias by the function of UVLO and OVP, when the power supply voltage falls below 3.5[V] or above 20[V].

4. REGULATOR & RESET FUNCTION

The regulator and reset circuits are as illustrated in Figure 1.
where $R1=R2$.

- The external circuit is composed of the transistor, KSB772 and a capacitor, about $33[\mu\text{F}]$. The capacitor is used as a ripple eliminator and should have good temperature characteristics.
- The regulator output voltage (pin 46) is decided as follows.
 $V_{\text{out}} = 2 \times 2.5 = 5[\text{V}]$ (where $R1 = R2$)
- When the voltage of pin 43 (V_{reset}) is at $5[\text{V}]$, the regulator output voltage (pin 46) because $5[\text{V}]$. If the voltage of pin 43 is $0[\text{V}]$, the output voltage of pin 46 because $0[\text{V}]$.

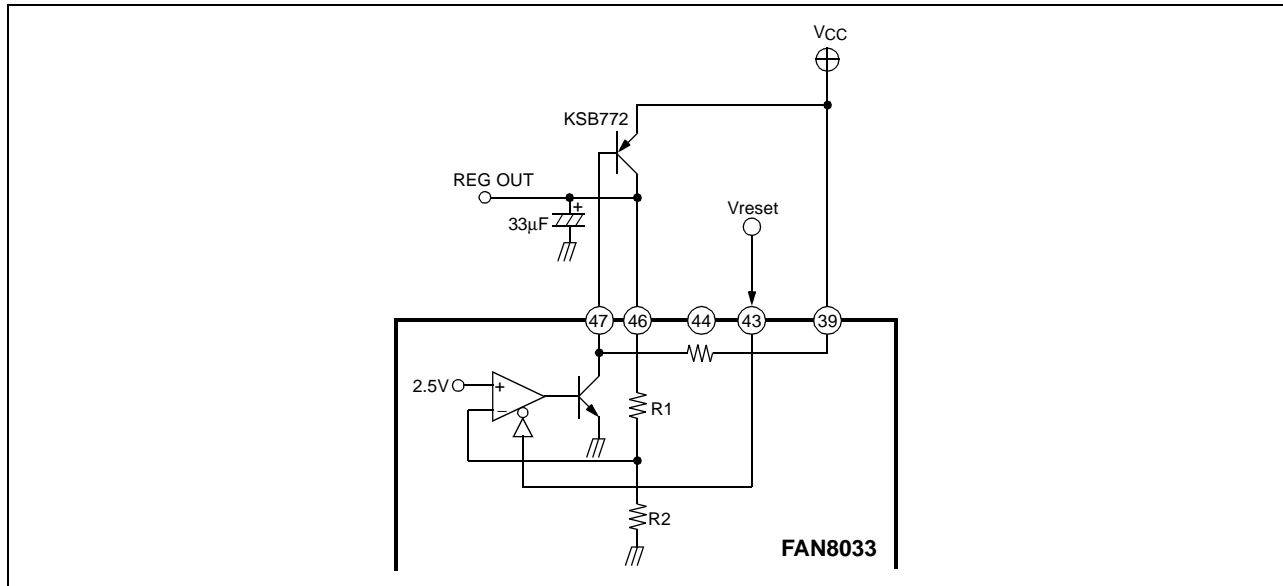
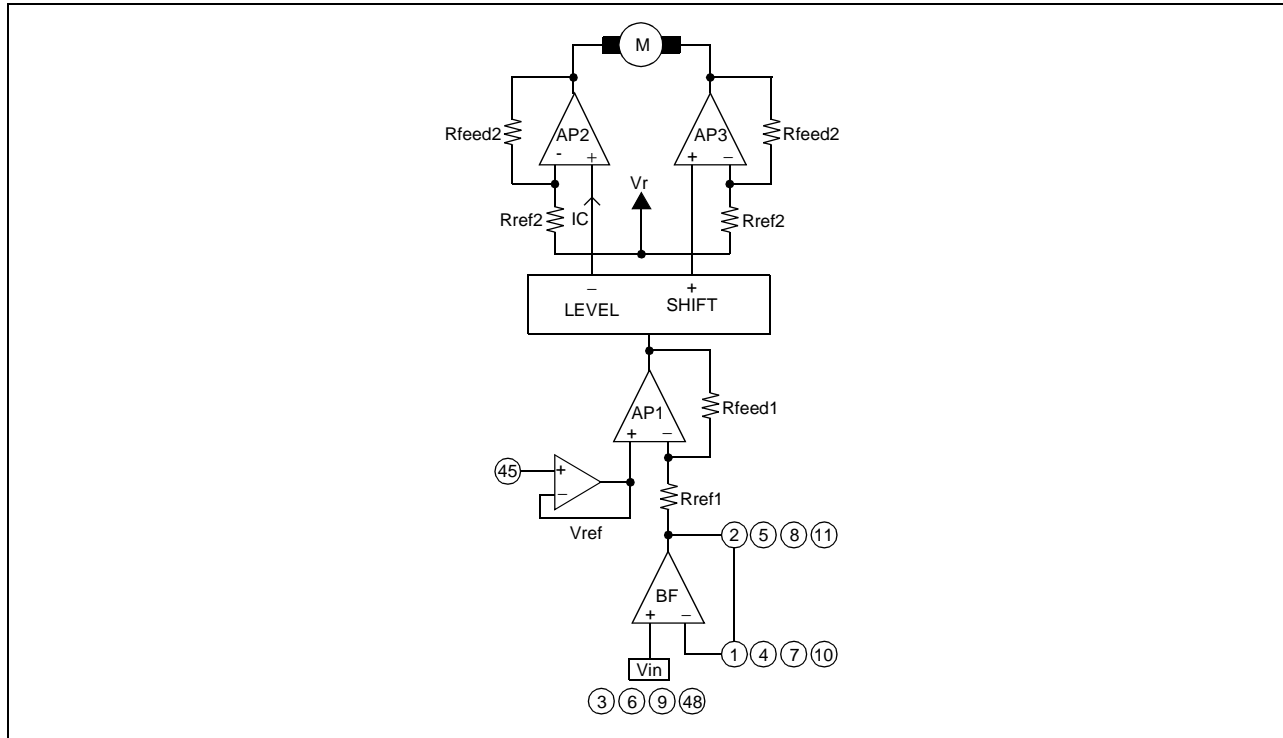


Figure 1. Regulator circuit

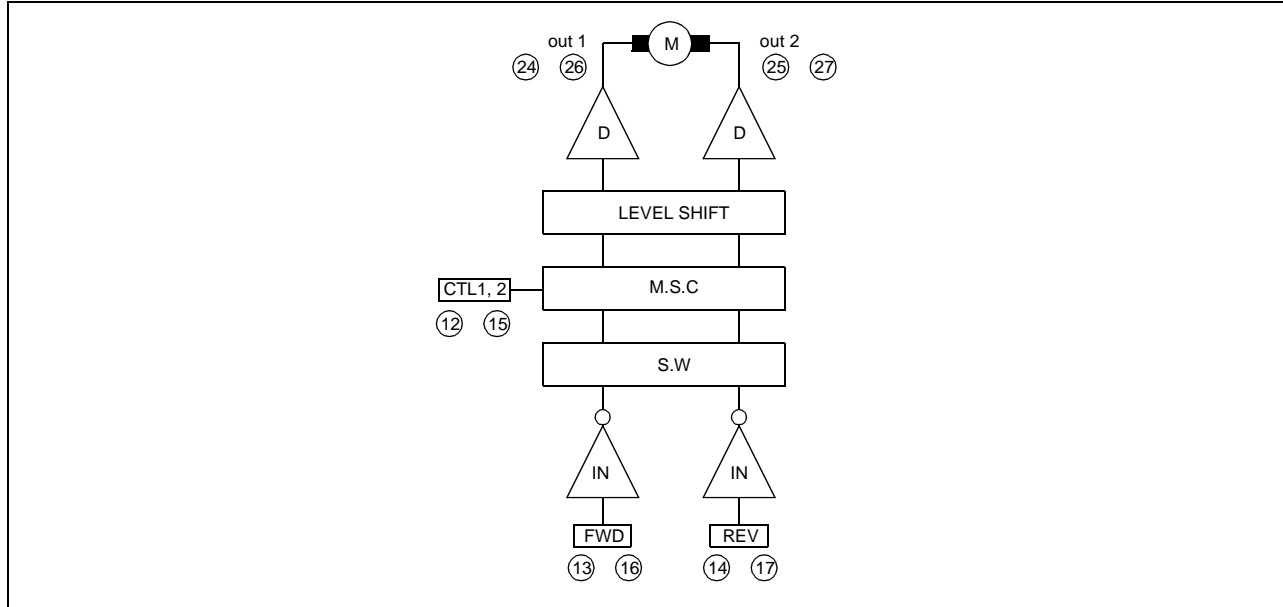
5. FOCUS, TRACKING ACTUATOR, SPINDLE, SLED MOTOR DRIVE PART



- The voltage, V_{ref} is the reference voltage given by the external bias voltage of the pin 45.
- The input signal (V_{in}) through pins 3, 6, 9 and 48 is amplified one times ($R_{ref1} = R_{feed1}$) by the AP1 and then fed to the level shift.
- The level shift produces the current due to the difference between the input signal and the arbitrary reference signal. The current produced as $+\Delta I$ and $-\Delta I$ are fed into the output amplifier, where output amplifier (AP2, 3) gain is two times (all $R_{ref2} = R_{feed2}$).
- If you desire to change the gain, the input buffer amplifier (BF) can be used.
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage V_r is expressed as below;

$$V_r = \frac{V_{CC} - V_{BE}}{2} [V]$$

6. TRAY, CHANGE MOTOR DRIVE PART



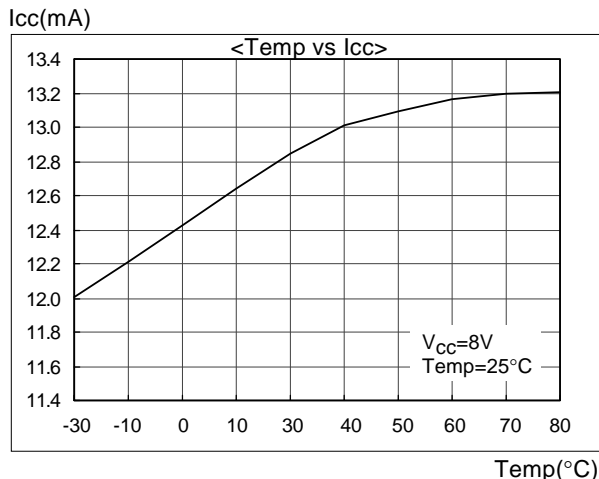
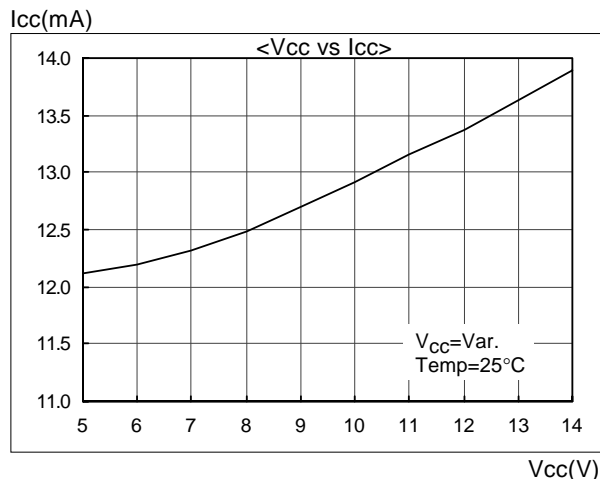
- Rotational direction control
The forward and reverse rotational direction is controlled by FWD (pin 13, 16) and REV (pin 14, 17) input conditions are as follows.

| INPUT | | OUTPUT | | |
|-------|-----|--------|-------|---------|
| FWD | REV | OUT 1 | OUT 2 | State |
| H | H | Vr | Vr | Brake |
| H | L | H | L | Forward |
| L | H | L | H | Reverse |
| L | L | Vr | Vr | Brake |

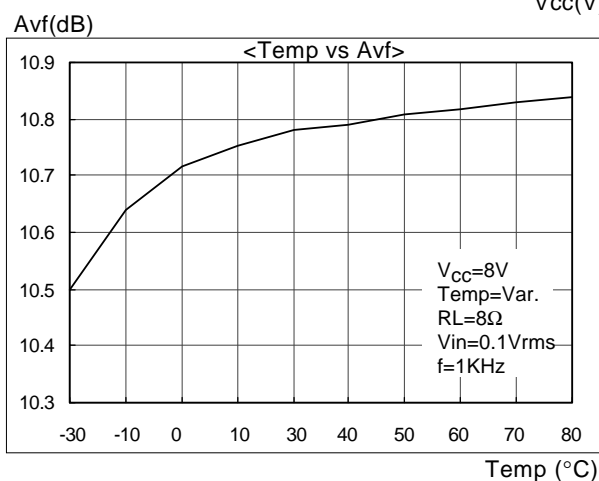
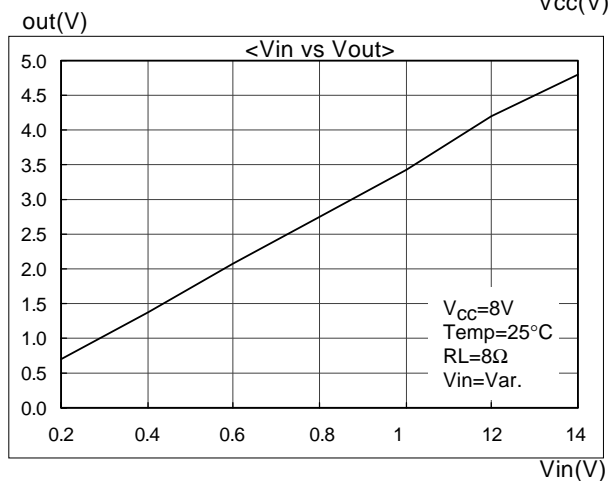
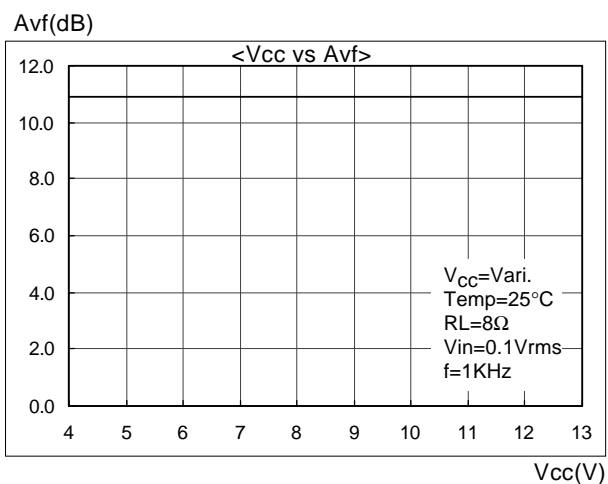
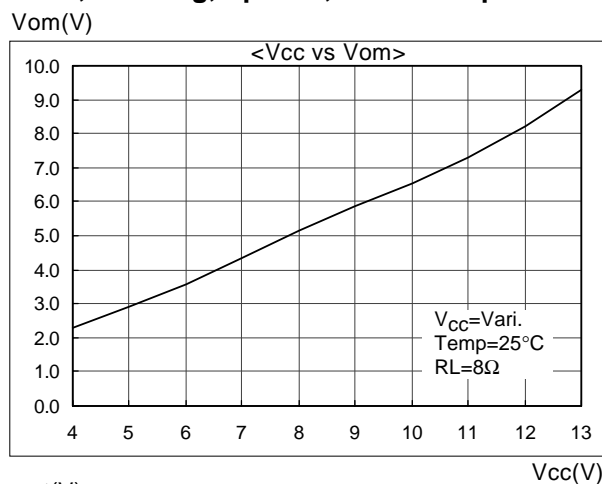
- where Vr is $(V_{cc} - V_{be}) / 2 = 3.65V$ (at $V_{cc}=8V$)
- where Out1 pins are pins 24 and 26, and out2 pins aer pins 25 and 27
- Motor speed control
 - The almost maximum torque is obtained when it is used with the pins 12 and 15 (CTL1, 2) open.
 - If the torque of the motor is too low, then the applied voltage at pins 12 and 15 (CTL1, 2) are 0[V].
 - When motor speed controlled, the applied voltage of the pins 12 and 15 (CTL1, 2) is between 0 and 4V.
 - Also, if the speed control is constant, the applied voltage of the pins 12 and 15 (CTL1, 2) is between 4 and 5V.
 - This IC's applied maximum voltage is 6V when VCC is 8V.
 - You must not use the applied CTL1, 2 voltage above 5.8V when VCC is 8V, and 3V when VCC is 5V.

Typical Performance Characteristics

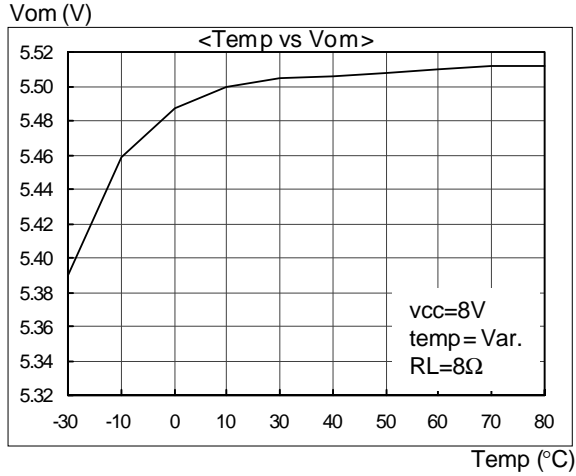
Total circuit



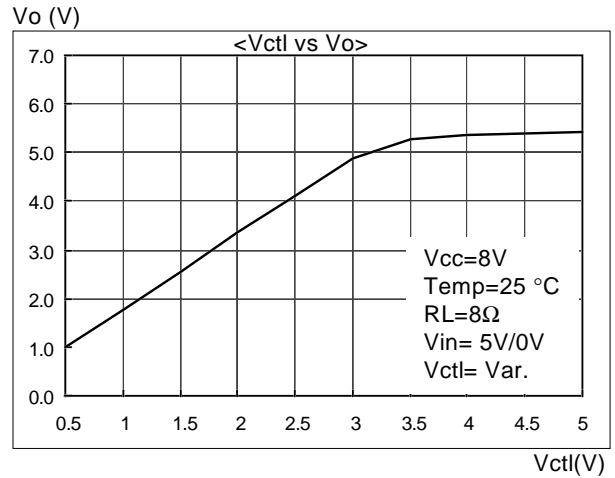
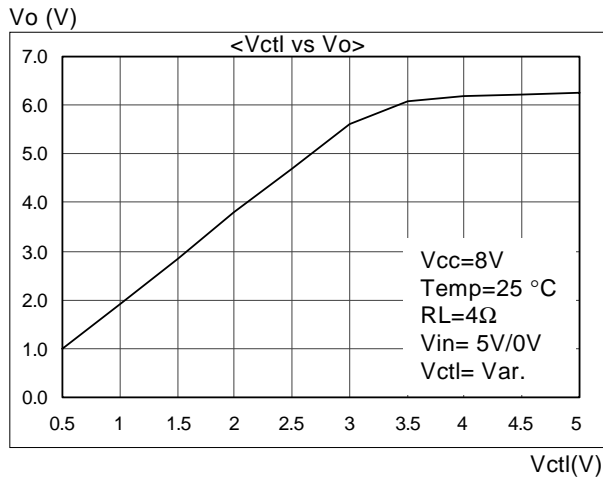
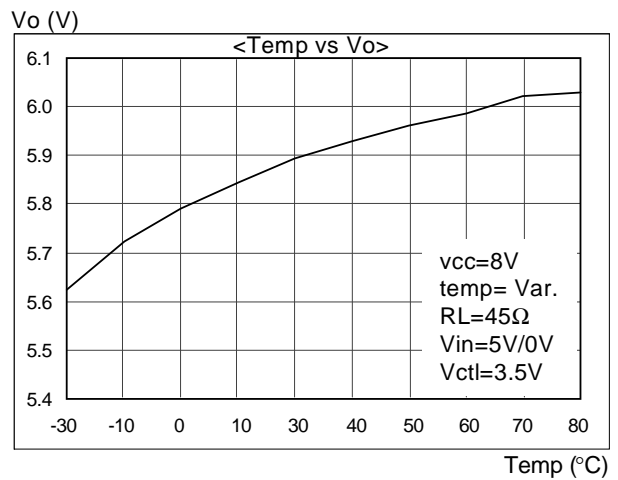
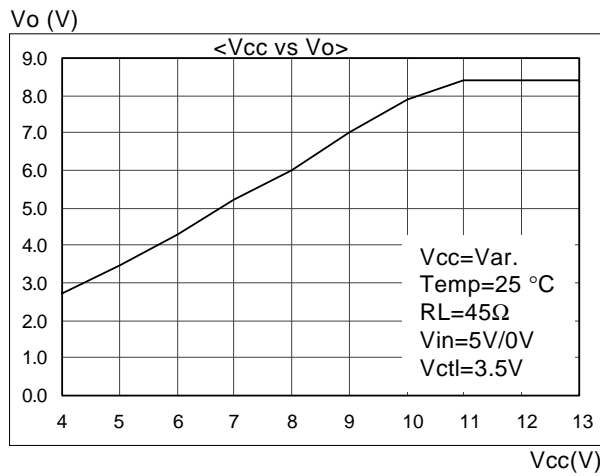
Focus, Tracking, Spindle, Sled drive part



Typical Performance Characteristics (Continued)



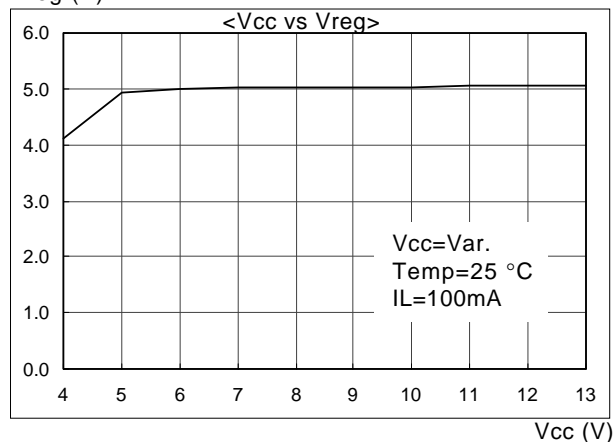
Tray, Change drive part



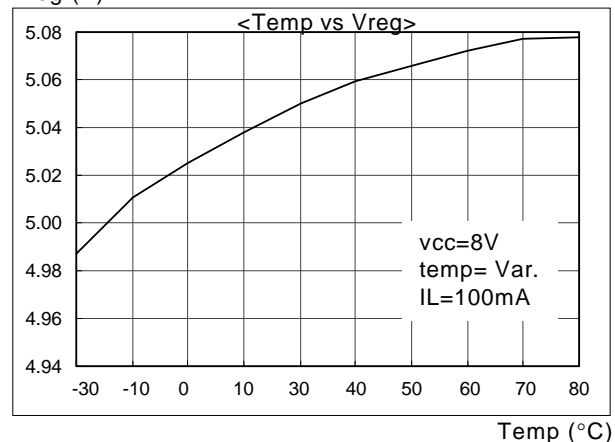
Typical Performance Characteristics (Continued)

Regulator part

Vreg (V)

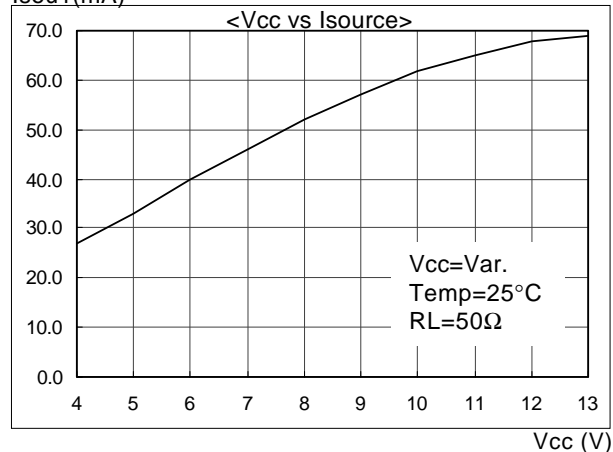


Vreg (V)

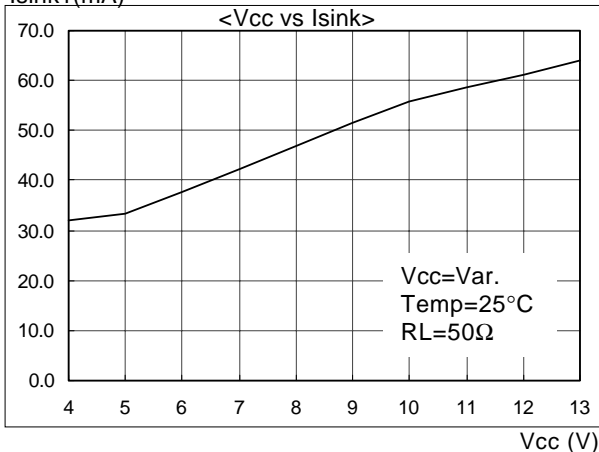


Normal op amp part

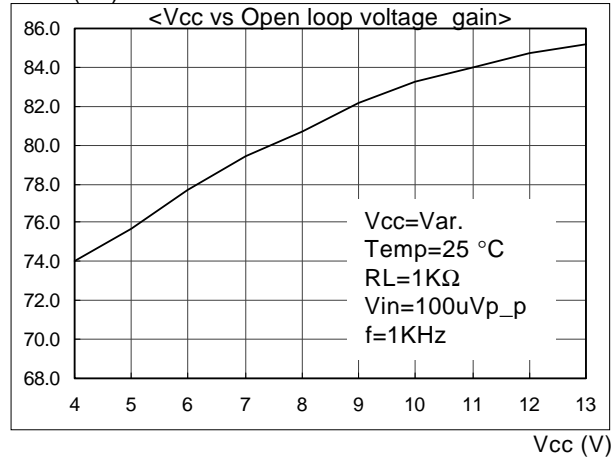
Isou1 (mA)



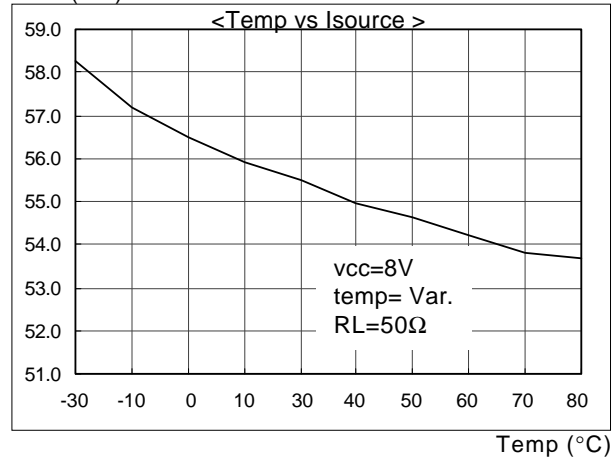
Isink1 (mA)



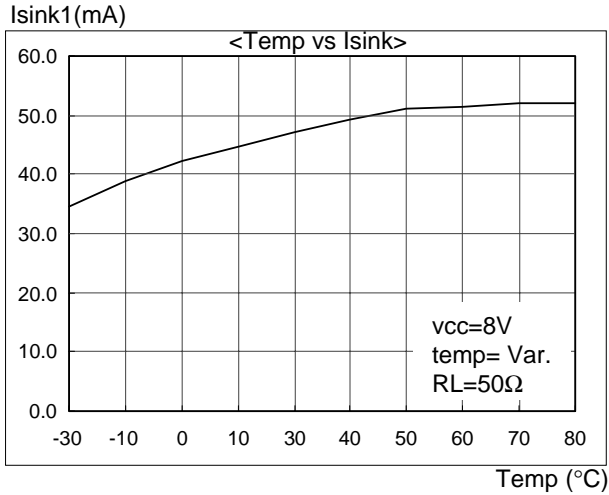
GVo1 (dB)



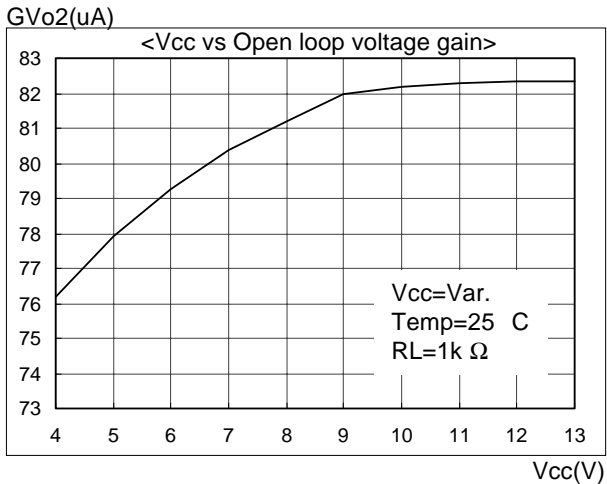
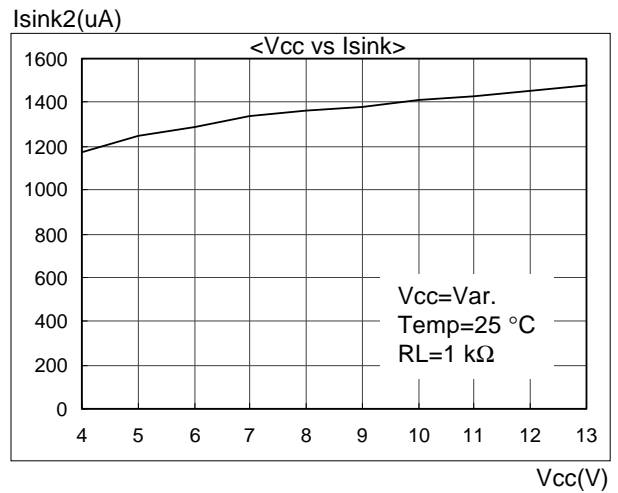
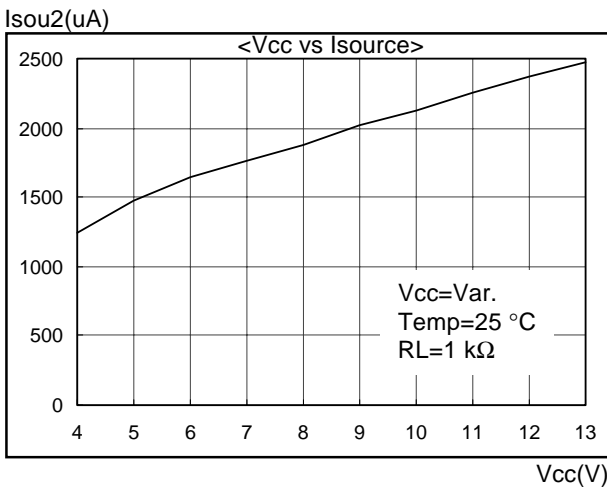
Isou1 (mA)



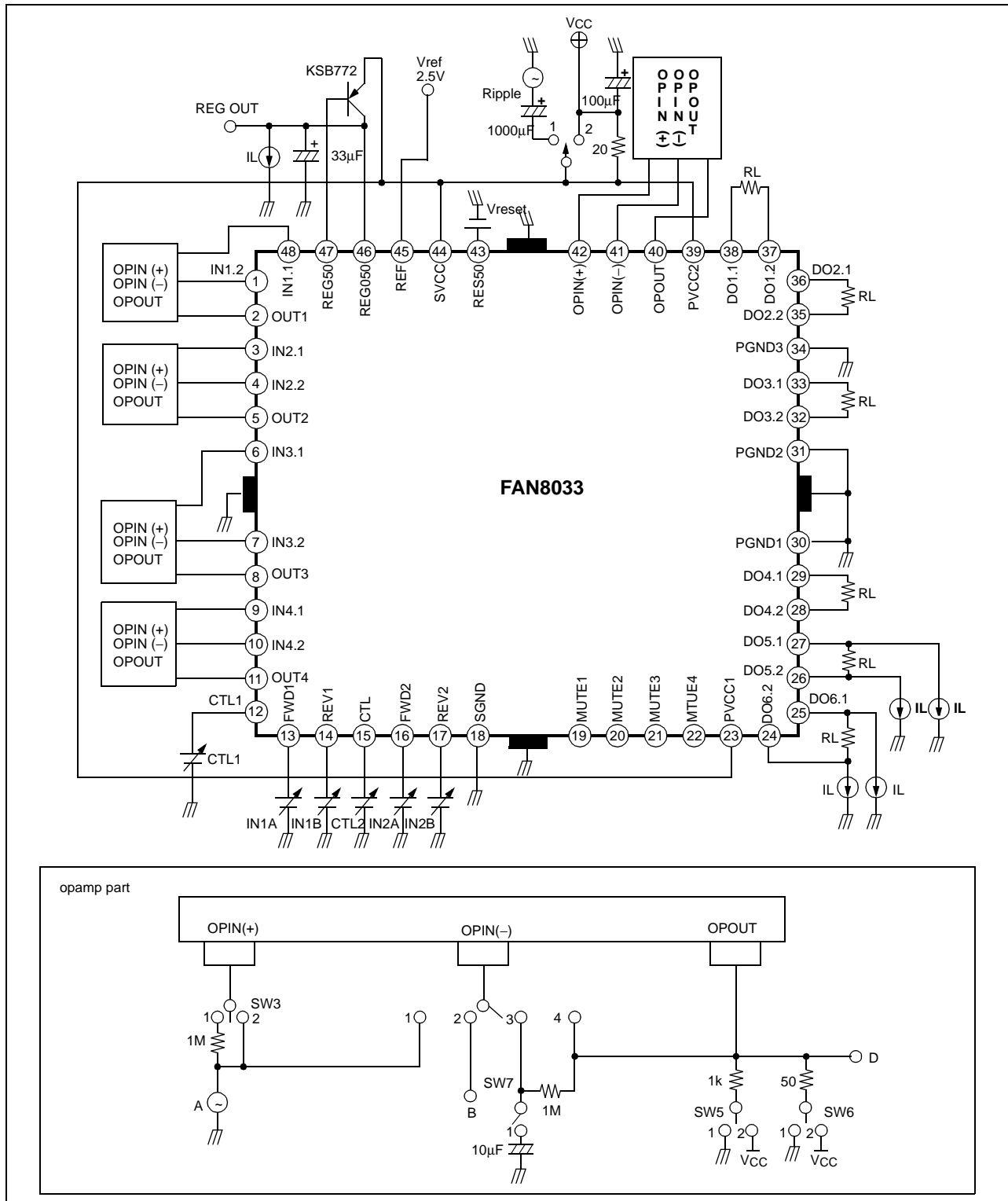
Typical Performance Characteristics (Continued)



Input op amp part

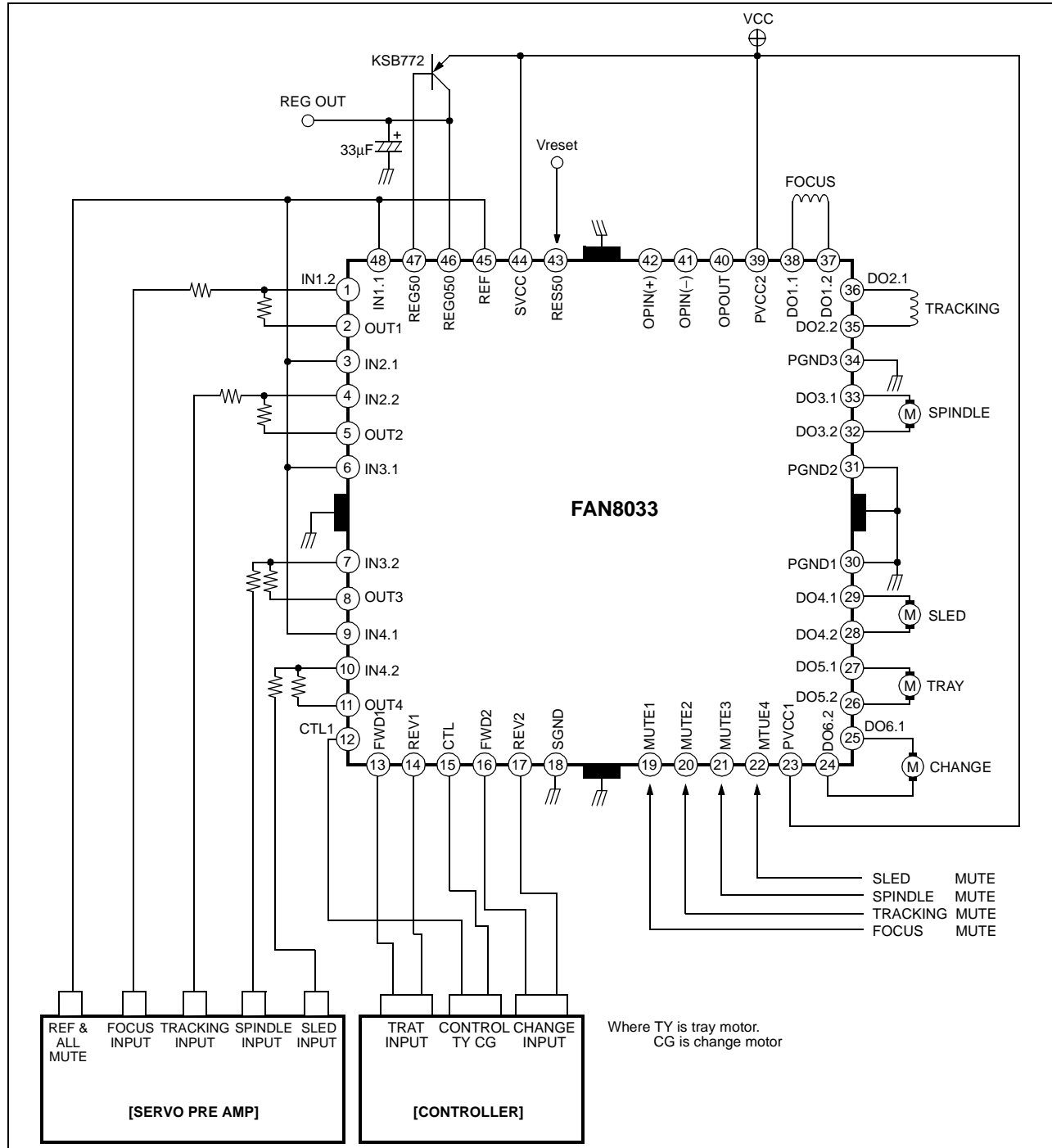


Test Circuits



Application Circuits 1

Voltage Mode Control

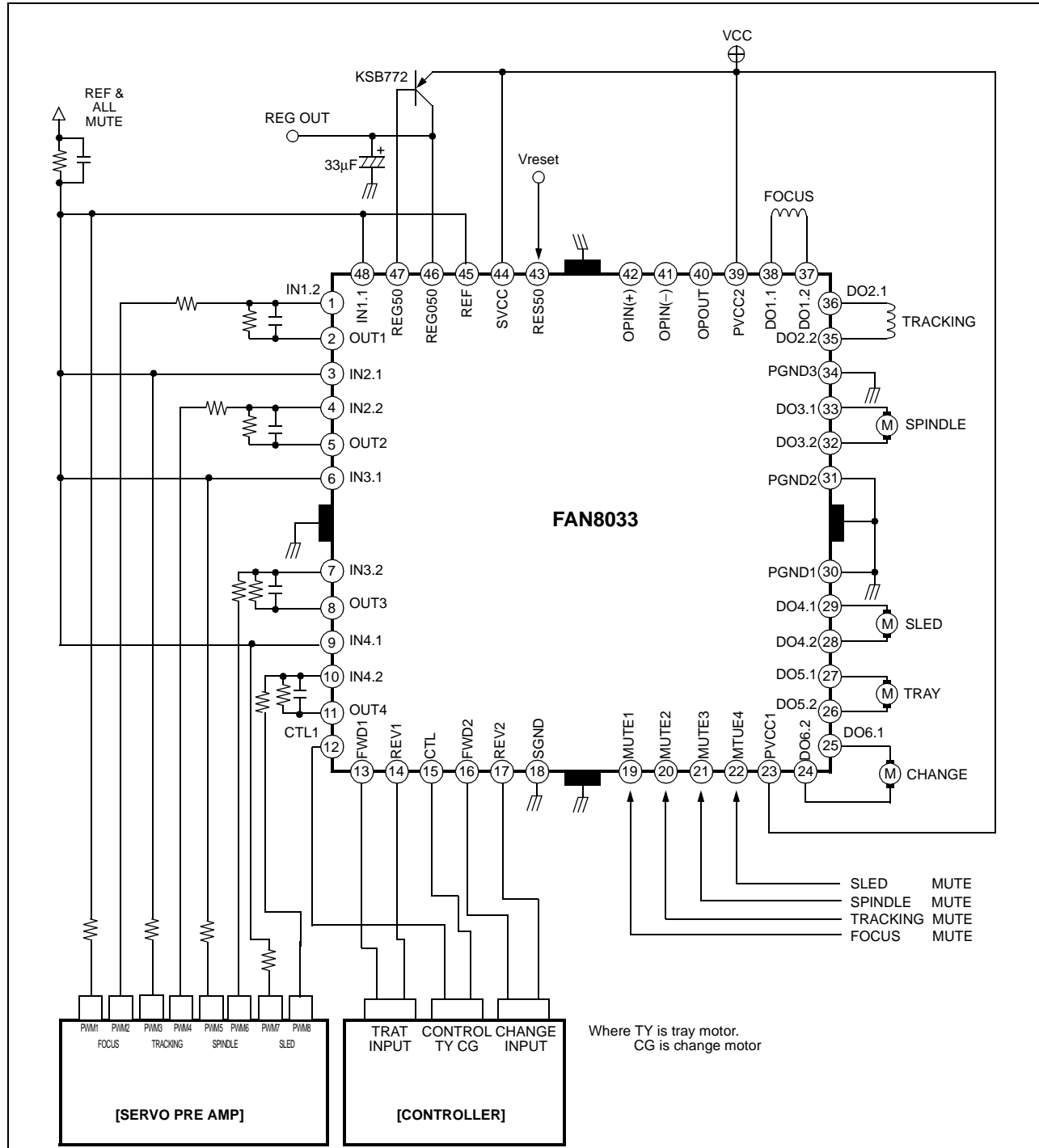


Notes:

Radiation pin is connected to the internal GND of the package.
Connect the pin to the external GND.

Application Circuits 2 (Continued)

Differential Mode Control



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