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FAN8042

5-CH Motor Driver

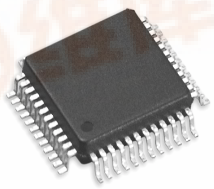
FAN8042 Features

- 4-CH balanced transformerless (BTL) driver
- 1-CH (forward reverse) control DC motor driver
- Operating supply voltage (4.5 V ~ 13.2 V)
- Built in thermal shut down circuit (TSD)
- Built in channel mute circuit
- Built in power save mode circuit
- Built in TSD monitor circuit
- Built in 2-OP AMPs

Description

The FAN8042 is a monolithic integrated circuit suitable for a 5-CH motor driver which drives the tracking actuator, focus actuator, sled motor, spindle motor, and tray motor of the CDP/CAR-CD/DVDP systems.

48-QFP-1010E



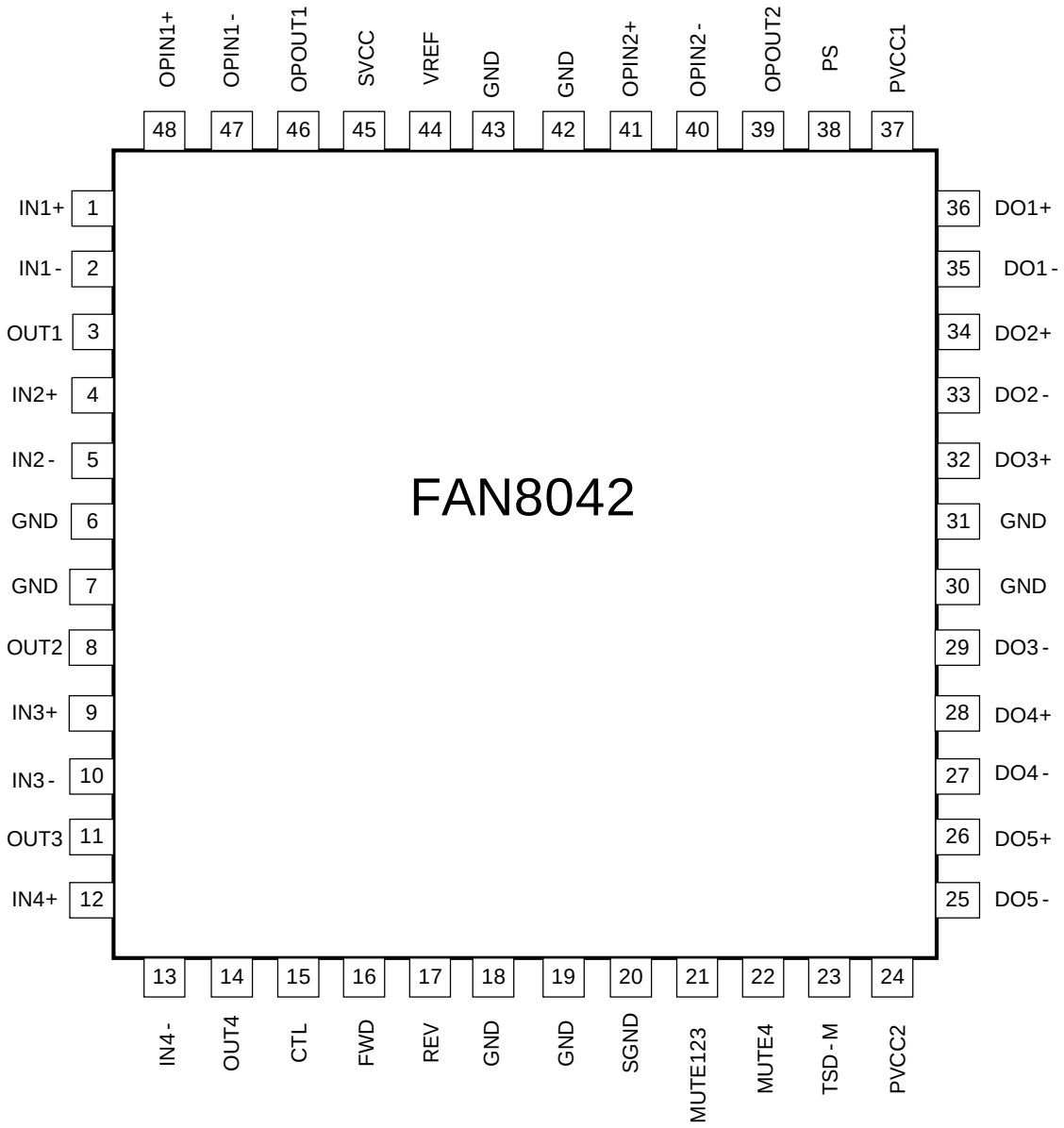
Typical Application

- Compact disk player
- Video compact disk player
- Car compact disk player
- Digital video disk player

Ordering Information

Device	Package	Operating Temperature
FAN8042	48-QFP-1010E	–35°C ~ +85°C

Pin Assignments



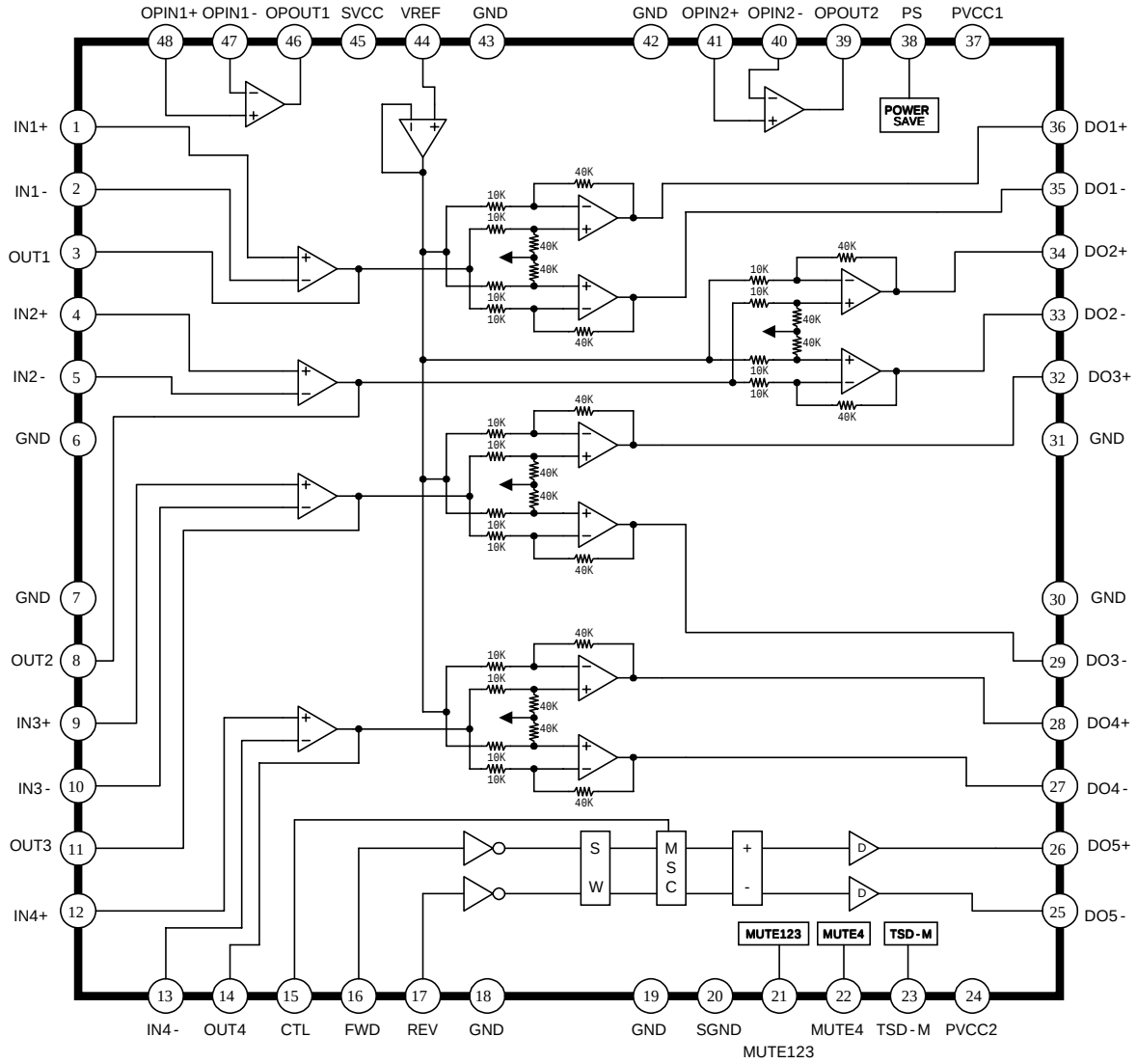
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Descrition
1	IN1+	I	CH1 op-amp input (+)
2	IN1–	I	CH1 op-amp input (–)
3	OUT1	O	CH1 op-amp output
4	IN2+	I	CH2 op-amp input (+)
5	IN2–	I	CH2 op-amp input (–)
6	GND	-	Ground
7	GND	-	Ground
8	OUT2	O	CH2 op-amp output
9	IN3+	I	CH3 op-amp input (+)
10	IN3–	I	CH3 op-amp input (–)
11	OUT3	O	CH3 op-amp output
12	IN4+	I	CH4 op-amp input (+)
13	IN4–	I	CH4 op-amp input (–)
14	OUT4	O	CH4 op-amp output
15	CTL	I	CH5 motor speed control
16	FWD	I	CH5 forward input
17	REV	I	CH5 reverse input
18	GND	-	Ground
19	GND	-	Ground
20	SGND	-	Signal Ground
21	MUTE123	I	Mute for CH1,2,3
22	MUTE4	I	Mute for CH4
23	TSD-M	O	TSD monitor
24	PVCC2	-	Power supply voltage 2 (For CH4, CH5)
25	DO5-	O	CH5 drive output (-)
26	DO5+	O	CH5 drive output (+)
27	DO4–	O	CH4 drive ouptut (–)
28	DO4+	O	CH4 drive output (+)
29	DO3–	O	CH3 drive ouptut (–)
30	GND	-	Ground
31	GND	-	Ground
32	DO3+	O	CH3 drive output (+)

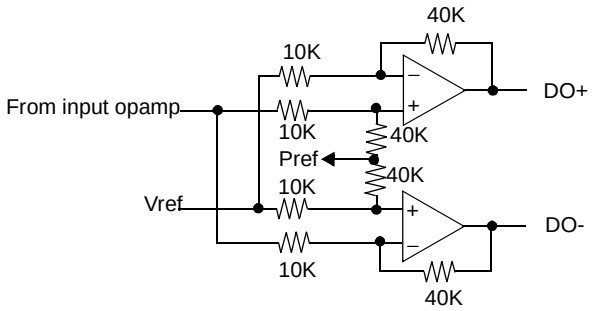
Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Descrition
33	DO2–	O	CH2 drive ouptut (–)
34	DO2+	O	CH2 drive output (+)
35	DO1–	O	CH1 drive ouptut (–)
36	DO1+	O	CH1 drive output (+)
37	PVCC1	-	Power supply voltage 1 (FOR CH1, CH2, CH3)
38	PS	I	Power save
39	OPOUT2	O	Normal op-amp2 output
40	OPIN2–	I	Normal op-amp2 input (–)
41	OPIN2+	I	Normal op-amp2 input (+)
42	GND	-	Ground
43	GND	-	Ground
44	VREF	I	Bias voltage input
45	SVCC	-	Signal & OPAMPs supply voltage
46	OPOUT1	O	Normal op-amp1 output
47	OPIN1–	I	Normal op-amp1 input (–)
48	OPIN1+	I	Normal op-amp1 input (+)

Internal Block Diagram

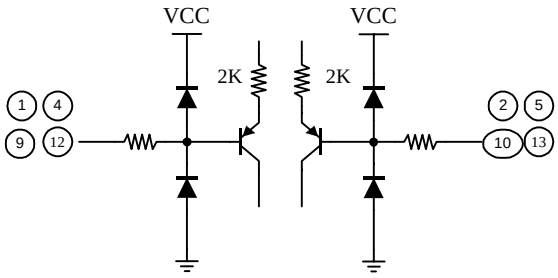
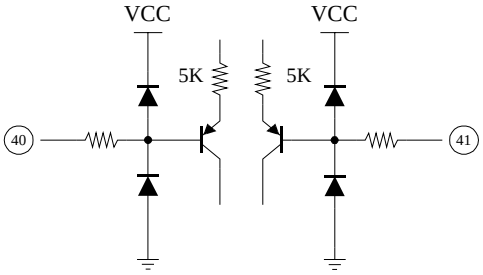
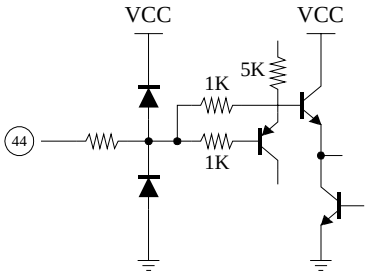
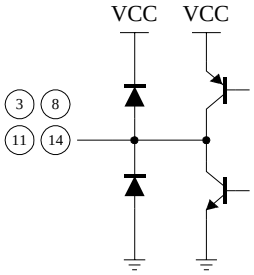


Note. Detailed circuit of the output power amp

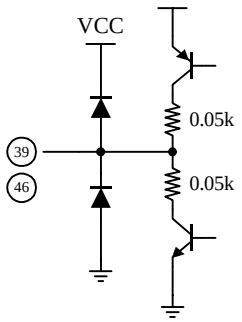
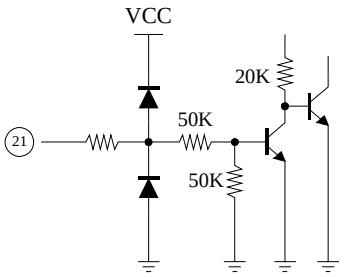
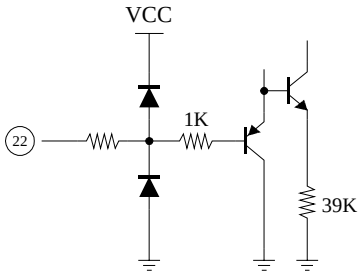
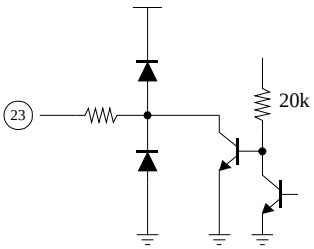


Pref1 is almost PVCC1 / 2
Pref2 is almost PVCC2 / 2

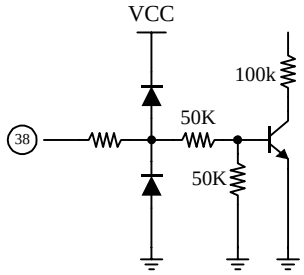
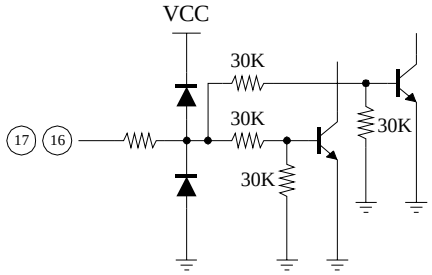
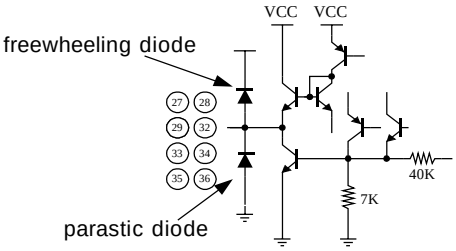
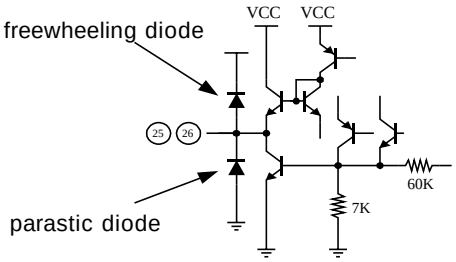
Equivalent Circuits

Description	Pin No	Internal Circuit
BTL INPUT	1,4,9,12, 2,5,10,13	
OP AMP INPUT	40,41	
VREF	44	
OP AMP OUTPUT	3,8,11,14	

Equivalent Circuits

Description	Pin No	Internal Circuit
OP OUT	39,46	
MUTE123	21	
MUTE4	22	
TSD-M	23	

Equivalent Circuits

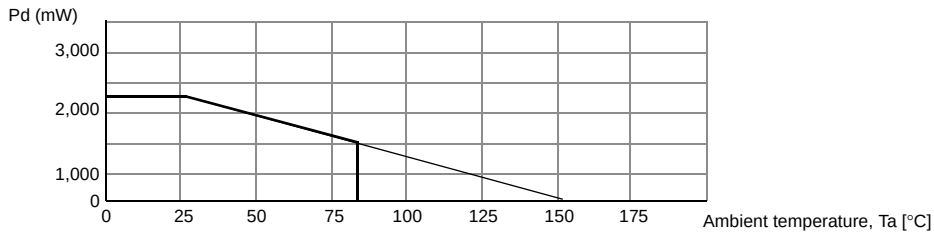
Description	Pin No	Internal Circuit
PS	38	
FWD,REV	16,17	
OUTPUT	27,29,33,35, 28,32,34,36	
OUTPUT	25,26	

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	$SVCC_{MAX}$	18	V
	PV_{CC1}	18	V
	PV_{CC2}	18	V
Power Dissipation	P_D	2.3[note]	W
Operating Temperature	T_{OPR}	–35 ~ +85	°C
Storge Temperature	T_{STG}	–55 ~ +150	°C
Maximum Output Current	I_{OMAX}	1	A

Notes:

1. When mounted on 70mm × 70mm × 1.6mm PCB
2. Power dissipation reduces 24mW/°C for using above T_A = 25°C
3. Do not exceed P_D and SOA



Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Supply Voltage	SV_{CC}	4.5	-	13.2	V
	PV_{CC1}	4.5	-	13.2	V
	PV_{CC2}	4.5	-	13.2	V

Electrical Characteristics

(SV_{CC} =5V, PV_{CC1} = PV_{CC2} = 11V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Quiescent circuit current	I_{CC}	Under no-load	-	30	-	mA
Power save on current	I_{PS}	Under no-load (Note1)	-	-	1	mA
Power save on voltage	V_{PSON}	Pin38 = Variation	-	-	0.5	V
Power save off voltage	V_{PSOFF}	Pin38 = Variation	2	-	-	V
Mute123 on voltage	V_{MON123}	Pin21 = Variation	-	-	0.5	V
Mute123 off voltage	$V_{MOFF123}$	Pin21 = Variation	2	-	-	V
Mute4 on voltage	V_{MON4}	Pin22 = Variation	-	-	0.5	V
Mute4 off voltage	V_{MOFF4}	Pin22 = Variation	2	-	-	V
BTL DRIVER CIRCUIT						
Output offset voltage	V_{OO}	V_{IN} = 2.5V	–100	-	+100	mV
Maximum output voltage 1	V_{OM1}	R_L = 10Ω	7.5	9.0	-	V
Maximum output voltage 2	V_{OM2}	R_L = 18Ω	8.5	9.5	-	V
Closed-loop voltage gain	A_{VF}	V_{IN} = 0.1Vrms	16.8	18	19.2	dB
Ripple rejection ratio	RR	V_{IN} = 0.1Vrms, f = 120Hz	-	60	-	dB
Slew rate	SR	Square, Vout = 4Vp-p	1	2	-	V/µs
INPUT OPAMP CIRCUIT						
Input offset voltage 1	V_{OF1}	-	–10	-	+10	mV
Input bias current 1	I_{B1}	-	-	-	400	nA
High level output voltage 1	V_{OH1}	-	4.4	4.7	-	V
Low level output voltage 1	V_{OL1}	-	-	0.2	0.5	V
Output sink current 1	I_{SINK1}	R_L = 50Ω	1	2	-	mA
Output source current 1	I_{SOU1}	R_L = 50Ω	1	2	-	mA
Common mode input range1	V_{ICM1}	-	-0.3	-	4.0	V
Open loop voltage gain 1	G_{VO1}	V_{IN} = –75dB	-	80	-	dB
Ripple rejection ratio 1	RR1	V_{IN} = –20dB, f = 120Hz	-	65	-	dB
Common mode rejection ratio 1	CMRR1	V_{IN} = –20dB	-	80	-	dB
Slew rate 1	SR1	Square, Vout = 3Vp-p	-	1.5	-	V/µs

Note:

1. When the voltage of the pin38 is below 0.5V then the power save circuit cuts off the main bias current, so that the whole circuits are disabled (whole circuits are "drive circuit ", "input op amp circuit " and "nomal op amp circuit ")

Electrical Characteristics (Continued)

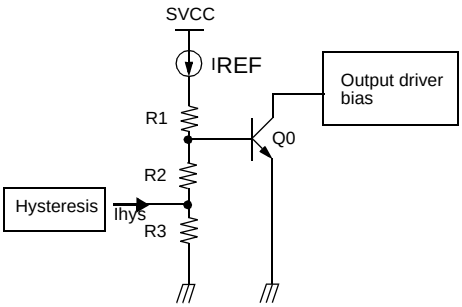
(SV_{CC} = 5V, PV_{CC1} = PV_{CC2} = 11V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
NORMAL OP AMP CIRCUIT 1						
Input offset voltage 2	V_{OF2}	-	–10	-	+10	mV
Input bias current 2	I_{B2}	-	-	-	400	nA
High level output voltage 2	V_{OH2}	-	4.4	4.7	-	V
Low level output voltage 2	V_{OL2}	-	-	0.2	0.5	V
Output sink current 2	I_{SINK2}	R_L = 50Ω	2	4	-	mA
Output source current 2	I_{SOU2}	R_L = 50Ω	2	4	-	mA
Common mode input range 2	Vicm2	-	-0.3	-	4.0	V
Open loop voltage gain 2	G_{VO2}	V_{IN} = –75dB	-	80	-	dB
Ripple rejection ratio 2	RR2	V_{IN} = –20dB, f = 120Hz	-	65	-	dB
Common mode rejection ratio 2	CMRR2	V_{IN} = –20dB	-	80	-	dB
Slew rate 2	SR2	Square, Vout = 3Vp-p	-	1.5	-	V/µs
NORMAL OP AMP CIRCUIT 2						
Input offset voltage 3	V_{OF3}	-	–15	-	+15	mV
Input bias current 3	I_{B3}	-	-	-	400	nA
High level output voltage 3	V_{OH3}	-	3	3.8	-	V
Low level output voltage 3	V_{OL3}	-	-	1.0	1.5	V
Output sink current 3	I_{SINK3}	R_L = 50Ω	10	-	-	mA
Output source current 3	I_{SOU3}	R_L = 50Ω	10	-	-	mA
Open loop voltage gain 3	G_{VO3}	V_{IN} =–75dB	-	80	-	dB
Ripple rejection ratio 3	RR3	V_{IN}= –20dB, f = 120Hz	-	65	-	dB
Common mode rejection ratio 3	CMRR3	V_{IN} = –20dB	-	80	-	dB
Slew rate 3	SR3	Square, Vout = 3Vp-p	-	1.5	-	V/µs
TRAY DRIVE CIRTUIT						
Input high level voltage	V_{IH}	-	2	-	-	V
Input low level voltage	V_{IL}	-	-	-	0.5	V
Output voltage 1	V_{O1}	PV_{CC2} = 11V, V_{CTL} = 3V, R_L = 45Ω	-	6	-	V
Output voltage 2	V_{O2}	PV_{CC2} = 13V, V_{CTL} = 4.5V, R_L = 45Ω	-	9	-	V
Output voltage 3	V_{O3}	PV_{CC2} = 11V, V_{CTL} = 1.5V, R_L = 10Ω	2.5	3	3.5	V
Output load regulation	ΔV_{RL}	V_{CTL}=3V, I_L=100mA → 400mA	-	300	700	mV
Output offset voltage 1	V_{OO1}	V_{IN} = 5V, 5V	–40	-	+40	mV
Output offset voltage 2	V_{OO2}	V_{IN} = 0V, 0V	–40	-	+40	mV

Application Information

1. Thermal Shutdown

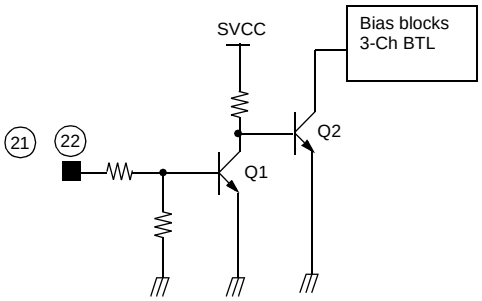
- When the chip temperature reaches to 160°C by abnormal condition, then the TSD circuit is activated.
- This shut down the bias current of the output drivers, and all the output drivers are in cut-off state. Thus the chip temperature begin to decrease.
- when the chip temperature falls to 135°C, the TSD circuit is deactivated and the output drivers are normally operated.
- The TSD circuit has the hysteresis temperature of 25°C.



2. CH MUTE Function

- When the pin21,22 is high, the TR Q1 is turned on and Q2 is off, so the bias circuit is enabled. On the other hand, when the pin21,22 is Low (GND) , the TR Q1 is turned off and Q2 is on, so the bias circuit is disabled.
- That is, this function will cause all the output drivers to be in mute state.
- Truth table is as follows;

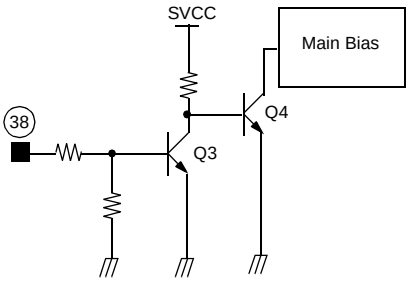
Pin 21,22	FAN8042
High	Mute-Off
Low	Mute-On



3. Power Save Function

- When the pin38 is high, the TR Q3 is turned on and Q4 is off, so the bias circuit is enabled. On the other hand, when the pin38 is Low (GND) , the TR Q3 is turned off and Q4 is on, so the bias circuit is disabled.
- That is, this function keeps all the circuit blocks of the chip off , thus the low power quiescent state is established
- Truth table is as follows;

Pin38	FAN8042
High	Power Save Off
Low	Power Save On

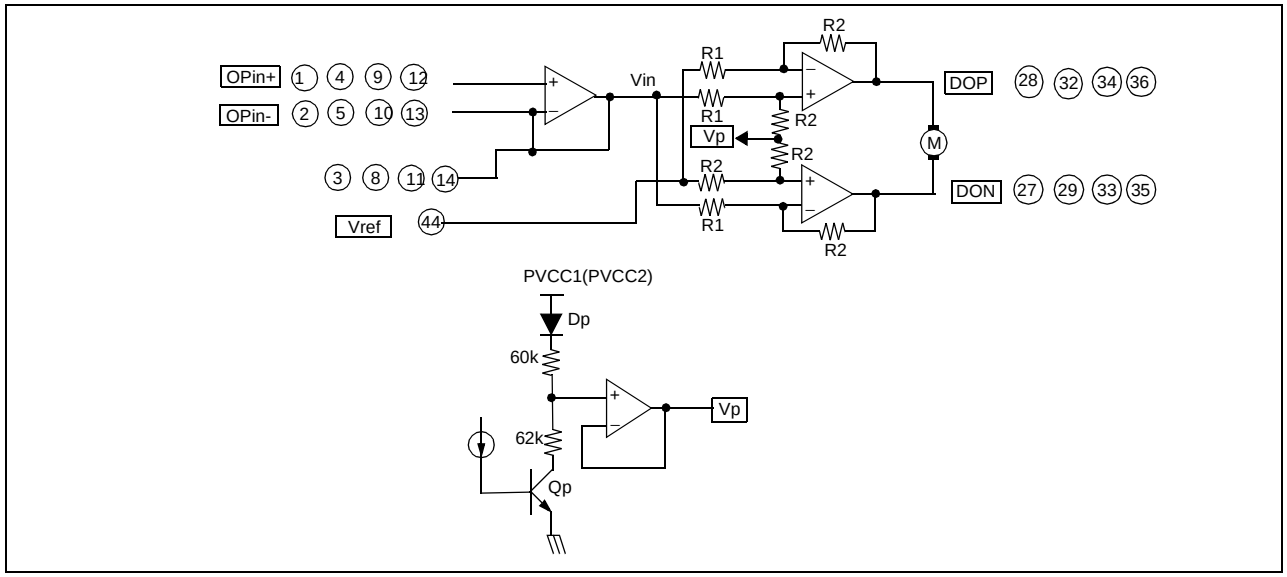


4. Tsd Monitor Function

- PIN23 is TSD monitor pin which detects the state of the TSD block and generates the TSD-monitor signal.
- In normal state Q5 is turned on, so Q6 is turned off. on the otherhand, When the TSD block is is activated then Q5 is turned off, so the voltage of pin23 is low.
- Truth table is as follows

pin23	FAN8042
High	Tsd Off
Low	Tsd On

5. Focus, Tracking Actuator, Spindle, Sled Motor Drive Part



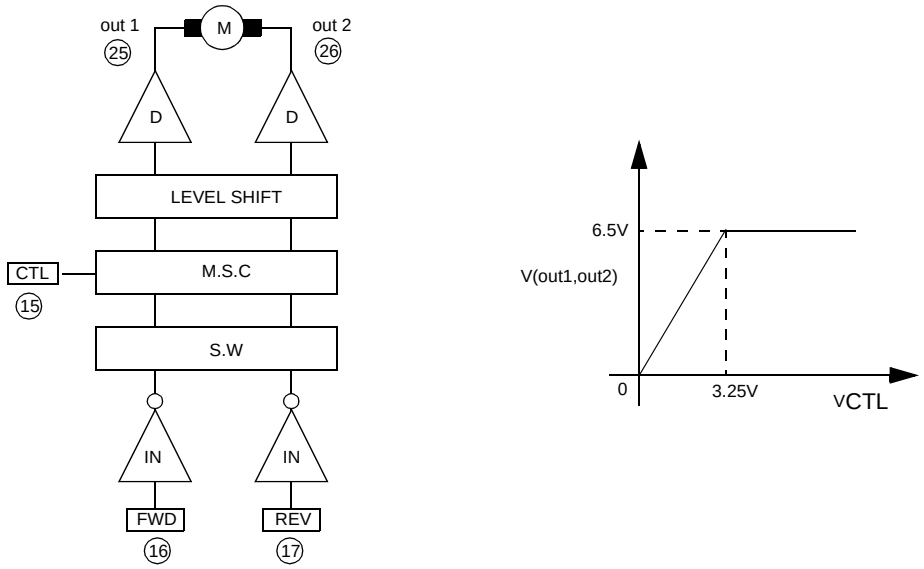
- The voltage, Vref is the reference voltage given by the external bias voltage of the pin 44.
- The input signal (Vin) through pins 1,4,9, 12 is amplified one time and then fed to the output stage. (assume that input opamp was used as a buffer)
- The total closed loop voltage gain is as follows

$$Vin = Vref + \Delta V$$
$$DOP = Vp + 4\Delta V$$
$$DON = Vp - 4\Delta V$$
$$Vout = DOP - DON = 8\Delta V$$
$$Gain = 20\log\frac{Vout}{\Delta V} = 20\log 8 = 18dB$$

- If you want to change the total closed loop voltage gain, you must use the input opamp as an amplifier
- The output stage is the balanced transformerless (BTL) driver.
- The bias voltage Vp is expressed as ;

$$Vp = (PVCC1 - VDp - VcesatQp) \times \frac{62k}{60k + 62k} + VcesatQp$$
$$= \frac{PVCC1 - VDp + VcesatQp}{1.97} + VcesatQp \quad \text{----------} \quad (1)$$

6. Tray, Changer,panel Motor Drive Part

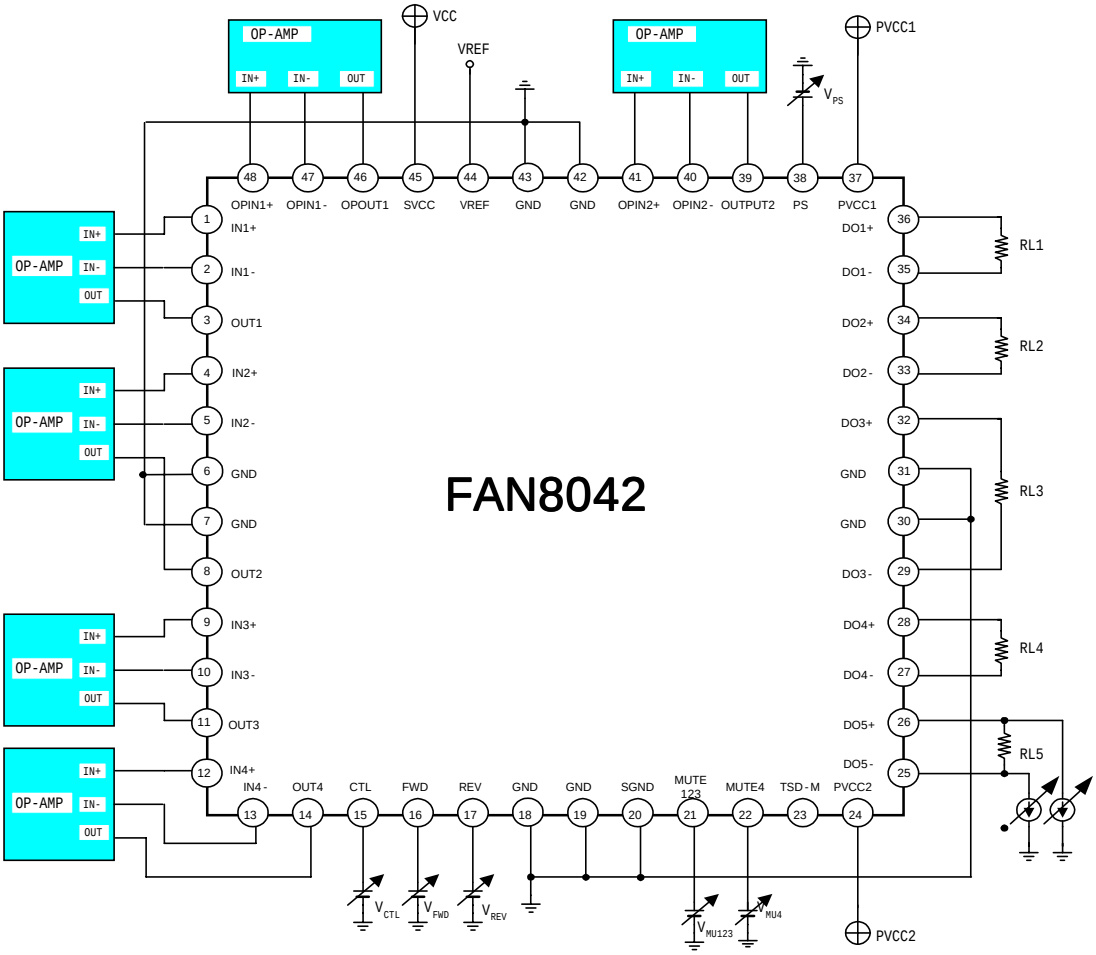


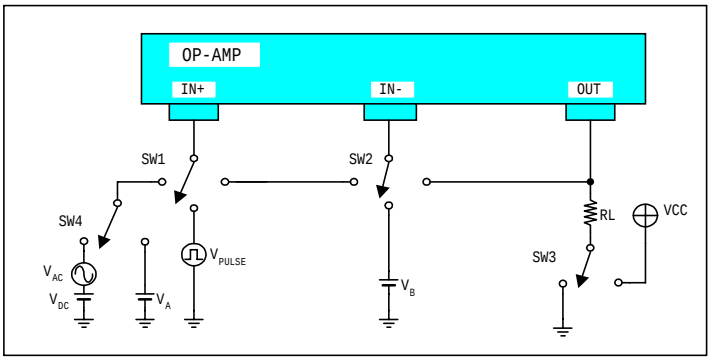
- Rotational direction control
  The forward and reverse rotational direction is controlled by FWD (pin16) and REV (pin17) and the input conditions are as follows.

INPUT		OUTPUT		
FWD	**REV**	**OUT 1**	**OUT 2**	**State**
H	H	Vp	Vp	Brake
H	L	H	L	Forward
L	H	L	H	Reverse
L	L	-	-	High impedance

- Where Vp(Power reference voltage) is approximately about 3.75V at PV_{CC2}=8V according to equation (1).
- Motor speed control (When SV_{CC}=PV_{CC2}=8V)
  - The almost maximum torque is obtained when the VCTL is open.
  - If the voltage of the pin15 is 0V, the motor will not operate.
  - When the control voltage of the pin15 is between 0 and 3.25V, the differential output voltage(V(out1,out2)) is about two times of control voltage. Hence, the control to the differential output gain is two.
  - When the control voltage is greater than 3.25V, the output voltage is saturated at the 6.5V because of the output swing limitation.

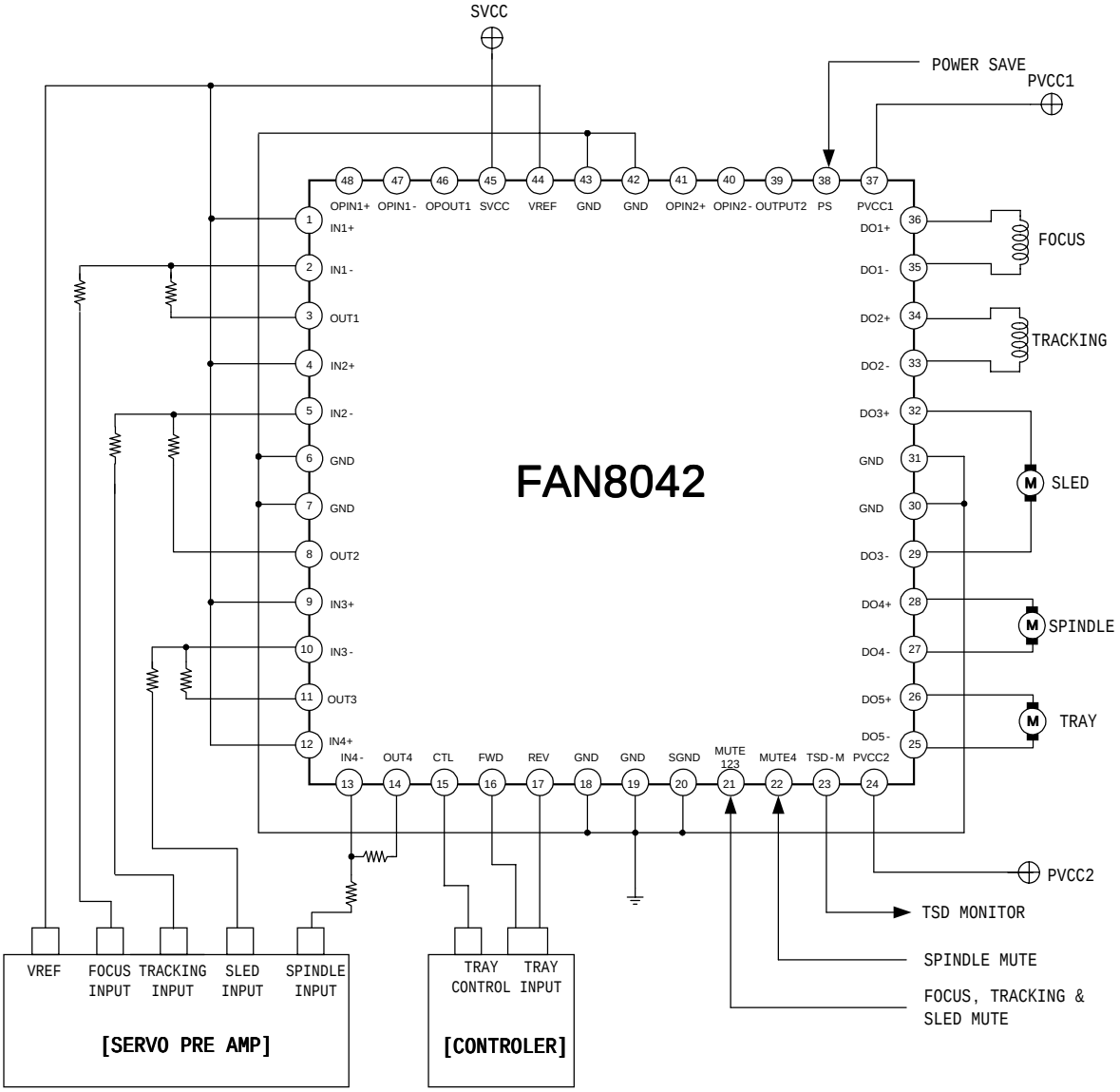
Test Circuits





Typical Application Circuits 1

[Voltage mode control mode]



Notes:

- Radiation pin is connected to the internal GND of the package.
- Connect the pin to the external GND
- This device that named FAN8042 is the same as FAN8034, and this datasheet was made for particular customers

Typical Application Circuits 2

[Differential PWM control mode]