FAIRCHILD SEMICONDUCTOR®

www.fairchildsemi.com

FAN8048

2 DC-DC Converter & 4-CH PWM Motor IC

Features

H-Bridge PWM Driver

- 4 Channels direct PWM H-bridge drivers
- Digital input and direct PWM output
- Internal power switches
  - ON state resistance : 2.0 Ω (typ.), which value added the upper and the lower switches

Synchronous DC-DC Converter

- Built-in step up converter (VG converter)
- Built-in two synchronous step up-down converter
- Built-in short circuit protection
- Internal Switches
  - Power Switch : 0.4Ω (typ.) at 500mA
  - -. Synchronous-Rectifier Switch : 0.4Ω (typ.) at 500mA

Others

- Built-in power-on reset circuit
- Built-in battery charge circuit
- Built-in voltage regulator control circuit
- Built-in thermal shutdown (TSD) circuit
- Buit-in channel mute circuit

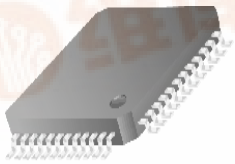
Typical application

- Portable CD-MP3 player

Description

The FAN8048 is a monolithic integrated circuit suitable for a 4 channels direct PWM H-bridge driver which incorporates two switch-mode step up-down converter with synchronous rectification provides local microprocessor and servo IC power in portable CD players and portable devices.

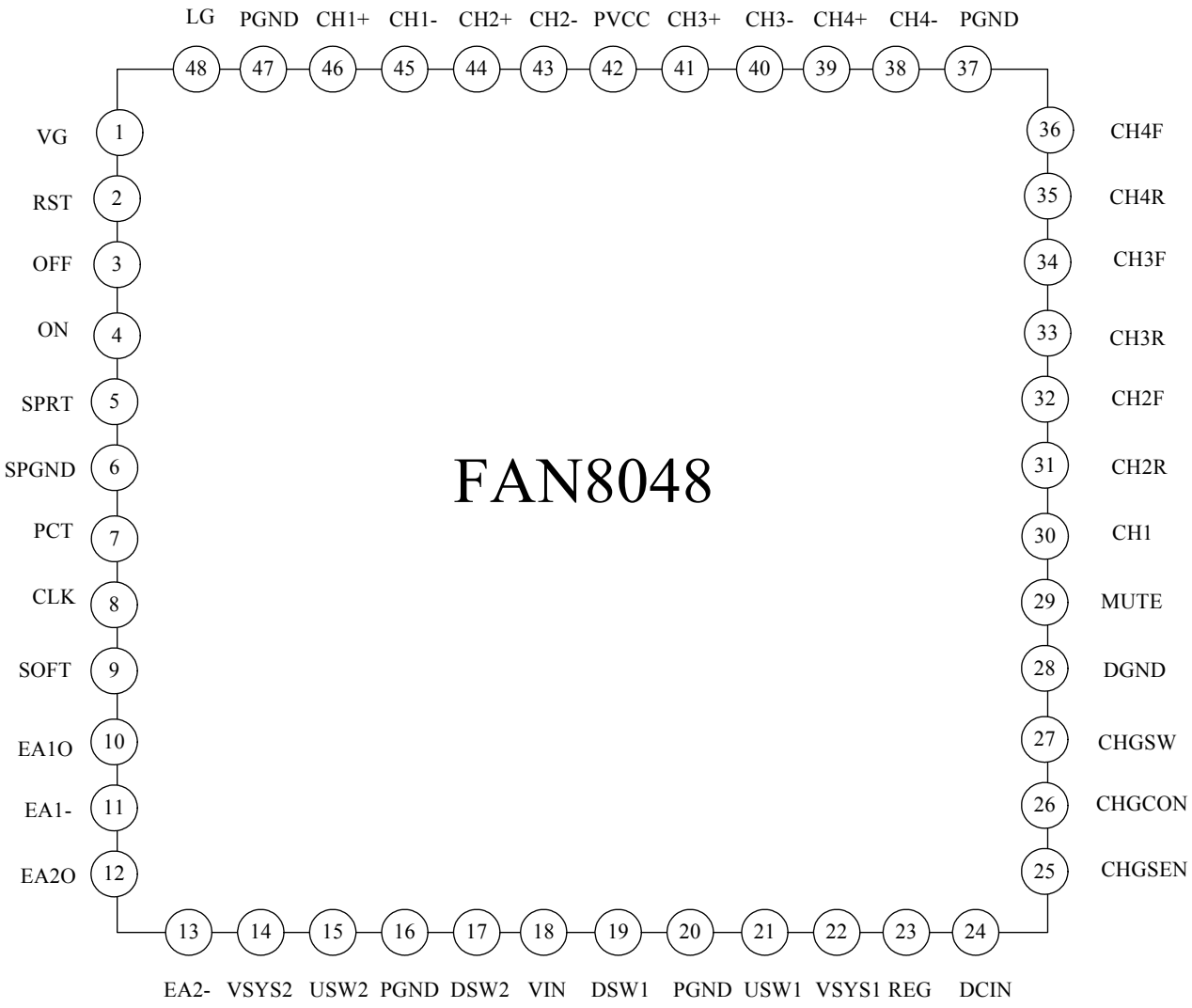
48-LQFP-0707



Ordering Information

Device	Package	Operating Temp.
FAN8048	48-LQFP-0707	-30°C ~ +85°C

Pin Assignments



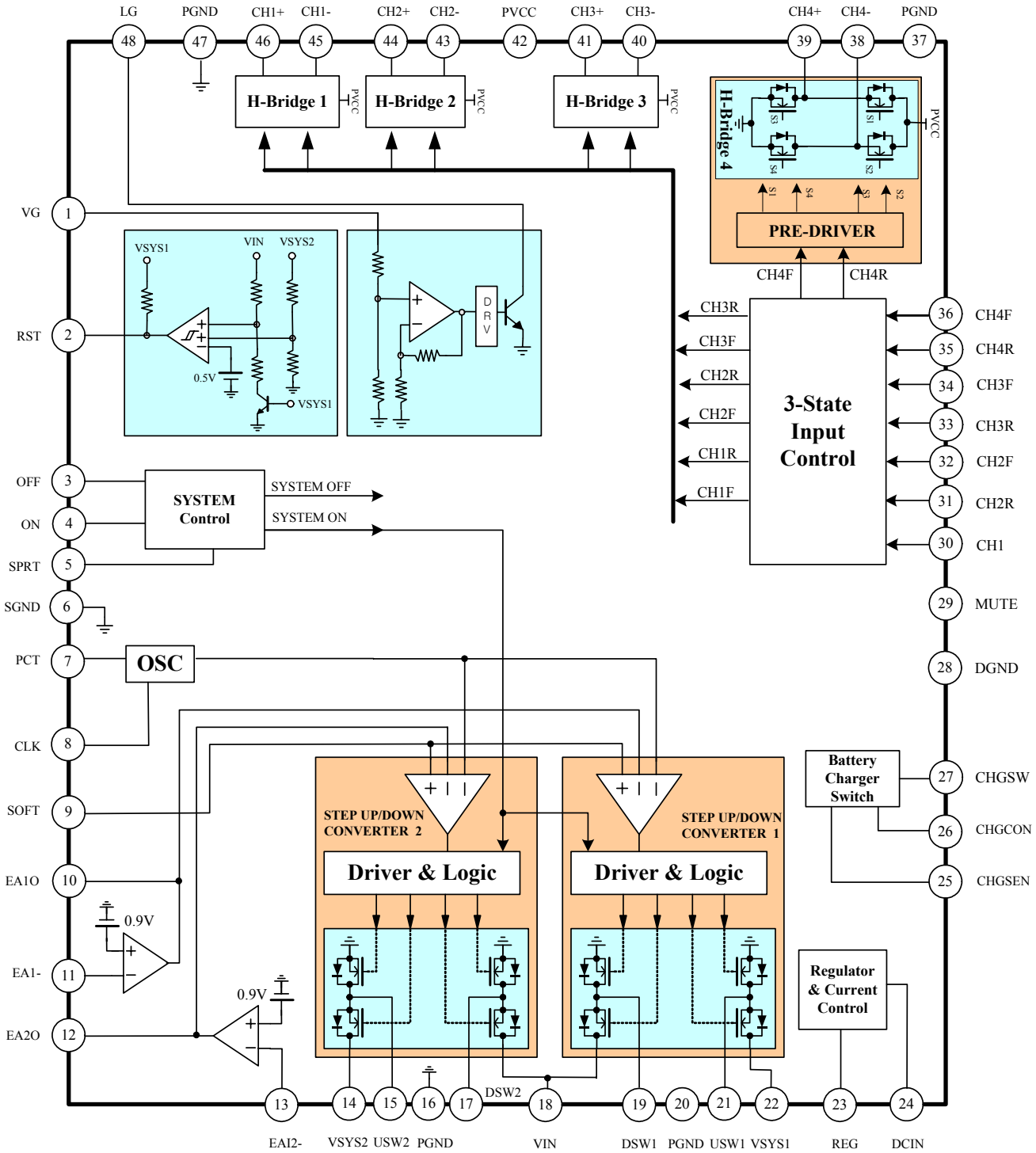
Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description
1	VG	-	Gate voltage for power MOSFET drive
2	RST	O	Power-on reset output
3	OFF	I	System-off signal input
4	ON	I	System-on signal input
5	SPRT	-	Short circuit protection delay time setting capacitor
6	SGND	-	Pre-driver ground
7	PCT	-	Triangular waveform pin
8	CLK	I	Clock input
9	SOFT	-	Soft start time setting capacitor of DC-DC converter 1 and 2
10	EA1O	O	Error amplifier output of DC-DC Converter1
11	EA1-	I	Error amplifier inverting input of DC-DC converter1
12	EA2O	O	Error amplifier output of DC-DC converter2
13	EA2-	I	Error amplifier inverting input of DC-DC converter2
14	VSYS2	-	Output of DC-DC converter2
15	USW2	-	DC-DCconvereter2 coil driving pin 1
16	PGND	-	Power ground
17	DSW2	-	DC-DC convereter2 coil driving pin 2
18	VIN	-	Input voltage of DC-DC coverter 1 and 2
19	DSW1	-	DC-DC convereter1 coil driving pin 2
20	PGND	-	Power ground
21	USW1	-	DC-DC convereter1 coil driving pin 1
22	VSYS1	-	Output of DC-DC converter1
23	REG	O	Regulator control output
24	DCIN	-	Adaptor power supply input pin
25	CHGSEN	I	Charger current sense Input
26	CHGCON	O	Charger control output
27	CHGSW	I	Charger mode switch input
28	DGND	-	Digital circuit ground
29	MUTE	I	Channel mute input
30	CH1	I	CH1 input pin
31	CH2R	I	CH2 reverse input pin
32	CH2F	I	CH2 forward input pin
33	CH3R	I	CH3 reverse input pin
34	CH3F	I	CH3 forward input pin
35	CH4R	I	CH4 reverse input pin
36	CH4F	I	CH4 forward input pin
37	PGND	-	Power ground
38	CH4-	O	Channel 4 negative output
39	CH4+	O	Channel 4 positive output
40	CH3-	O	Channel 3 negative output
41	CH3+	O	Channel 3 positive output
42	PVCC	-	Power supply for H-bridge driver
43	CH2-	O	Channel 2 negative output
44	CH2+	O	Channel 2 positive output

Pin Definitions (Continued)

Pin Number	Pin Name	I/O	Pin Function Description
45	CH1-	O	Channel 1 negative output
46	CH1+	O	Channel 1 positive output
47	PGND	-	Power ground
48	LG	-	VG voltage up coil driving pin

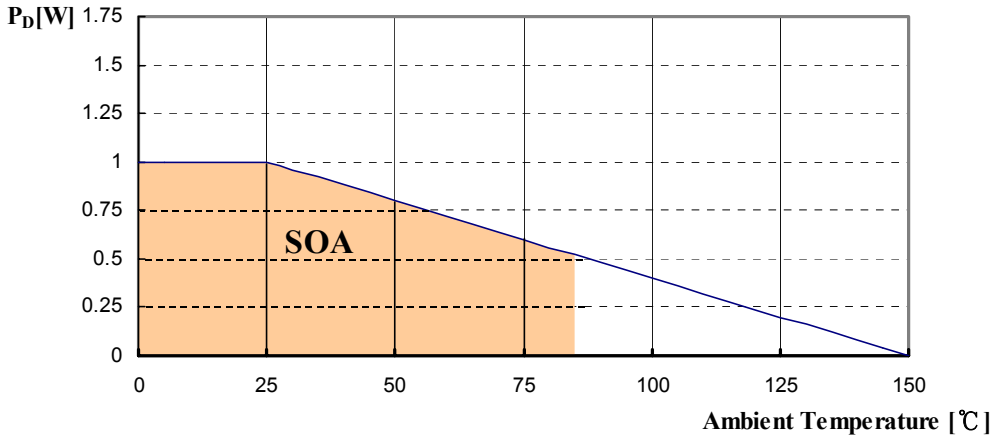
Internal Block Diagram



Absolute Maximum Ratings (Ta = 25×C)

Parameter	Symbol	Value	Unit
H-bridge driver supply voltage	PVCC	7	V
Predriver supply voltage	VG	12	V
Primary side input voltage of DC-DC converter	VIN	7	V
Output voltage of DC-DC converter1	VSYS1	7	V
Output voltage of DC-DC converter2	VSYS2	7	V
AC adapter supply voltage	VDCIN	12	V
H-bridge driver output current	I_O	500	mA
Power dissipation	PD	1.0	W
Operating temperature	T_{OPR}	-30 ~ +85	°C
Stroage temperature	T_{STG}	-55 ~ +150	°C

Power Dissipation Curve (Air Condition = 0m/S)



Notes:
1. When mounted on 2mm × 114.3mm × 1.6mm PCB (FR-4 glass epoxy material).
2. Refer: EIA/ J SED 51-2 and EIA/ J SED 51-3
JSED51-2 : Integrated circuits thermal test method environmental conditions - Natural convection
JSED51-3 : Low effective thermal conductivity test board for leaded surface mount packages
3. Do not exceed PD and SOA(Safe Operating Area).

Recommended Operating Conditions (Ta = 25×C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
H-bridge driver supply voltage	PVCC	1.2	2.4	4.5	V
Power supply of DC-DC converter	VIN	1.8	2.4	4.5	V
Output voltage of DC-DC converter1	VSYS1	2.0	-	3.6	V
Output voltage of DC-DC converter2	VSYS2	1.6	-	VSYS1	V
AC adaptor supply voltage	DCIN	5.0	7.0	10.0	V

Electrical characteristics

(PVCC=VIN=2.4V, VSYS1=VSYS2=2.7V, VG=7.0V, DCIN=0V, C_{PCT}=470pF, Ta=25°C,unless otherwise specifid)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CURRENT						
PVCC quiescent current	I_{PVCC}	-	-	-	3.0	μA
VIN operating current	I_{VIN}	VON = 0V	-	1.6	3.0	mA
DCIN operating current	I_{DCIN}	DCIN = 5V	-	-	1.0	mA
VG operating current1	I_{VG}	Non driving 4 channels	-	1.0	1.5	mA
VG operating current2 (Note1)	I_{VG4CH}	Driving by 4 channels	-	1.5	2.0	mA
VSYS1 operating current	I_{VSYS1}		-	3.0	5.0	mA
VSYS2 operating current	I_{VSYS2}		-	-	1.0	mA
SYNCHRONOUS DC-DC CONVERTER PART						
VG CONVERTER PART						
VG output voltage	V_{VG}	IVG=1mA	6.0	7.0	8.0	V
VG converter start voltage	V_{VGST}	VG=3 → 5V Sweep	3.3	3.9	4.5	V
Oscillation frequency	F_{LG}	VG=3.5V, VLG=5V	65	100	135	KHz
STEP UP/DOWN CONVERTER (COMMON))						
VSYS voltage at voltage up mode	V_{UP}	VIN=2.0V, ISYS=100mA	2.58	2.7	2.82	V
VSYS Load Stability at voltage up mode	ΔV_{UP}	VIN=2.0V, ISYS=0 to 150mA	-30	1.0	30	mV
VSYS voltage at voltage down mode	V_{DOWN}	VIN=3.0V, ISYS=100mA	2.58	2.7	2.82	V
VSYS load stability at voltage down mode	ΔV_{DOWN}	VIN=3.0V, ISYS=0 to 150mA	-30	1.0	30	mV
VSYS output stability at voltage up/down	ΔV_{UPDW}	$\Delta V_{UPDW}=V_{UP}-V_{DOWN}$	-30	0	30	mV
ERROR AMPLIFIER						
Error amplifier threshold voltage	V_{EINTH}	-	0.86	0.9	0.94	V
Error amplifier output voltage	V_{EOL}	-	-	0.16	0.2	V
Error amplifier input current	I_{EIN}	VEI=0.8V	-1	0.1	1	μA
Error amplifier source current	$I_{ESOURCE}$	VEO=0V, VEI=0V	150	-	-	μA
Error amplifier sink current	I_{ESINK}	-	1	-	-	mA
VSYS1 OPTION CIRCUIT						
Error amplifier1 short circuit detection voltage	V_{eos}	SPRT=L → H	1.20	1.35	1.45	V
SPRT input current1	I_{sprt1}	VEI=0V, VSPRT=0V	-9	-6	-4	μA
SPRT input current2	I_{sprt2}	OFF=VSPRT=0V	-16	-12	-8	μA
SPRT threshold voltage	V_{sprth}	VPCT=0.3V, VEO=0.4V,VEI=0V, DSW=H → L	0.4	0.5	0.6	V
SOFT input current	I_{soft}	VSOFT=0V	-13	-10	-7	μA
SPRT/SOFT discharge reset voltage	V_{dis}	VSYS1=1.3 → 1.7V VSPRT, VSOFT=L → H	1.30	1.48	1.62	V
Voltage in switching between the starter and normal modes	V_{stn}	VSYS1=1.5 →2.0 V,DSW=H → L	1.70	1.84	1.95	V
Vstn hysterisis voltage (Note1)	V_{sthys}	VSYS1=1.5 →2.0 V	100	200	300	mV

Electrical characteristics (Continued)

(PVCC=VIN=2.4V, VSYS1=VSYS2=2.7V, VG=7.0V, DCIN=0V, C_{PCT}=470pF, Ta=25°C,unless otherwise specifid)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VSYS2 OPTION CIRCUIT						
VSYS2 voltage at buck mode operation	V_{BUCK}	VIN=2.4V, VSYS2=1.8V ISYS2=100mA	-	1.8	-	V
Load stability of VSYS2 at buck mode operation	V_{LS}	VIN=2.4V, VSYS2=1.8V ISYS2=0 → 100mA	-30	0	30	mV
OSCILLATOR (PCT)						
Source current	I_{SOURCE}	-	34	42	50	μA
Sink current	I_{SINK}	-	11	14	17	μA
Oscillation frequency1	F_{OSC1}	No CLK, At self oscillation	45	60	75	KHz
Oscillation frequency2	F_{OSC2}	CLK=88.2kHz, At synchronization mode	85.2	88.2	91.2	KHz
Maximum duty ratio (Note1)	D_{MAX}	CLK=88.2kHz		75		%
OUTPUT SWITCHES						
On resistance of upper switch	R_{ONSWU}	Switch A and D, ISYS=500mA	-	0.4	0.6	Ω
On resistance of lower switch	R_{ONSWL}	Switch B and C, ISYS=500mA	-	0.4	0.6	Ω
Leakage current of upper switch	I_{LSWU}	Switch A and D	-	0	2	μA
Leakage current of lower switch	I_{LSWL}	Switch B and C	-	0	2	μA
POWER-ON RESET						
RST threshold voltage1	V_{RST1}	VIN=2.4V, VSYS2=1.0 → 1.8V	1.20	1.35	1.50	V
Hysteresis voltage1	ΔV_{RST1}	VIN=2.4V, VSYS2=1.8 → 1.0V	40	70	100	mV
RST threshold voltage2	V_{RST2}	VSYS2=2.7V, VIN=1.0 → 1.8V	1.30	1.45	1.60	V
Hysteresis voltage2	ΔV_{RST2}	VSYS2=2.7V, VIN=1.8 → 1.0V	50	80	110	mV
CONTROL INPUT						
System-on threshold voltage	V_{ONTH}	VSYS1=VSYS2=0V	-	VIN - 0.65		V
System-on input low level voltage	V_{ONL}	VSYS1=VSYS2=0V	VIN -1.0	-	-	V
System-on input current	I_{ON}	VON=0V	6	16	26	μA
System-off threshold voltage	V_{OFFTH}	-		VSYS1-1.15		V
System-off input low level voltage	V_{OFFL}	-	VSYS1-1.4	-		V
System-off input current	I_{OFF}	-	-85	-70	-55	μA
H-BRIDGE PWM DRIVER PART						
(CH1)						
Out on Resistance	R_{ON1}	Top + bottom switches	-	2.0	3.0	Ω
Input Resistance	R_{IN1}	-	-	50	-	KΩ
High level Input voltage	V_{IH1}	-	2.2	-	-	V
Low level Input voltage	V_{IL1}	-	-	-	0.5	V
Rising Time (Note1)	T_{RISE1}	-	-	0.2	-	μs
Falling Time (Note1)	T_{FALL1}	-	-	0.2	-	μs
Minimum Pulse Width (Note1)	T_{MIN1}	-	-	300	-	ns

Electrical characteristics (Continued)

(PVCC=VIN=2.4V, VSYS1=VSYS2=2.7V, VG=7.0V, DCIN=0V, C_{PCT}=470pF, Ta=25°C,unless otherwise specifid)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
(CH2,3,4)						
Out on Resistance	R_{ON}	Top + bottom switches	-	2.0	3.0	Ω
Input Resistance	R_{IN}	-	-	30	-	KΩ
High level Input voltage	V_{IH}	-	2.2	-	-	V
Low level Input voltage	V_{IL}	-	-	-	0.5	V
Rising Time (Note1)	T_{RISE}	-	-	0.2	-	μs
Falling Time (Note1)	T_{FALL}	-	-	0.2	-	μs
Minimum Pulse Width (Note1)	T_{MIN}	-	-	300	-	ns
CONTROL INPUT						
Mute input high voltage	V_{MUTEH}	-	2.2	-	-	V
Mute input low voltage	V_{MUTEL}	-	-	-	0.5	V
REGULATOR AND CHARGER PART						
Regulator output voltage	V_{VIN}	DCIN=6.5V, Ivin1=200mA	3.7	4.0	4.3	V
Line regulation of regulator	ΔVdc	DCIN=5V → 7V, Ivin1=200mA	-50	0	50	mV
Load regulation of regulator	ΔVrl	Ivin1=0 → 200mA	-40	0	10	mV
CHGON Current	Ichon	-	15	-	-	mA
Constant Charge Current	Ichg	Rs=1.1Ω	400	450	500	mA
CHGSW-on high voltage	V_{CHGSWH}	-	2.0	-	-	V
CHGSW-on low voltage	V_{CHGSWL}	-	-	-	0.5	V
THERMAL SHUT DOWN						
Operating temperature (Note1)	TSD	-	-	150	-	°C
Thermal hysteresis (Note1)	T_{HYS}	-	-	20	-	°C

Notes:
1. Design reference value

Application Information

1. System Control and Protection Functions

1-1. System Enable/Disable Function

As shown in Figure 1, system enable ON (pin4) should be set low (typically under VIN - 0.65V) only once until OFF (pin3) receives the disable signal (typically under VSYS1 - 0.85V), then all circuits remain in enable status.

Also, to prevent malfunction, this function activates when the circuit short condition exists such as over current or circuit shorts, the whole circuit becomes the disable.

When the circuit is enabled, to obtain the necessary power (VG) to operate the internal circuits and upper side output power switches of the 4 channels H-bridge driver, the VG converter circuit is activated. Also, to stably operate all circuits, the VG converter keeps other circuits from activating until the output voltage of the VG converter reaches the specific voltage (3.9V). When the output voltage of the VG converter reaches 3.9V, the first DC-DC converter (DC-DC Converter1) activate. And when output voltage of DC-DC converter1(VSYS1) reaches 1.35V, the second converter (DC-DC Converter2) activates in sequence. The circuit activation sequence as stated above and a flow chart are shown in Figure 3 and Figure 4.

1-2. Channel Mute Function

When MUTE (pin29) is high (typically above 2.2V), the mute circuit activates, so the all motor driver (4 channels H-bridge driver) outputs are in mute state; on the other hand, when it is low (under 0.5V), mute state is off.

1-3. Thermal Shut Down(TSD) Function

This thermal shutdown (TSD) function is designed to protect the chip from being damaged as the chip's internal temperature rises. If the TSD circuit activates, all motor driver (4 channel H-bridge drivers) outputs are in mute state. When the chip's internal temperature reaches 150°C (typical), then the TSD circuit is activated, and when the chip temperature falls to 130°C or below, the TSD circuit is deactivated and the output drivers operate normally.

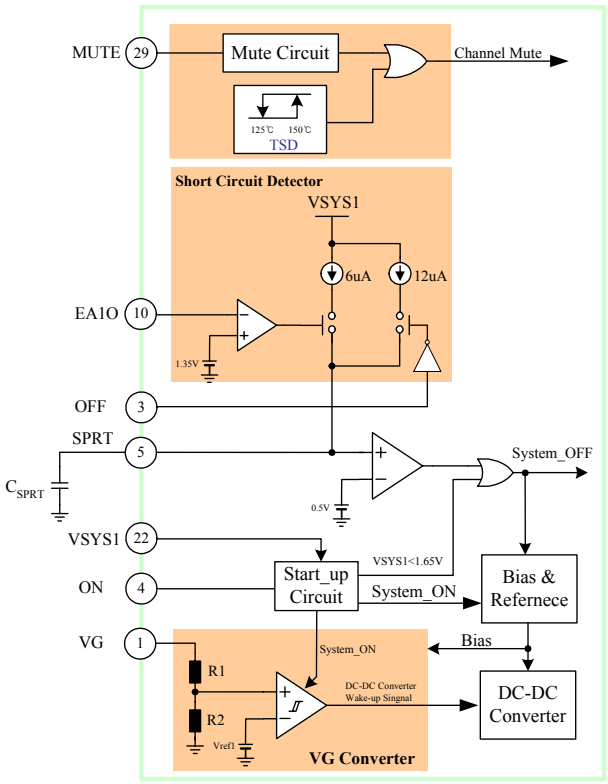


Figure 1. Block Diagram of System Control Circuit

1-4. Power-On Reset (POR) Function

FAN8048 has two DC-DC converters to supply stable power to external circuits and components of the CD player set. Therefore, for these output voltages of DC-DC converters to provide stable power to external circuits and their components, the DC input voltage,VIN, and the output voltages of converter, VSYS1 and VSYS2, monitoring function is required.
The DC input voltage, VIN, and the output voltage of converter2 are individually divided by the internal resistors and then compared with the internal 0.5V reference voltage, VREF2, to determine the low voltages condition.
This power on reset (POR) circuit is shown in Figure2.

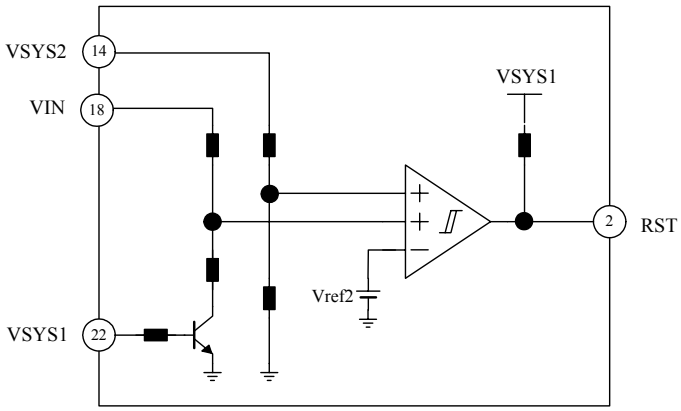


Figure 2. Block Diagram of Power On Reset

1-5. Power Sequence

The following graph and flowchart of Figure 3 and Figure 4 show the power sequence of the VG converter and two DC-DC converters (DC-DC converter1 and DC-DC Converter2); herein, VG converter generates power for internal circuits and upper side output power switches of the 4 channels H-bridge driver, and the DC-DC converters supply the external circuits and components.

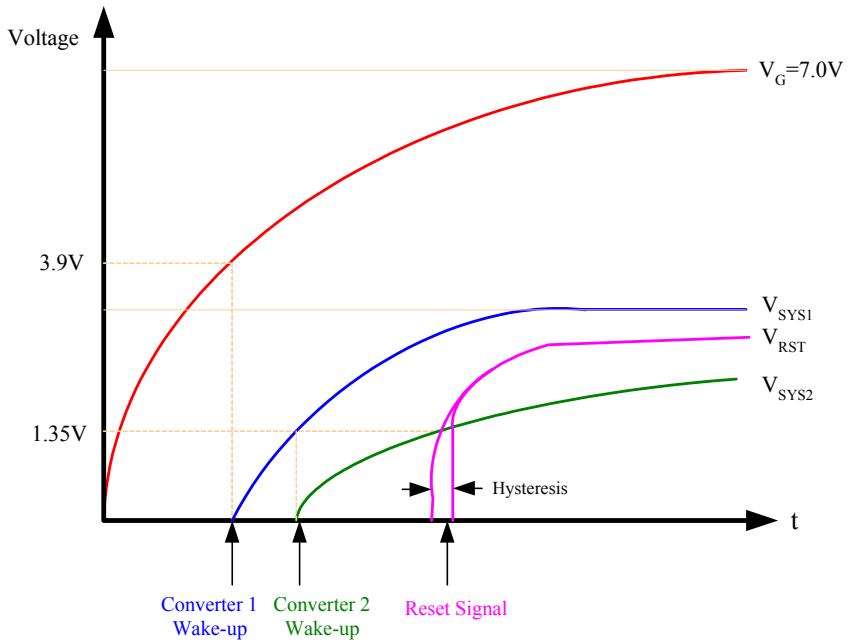


Figure 3. Plot of Power Sequence

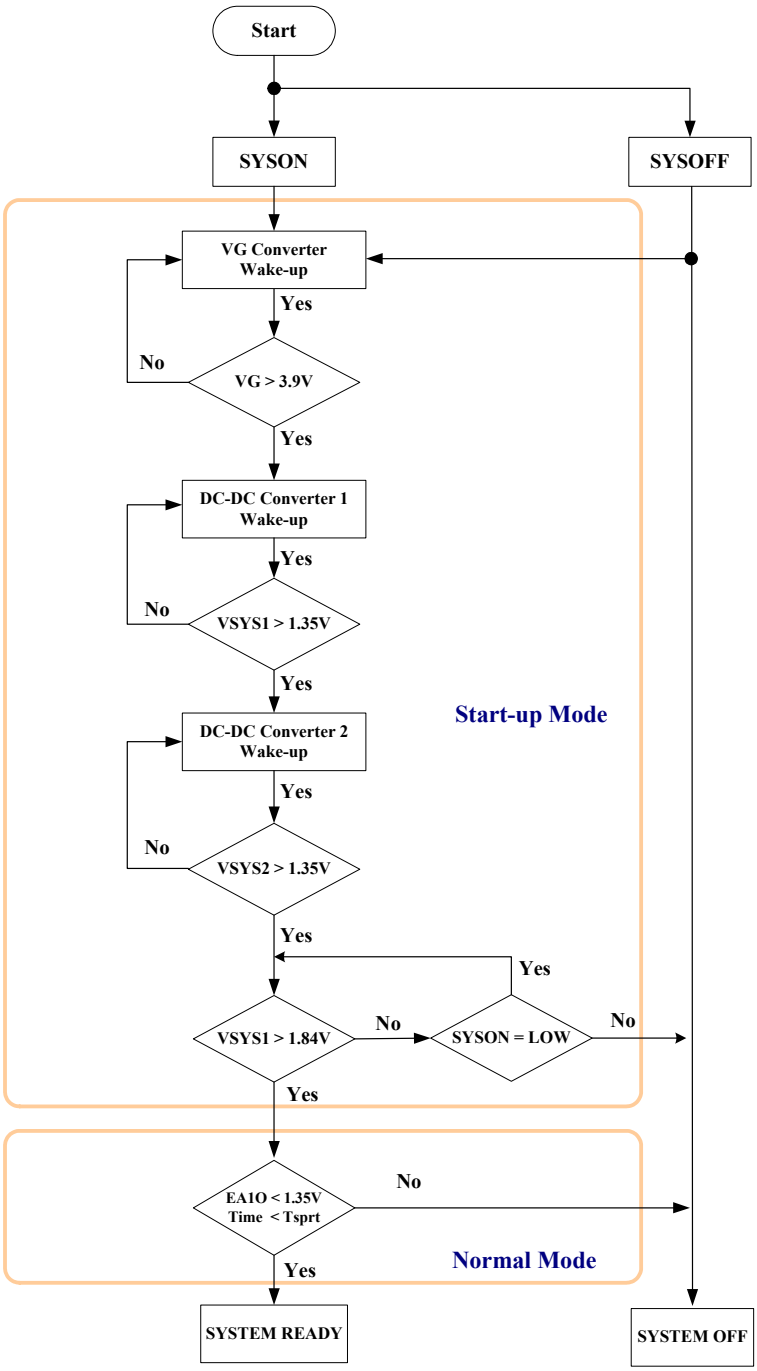


Figure 4. Flow Chart of Power Sequence

2. H-Bridge Driver (CH1, CH2, CH3 and CH4)

2-1. H-Bridge Driver for Actuators and Sled Motor (CH2, CH3 and CH4)

Channel 2, channel 3, and channel 4 have two inputs FWD and RVE and an H-bridge type of output to the forward or reverse Sled motor and the Focus and Tracking actuator as shown in Figure 5. The H-bridge driver operation is as in the following logical truth table below. That is, to forward or reverse, the output is the same as the input, and when the two input signals match, the lower switching devices (switches B and C) are turned-on, Sled motor, Focus and Tracking actuator are in braking state.

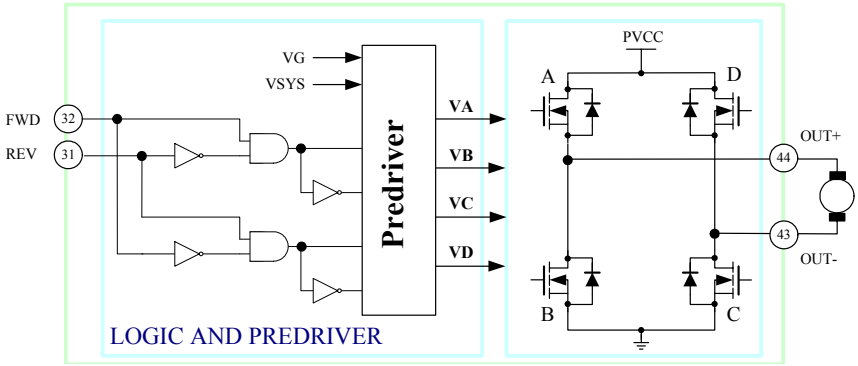


Figure 5. Block Diagram of H-Bridge driver for CH2, CH3 and CH4

2-2. Logical Truth Table

FWD	REV	OUT+	OUT-	Function
L	L	L	L	Brake
L	H	L	H	Reverse
H	L	H	L	Forward
H	H	L	L	Brake

2-3. H-Bridge driver for spindle motor (CH1)

Figure 6 shows spindle motor driver. The circuit consists of 3-states of input (High, Low, and High impedance) to perform forwarding, reversing, and braking of the motor. The detailed operation is shown in logical truth table.

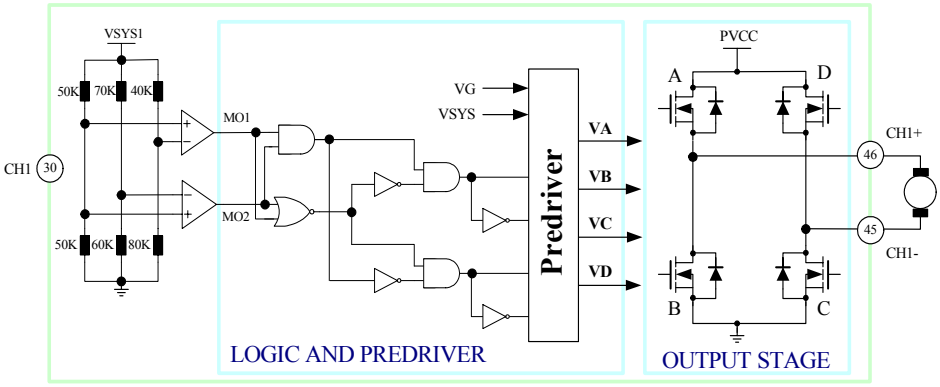


Figure 6. Block Diagram of H-Bridge driver for Spindle motor

2-4. Logical Truth Table

INPUT	MO1	MO2	CH+	CH-	Function
H	H	H	H	L	Forward
L	L	L	L	H	Reverse
Z	L	H	L	L	Brake

Note:

1. Z is high impedance input

3. DC-DC Converter (VG Converter and Synchronous DC-DC Converter)

3-1. VG Converter (Step up Converter)

The VG converter is used to generate necessary power (VG) for upper side output power switches operation of 4 channels H-bridge driver and other internal circuit operations as shown in Figure 7. The output voltage (VG) of VG converter is internally set to 7.0V, and it activates DC-DC Converter 1 when VG converter output voltage reaches 3.9 V. Also VG converter has an oscillator function, which is required for switching operations and to minimize external components.

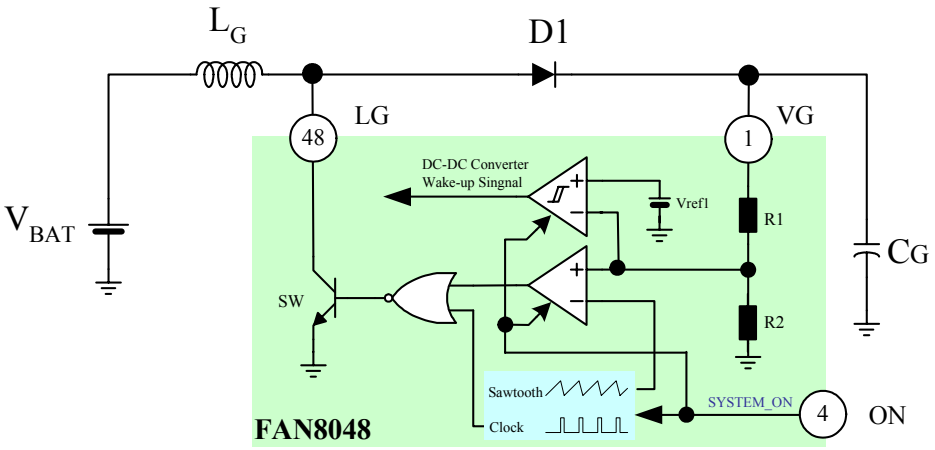


Figure 7. Set up Converter (VG Converter)

3-2. Synchronous Step-up/Down Converter

The FAN8048 provides high efficiency and low noise power for applications such as portable instrumentation. Figure 8 shows the functional block diagram of synchronous step up/down converter.

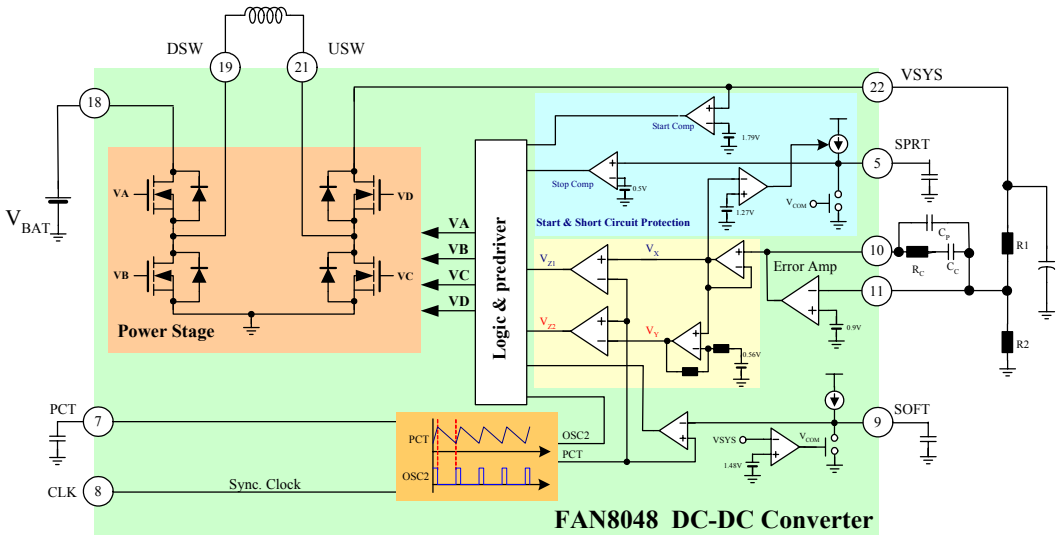


Figure 8. Block diagram of Step-up/down converter

In Figure 8, the output voltage (VSYS) of DC-DC converter is calculated as follows:

$$V_{SYS} = V_{REF} \times (1 + \frac{R1}{R2}) \; [V]$$

$$where, \;\; V_{REF} = 0.9[V]$$

3-3. Oscillator

Oscillator frequency is determined by the charging/discharging current i_{CG} and i_{DCG} of the internal circuit and capacitor (C_{PCT}) connected to PCT (pin7) and ground. To change oscillator frequency, you may change the C_{PCT} capacitor.

For example, the external capacitor (C_{PCT}) value can be calculated as follows:

$$t_{PCT} = \frac{C_{PCT} \times \Delta V_{PCT}}{i_{CG}} + \frac{C_{PCT} \times \Delta V_{PCT}}{i_{DCG}} = \frac{C_{PCT} \times \Delta V_{PCT}(i_{CHG} + i_{DCG})}{i_{CG} \times i_{DCG}}$$

$$f_{PCT} = \frac{1}{t_{PCT}} = \frac{i_{CG} \times i_{DCG}}{C_{PCT} \times \Delta V_{PCT} \times (i_{CG} + i_{DCG})}$$

$$C_{PCT} = \frac{i_{CG} \times i_{DCG}}{f_{PCT} \times \Delta V_{PCT} \times (i_{CG} + i_{DCG})}$$

Where, i_{CG} is charging current, which is 42uA, i_{DCG} is discharging current, which is 14uA, and oscillator peak-peak voltage, ΔV_{PCT} is approximately 300mV. This oscillator is designed to synchronize the frequency of the oscillator itself to the clock pulse frequency separately input to external CLK (pin8). To utilize this function, the oscillator frequency itself should be configured lower than the frequency of the external synchronous signal.

3-4. Error Amplifier

The error amplifier of the DC-DC converter is used to amplify the difference between internal reference voltage and output voltage. This amplified voltage generates a square wave pulse corresponding to the difference of triangular waveform-PCT output formed by triangular wave oscillatory circuit of pulse width modulation comparator (PWM comparator), whereby the square wave pulse stabilizes the output voltage by operating the DC-DC converter's switching devices through the operation circuit. The most well-known system stabilization method using an error amplifier is pole-zero compensation. Detailed system design standards and methods will be discussed in a later section of this document.

3-5. Short Circuit Protection Function

The short circuit protection is a function to protect circuits from being damaged from various abnormal conditions such as over current or circuit shorts; and on this occasion, when the error amplifier output voltage, EIO1, (pin10) of DC-DC converter1 reaches the specific voltage (typically 1.35V), the internal current source, i_{SPRT}, start charging the external capacitor, C_{SPRT} connected between SPRT(pin5) and ground as shown in Figure 1 and the DC-DC converter circuit will be shutdown. Also, to prevent malfunction, this function activates only when the circuit short condition exists for a certain amount of time. This time setting (T_{SPRT}) is determined according to the capacitance of external capacitor C_{SPRT}, and its formula is as follows:

$$T_{SPRT} = \frac{C_{SPRT} \times 0.5}{i_{SPRT}} [\text{sec}]$$

Where, i_{SPRT} is charging current, which is 6uA.

3-6. Soft Start

This function limits overshoot in the initial operation. This circuit operates when DC-DC converter 1 output voltage rises over a specific voltage (typically 1.48V), thereafter it starts charging the external capacitor C_{SOFT} connected between SOFT (pin9) and Ground. It restricts the error amplifier output voltage caused by sharp-rising capacitor voltage. Soft start time is determined by the following formula:

When the output voltage of the conveter, VSYS1, is brought above typically 1.48V, the soft start function is enable and the internal current source is begin to charging the capacitor, C_{SOFT}. A detailed diagram of this fuction is shown in Figure 8. The component C_{SOFT} provide a slow ramping voltage on the SOFT pin to provide a soft start function. The time constant in this case is shown by the next formular.

$$T_{SOFT} = C_{SOFT} \times i_{SOFT} = C_{SOFT} \times 10uA [\text{sec}]$$

where, i_{SOFT} = 10uA

3-7. Operation mode of Step-up/down converter

Figure 9 shows the connection of the four internal output power switches, external Inductor, and input/output voltage, which are components of the FAN8048 built-in DC-DC converter.

As shown in Figure 10, the DC-DC converter determines a switching operation mode (Buck, Buck-Boost and Boost) according to the relationship between control voltage VX and VY and oscillator output voltage V_{PCT}. Also, the DC-DC converter indicates the different operational statuses of output power switch (Output switches, A, B, C, and D) according to operational mode. Herein, control voltage VX is the output voltage of error amplifier, and voltage VY is level shift voltage in VX.

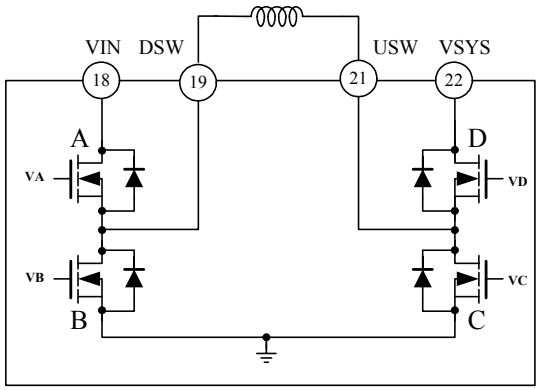


Figure 9. Simplified Diagram of Output Swiches

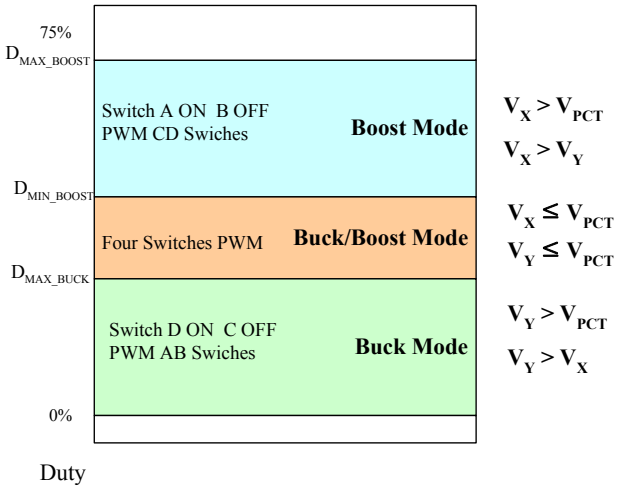


Figure 10. Switching control vs. internal control voltages, V_X and V_Y

3-8. Buck(Step-down) converter mode (VIN > VSYS)

The step-down converter keeps the average output voltage VSYS lower than DC input voltage VIN all the time. Figure 11-a shows a conceptual circuit diagram of the step-down converter in case an electrical load is pure resistance. Herein, all switching devices are supposed to be at ideal conditions and instantaneous output voltage VSYS is dependent on the status of switching devices. That is, the input/output of the step-down converter is obtained by the following formula according to the Volt-Sec balance condition and each waveform is shown in Figure.11-b, where D means duty cycle. In this formula, since duty ratio D is smaller than 1.0, average output voltage VSYS is always displayed in the lower range of the DC input voltage.

$$V_{SYS} = \frac{1}{D} \times V_{IN}[V]$$

where, D is duty cycle.

$$D = \frac{T_{ON}}{T_S}$$

In practical application circuits, there are several drawbacks as follows:

(1) As most practical circuits are not exposed to pure electrical resistance loads, but to inductive loads and because of the stray inductive there is the switch would have dissipate the inductive energy and therefore it may be destroyed. .
(2) This is not the case of most application circuit, but when output voltage fluctuates between zero and power voltage VIN, a low pass filter composed of an inductor and capacitor is required to minimize the output voltage ripple.

Figure 12 shows the operation waveform of internal control voltage VX and VY and output power switching devices in Step-down converter mode. When the internal control voltage VY is higher than control voltage VX and triangular waveform V_{PCT}, switch D is always turned-on and switch C is always turned-off in step-down converter mode. The switching operation of switch A is activated by the signal generated by comparison between internal control VX and triangular waveform voltage V_{PCT}. Also, synchronous switch B remains turned-on during synchronous switch B turn-off time. That is, in step-down converter mode, switch A and B always activate in opposite switching operations. The peak-peak ripple voltage (ΔVSYS) of output voltage is calculated using the following formula:

$$\Delta V_{SYS} = \frac{\Delta Q}{C_O} = \frac{1}{C_O} \times \frac{1}{2} \times \frac{\Delta I_L}{2} \times \frac{T_S}{2} = \frac{T_S}{8C} \times \frac{V_{SYS}}{L}(1-D)T_S$$

Where, ΔI_L is the inductor current from Figure11 (b) during turn-off (t_{OFF}).

$$\Delta I_L = \frac{V_{SYS}}{L}(1-D)T_S$$

The value of the output capacitor to reduce output voltage ripple is calculated using the following formula.

$$C = \frac{T_S}{8L} \times \frac{V_{SYS}}{\Delta V_{SYS}}(1-D){T_S}^2$$

The average value of the inductor current at boundary between continuos and discontinuous conduction mode is

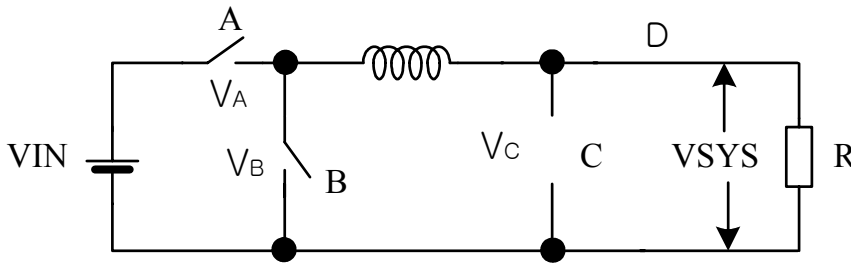
$$I_{LB} = \frac{1}{2} i_{L,peak} = \frac{DT_S}{2L}(V_{IN} - V_{SYS})$$

where,

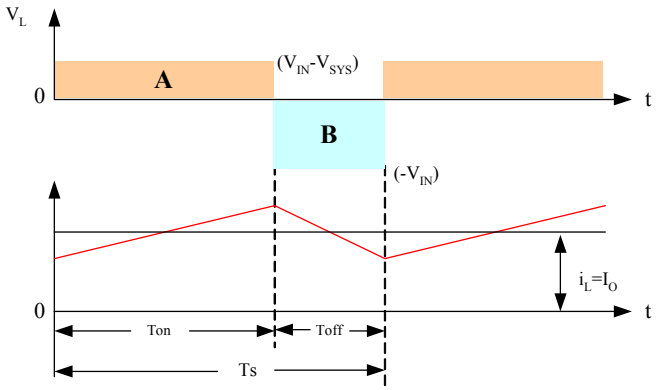
$$V_{IN} = \frac{V_{SYS}}{D}[V]$$

So to obtain the inductor value using the above formula, the redefined formula is as follows:

$$L = \frac{V_{SYS}(1-D)T_S}{2I_{O,\min}}$$



(a)



(b)

Figure 11. Synchronous Step-down Converter

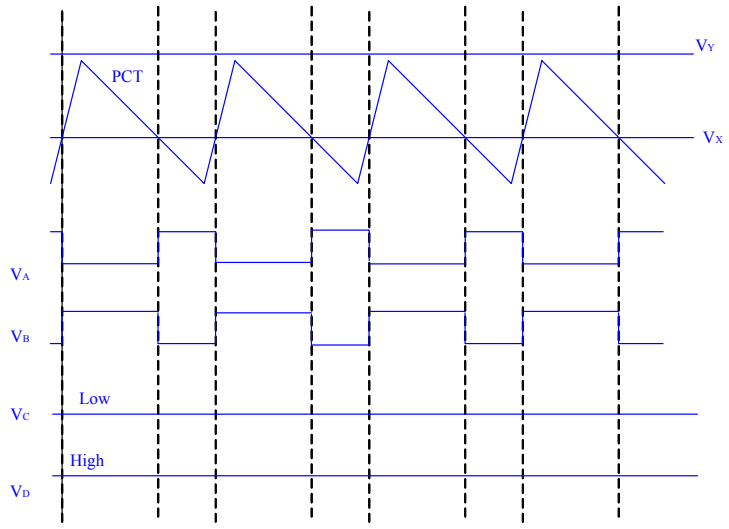


Figure 12. Switches operation waveforms during Buck Converter mode

3-9. Buck-Boost (Step-down/up) Converter Mode (VIN = VSYS)

As shown in Figure.13-a, the synchronous buck-boost converters take the mixed form of step-up and step-down converters. That is, in case switching devices in the series connection of the two converters activate in the same duty ratio, the input/output relationship during normal conditions can be expressed as follows: Namely, the output voltage VSYS can be higher or lower than DC input voltage VIN according to duty ratio D.

$$V_{SYS} = \frac{D}{1-D} V_{IN}[V]$$

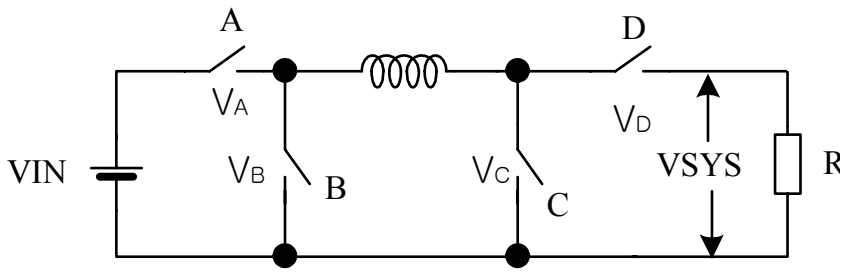
As shown in Figure 13-b, the current flowing through the inductor is constant in continuous conduction mode. And the input and output voltages relationship formula can be defined as follows, because , the integral of the inductor voltage over one time period to zero.

$$V_{SYS} D T_S + (-V_{SYS})(1-D) T_S = 0$$
$$\frac{V_{SYS}}{V_{IN}} = \frac{D}{1-D}$$

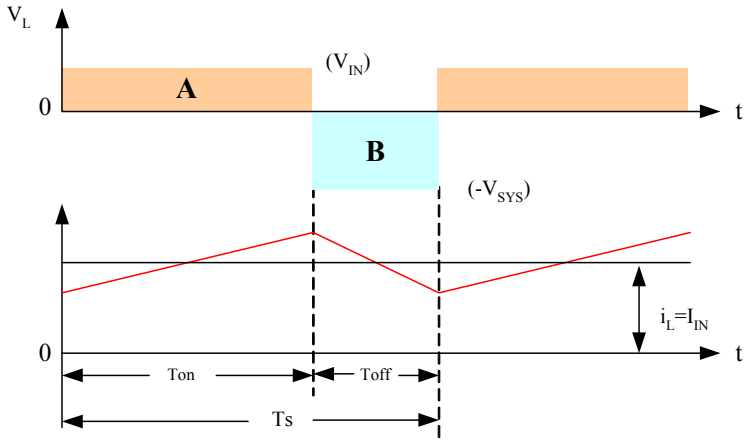
Assuming a lossless circuit, input and output power are the same (Pin=Po) and the above formula can be redefined as follows:

$$\frac{I_{SYS}}{I_{IN}} = \frac{1-D}{D}$$

As you can see in Figure 14, when internal control voltage VX and VY remain in the triangular waveform voltage V_{PCT} range, the converter acts as a step-up or step-down converter mode according to DC input voltage VIN and electrical load VSYS and ISYS status. As displayed in Figure13-a, in this operation mode all four switching devices of the output terminal activate upon operational mode step-up or step-down. Figure13-b shows the operational waveform of each section in this activation mode.



(a)



(b)

Figure 13. Synchronous Step-up/down Converter

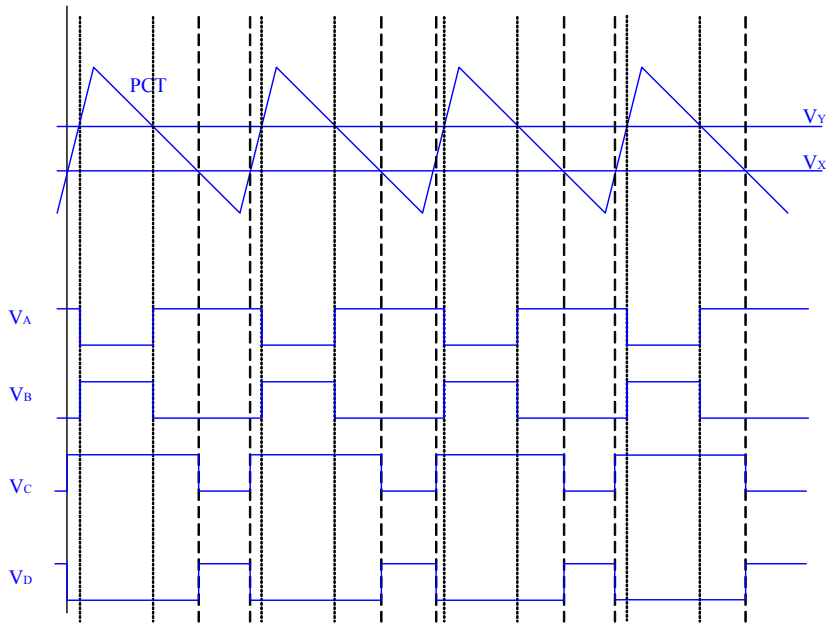


Figure 14. Output switches operation and waveforms at Buck/Boost (Step-up/down) mode

3-10. Boost (Step-up) converter mode (VIN < VSYS)

The step-up converter keeps the average output voltage VSYS higher than DC input voltage VIN, and its circuit diagram is shown in Figure 15-a. Figure 15-b shows an operational waveform in case inductor current is steady-state. Since in steady-state, the integral of the inductor voltage over one time period to zero, this can be expressed by the following formula:

$$(V_{IN} \times t_{ON}) + ((V_{IN} - V_{SYS}) \times t_{OFF}) = 0$$

From the above formula, a redefined formula is as follows after dividing by cycle Ts:

$$\frac{V_{SYS}}{V_{IN}} = \frac{T_S}{t_{OFF}} = \frac{1}{1-D}$$

$$V_{SYS} = \frac{1}{1-D} \times V_{IN}[V]$$

Assuming a lossless circuit, input and output power are the same (Pin=Po) and the above formula can be redefined as follows:

$$V_{IN} I_{IN} = V_{SYS} I_O$$

This can be expressed as follows using input/output current and duty ratio:

$$\frac{I_O}{I_{IN}} = (1-D)$$

In the boundary condition of continuous mode and discontinuous mode, the inductor's average current is defined as follows:

$$i_{LB} = \frac{1}{2} i_{L,peak}$$

$$= \frac{1}{2} \frac{V_{IN}}{L} T_{ON}$$

$$= \frac{T_S V_{SYS}}{2L} D(1-D)^2$$

From the above formula, since inductor current and input current are the same (i_{IN}=i_L), the average output current at the edge of continuous conduction mode can be redefined as below:

$$I_{OB} = \frac{T_S \times V_{SYS}}{2L} D(1-D)^2$$

In a practical synchronous step-up converter, the parasitic elements are due to the loss associated with the inductor, the capacitor and the switches; however, in this formula we assume that all components are at ideal conditions.In the continuous mode, as the output current and peak-peak voltage ripple are considered to be constant, this formula can be redefined as below:

$$\Delta V_{SYS} = \frac{\Delta Q}{C} = \frac{I_O D T_S}{C} = \frac{V_{SYS}}{R} \frac{D T_S}{C}$$

$$\frac{\Delta V_{SYS}}{V_{SYS}} = \frac{D T_S}{RC}$$

Where,

$$R = \frac{V_{SYS}}{I_O}[\Omega]$$

In Figure 16, when control voltage VX is always higher than VY and triangular waveform voltage V_{PCT}, Switch pairs C and D will alternately switching and their circuit is designed to operate as a step-up converter, whose output voltage is always higher than input voltage. Figure 15 shows the operational waveform at the output terminal of each switching device when it acts as a step-up converter. In this operations section, Switch A is always turned-on and switch B is always turned-off. Also, to limit the maximum output voltage in this mode, the maximum duty ratio is limited to about 75%.

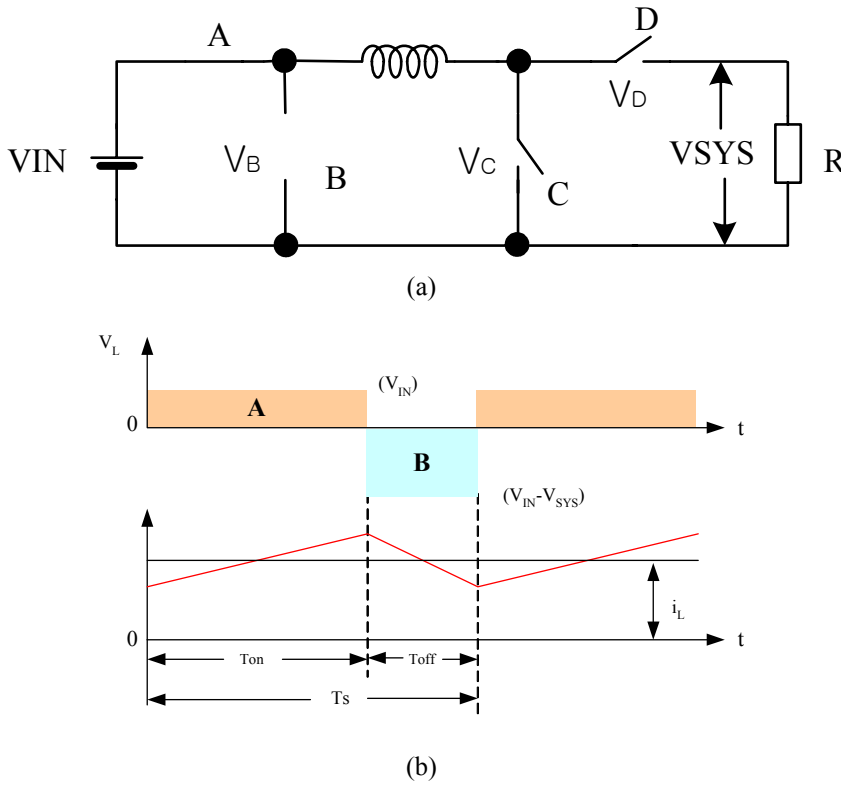


Figure 15. Synchronous Step-up Converter

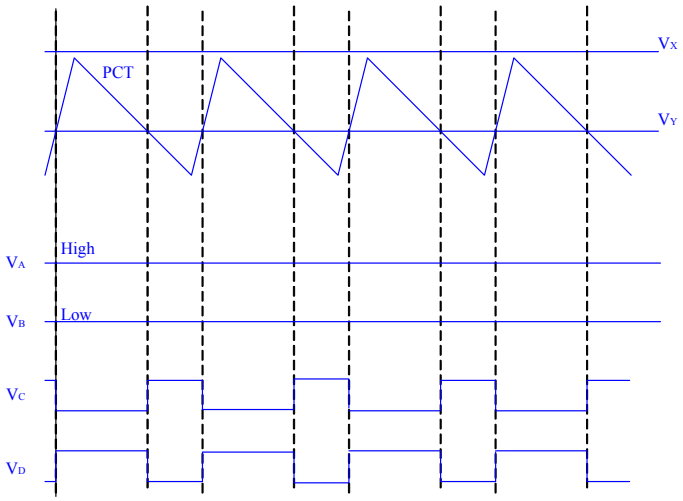


Figure 16. Output switch operational waveforms in Boost (Step-up) converter mode

3.10.1 Effect of Parasitic Elements in Step-up Converter

In a practical synchronous step-up converter, the parasitic elements are due to the loss associated with the inductor, the capacitor and the switches; however. Figure 17 qualitatively show the effect of these parasitics on the voltage transfer ratio. Unlike the ideal characteristic, in paractice VSYS/VIN declines as the duty ratio approaches unity. Because of very poor switch utilization at high values of duty ratio, the curves in this range are show as dotted.

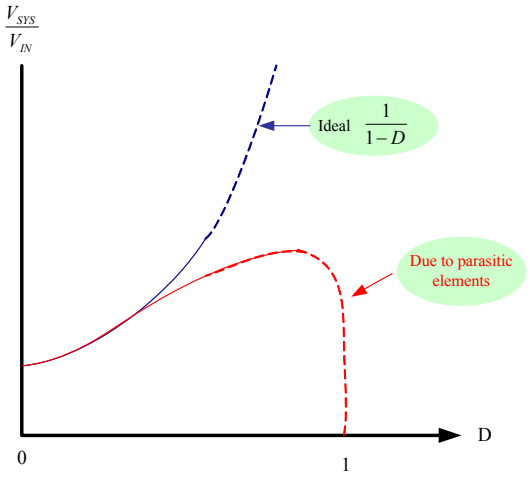


Figure 17. Effect of parasitic elements on voltage conversion ratio

3.11 Component of Error Amplifier Compensation Network

In this chapter, we would like discuss the method of converter error amplifier design to control voltage mode PWM. In general, a negative feedback control circuit composed of error amplifier using an operational amplifier and comparator is often used to stabilize output voltage in switching mode converters. Controller design standards and methods for a stable system are as follows:

(1) To reduce regulation error of the output voltage, the loop gain crossover frequency, f_C, should be as high as possible.
(2) To obtain stable phase margin, let the slope gain at 0dB be -20dB/dec. That is, have the gain phase at 0dB close to -90°.
(3) Set the loop gain crossover frequency, f_C be set to 1/5 ~ 1/10 of the switching frequency f_S.
But in boost converter, due to the RHP zero, f_{RHPZ}, the loop gain frequency, fC, must be designed well below the RHP zero because the boost converter have a right half plane (RHP) zero. ($f_C = f_{RHPZ}/10$)
(4) Set compensation pole, f_{P1} to cancel the ESR zero f_{FILTER_ZERO}. ($f_{P1} = f_{FILTER\_ZERO}$)
(5) Place a high-frequency compensator pole, f_{P2} to get the maximum attenuation of the switching ripple and high frequency noise the minimum phase lag at f_C.
(6) Place a two compensator zeroes, f_{Z1} and f_{Z2} below f_C. Place the fz1 below the power stage natural frequency, f_{FILTER_POLE} to avoid a conditional stability. When setting these two zeroes (fz1 and fz2), converter performance and stability margin should be considered.
(7) Select the compensator parameters. (R's and C's)

To meet the design standards mentioned above, Figure 18 shows circuits and the characteristics of a typical compensator, which has a controller structure with two zeroes (fz1 and fz2) and poles (fp1 and fp2).

First of all to design an error amplifier, natural frequency of system, f_{FILTER_POLE} and ESR zero using an equivalent series resistance of the output capacitor can be obtained by the following formula.

Double poles by the output filter are obtained from the following formula:

$$f_{FILTER\_POLE} = \frac{1}{2\pi\sqrt{LC_O}}[Hz]$$

Where, Co is the output capacitor.

The ESR zero by the output capacitor, C_O and equivalent series resistance of the output capacitor, R_{ESR} can be obtained by the following formula.

$$f_{FILTER\_ZERO} = \frac{1}{2\pi \times R_{ESR} \times C_O}[Hz]$$

where, R_{ESR} is the equivalent series resistance of output filter capacitor.

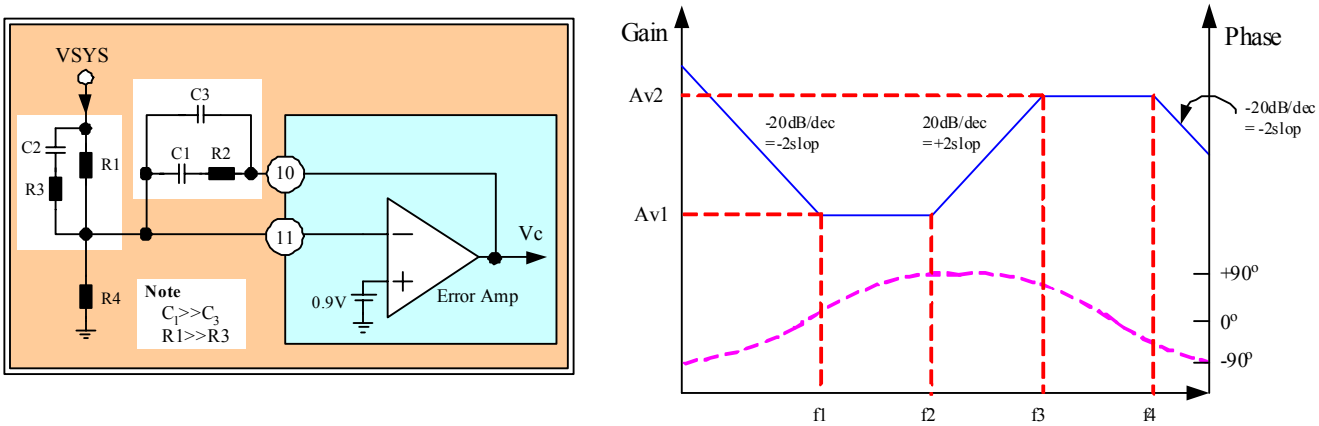


Figure 18. Error Amplifier Compensation Circuit

A troublesome feature in boost converter mode is the right-half plan (RHP) zero, and is given by:

$$f_{RHPZ} = \frac{V_{IN}^{\ 2}}{2\pi \times I_O \times L}[Hz]$$

.Most applications demand an improved transient response to allow a smaller output filter capacitor, and to achieve a higher bandwidth, type 3 compensation is required. In Figure 18, pole and zero of the error amplifier are expressed as follows:

$$f_I = \frac{1}{2\pi \times R1 \times (C1 + C3)}[Hz]$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}[Hz]$$

$$f_{Z2} = \frac{1}{2\pi \times C2(R1 + R3)}[Hz]$$

$$f_{P1} = \frac{1}{2\pi \times R3 \times C2}[Hz]$$

$$f_{P2} = \frac{1}{2\pi \times R2 \times \frac{C1 \times C3}{C1 + C3}}[Hz]$$

And because it has C1 >> C3 and R1 >> R3 in general, it can be simplified as below:

$$f_I = \frac{1}{2\pi \times R1 \times C1}[Hz]$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1}[Hz]$$

$$f_{Z2} = \frac{1}{2\pi \times R1 \times C2}[Hz]$$

$$f_{P1} = \frac{1}{2\pi \times R3 \times C2}[Hz]$$

$$f_{P2} = \frac{1}{2\pi \times R2 \times C3}[Hz]$$

3-12. Considerations of Input and Output Capacitors in DC-DC converter

Input Capacitors

The input capacitor is necessary to minimize the peak current drawn from the battery. Typically a several ten times uF tantalum capacitor is recommending. Low equivalent series resistance (ESR) capacitors will help to minimize battery voltage ripple.

Output Capacitors

Low ESR capacitors should be used at the output of the DC-DC converter to minimize output ripple. The high frequency switching speeds and fast changes in the output capacitor current, mean that the equivalent impedance of the capacitor can contribute greatly to the output ripple. In order to minimize these effects choose an output capacitor with less than 10nH of equivalent series inductance (ESL) and less than 100mW of equivalent series resistance (ESR). Typically these characteristics are met with ceramic capacitor, but may also be met with certain types of tantalum capacitor. For a step change of load, the output filter inductor in Figure 19 acts as a source of constant current during in this load transient, and the change in load current as a transient is supplied by the filter capacitor. Hence, following a load transient,

$$\Delta V_{SYS} = -ESR \times \Delta I_{SYS}$$

3-13. Layout and Ground Considerations

High frequency switching and large peak currents means PCB design for DC-DC converters requires careful consideration. A general rule is to place the DC-DC converter circuitry well away from any sensitive RF or analog components. The layout of the DC-DC converters and its external components are also based on some simple rules to minimize EMI and output voltage ripple.

Layout

1. Place all power components, FAN8048, inductor, input capacitor and output capacitor as close together as possible.
2. Keep the output capacitor as close the FAN8048 as possible with very short traces to the VSYS and GND pins.
3. Keep the external feedback loop network as close the FAN8048 as possible with very short traces, but away from the four channels output as far as possible.

Grounding

1. Use a star grounding system with separate traces for the power ground and the low power signals such as ON/OFF and MUTE. The star should radiate from where the power supply enters the PCB.
2. On the multilayer boards use components side copper for grounding around the FAN8048 and connect back to a quiet ground plane using vias.

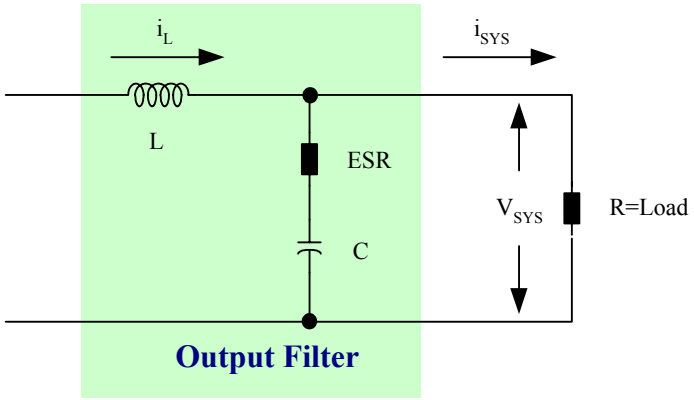


Figure 19. ESR in the output capacitor

4. Series Voltage Regulator and Battery Charger Function

As shown in Figure 20, if the external adaptor supplies high voltage (in general, adaptor voltage used for portable devices is above 4.5V), the series voltage regulator is internally designed to be 4V so as to be suitable for circuit operation; and when necessary, it has the function of battery charging using an external adaptor.

4.1 Non-charging mode (Series Voltage Regulator Function)

When battery-charging mode is unnecessary, CHGSW (pin27) input may be LOW. On this occasion, the output voltage VREG (Voltage on pin18) of the series voltage regulator is internally designed to be 4.0V.

When DCIN(pin24) is not supplied (when VIN is connected from the batteries), this circuit is need diode(D1) for prevent the VIN (Volatege on pin18) leakage current can not flow in to the IC.

The related formula for this is expressed as follows:

$$V_{REG} = ((1 + \frac{R1}{R2}) \times 0.5) - V_{Q1,SAT} = 4[V]$$

4.2 Charging mode (Battery Charger function)

To charge the battery using an external adaptor, CHGSW (pin27) input should be HIGH. In charging mode, internal transistor Q1 and external transistor Q3 are turned-on to connect the battery with the external adaptor.
On this occasion, charging current, i_{CHG} can be determined by current detection resistance Rs, and charging current is obtained by the following formula:

$$I_{CHG} = \frac{0.5}{R_S}[A]$$

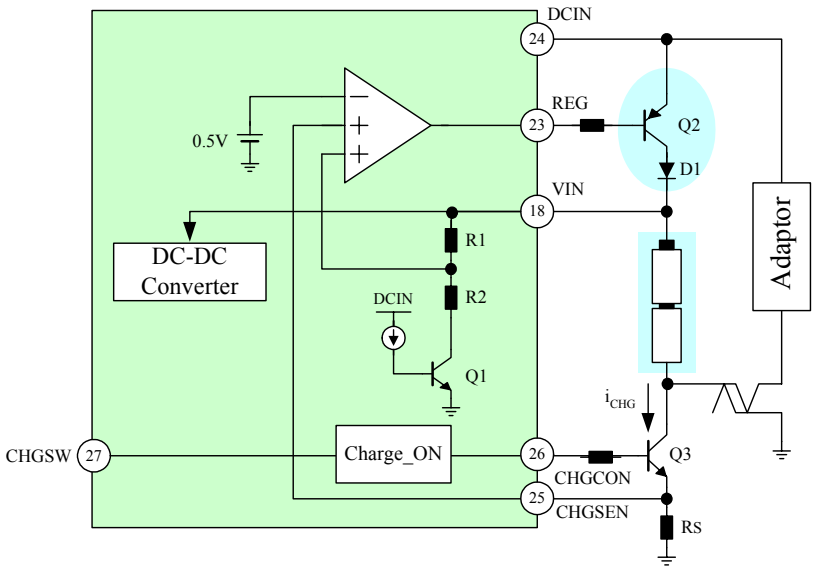


Figure 20. Block Diagram of Regulator and Battery charger

5. Precaution

1. Attach a de-coupling capacitor between power supply pins and ground.

2. Check that the following items will not result while this IC is in use, or otherwise the IC will be broken or burned with smoke generated.

   -. Short-circuiting between output pins
   -. Short-circuiting between output and ground pins
   -. Short-circuiting between output and power supply pins
   -. Reverse insertion of IC

The following pins are all output pins.

VG(pin1), RST(pin2), EA1O(pin10), EA2O(pin12), VSYS2(pin14), USW2(pin15), DSW2(pin17), DSW1(pin19), USW1(pin21), VSYS1(pin22), REG(pin23), CHGCON(pin26), CH4-(pin38), CH4+(pin39), CH3-(pin40), CH3+(pin41), CH2-(pin43), CH2+(pin44), CH1-(pin45) and CH1+(pin46)

The following pins are all ground pins.

SGND(pin6), PGND(pin16), PGND(pin20), DGND(pin28), PGND(pin37) and PGND(pin47)

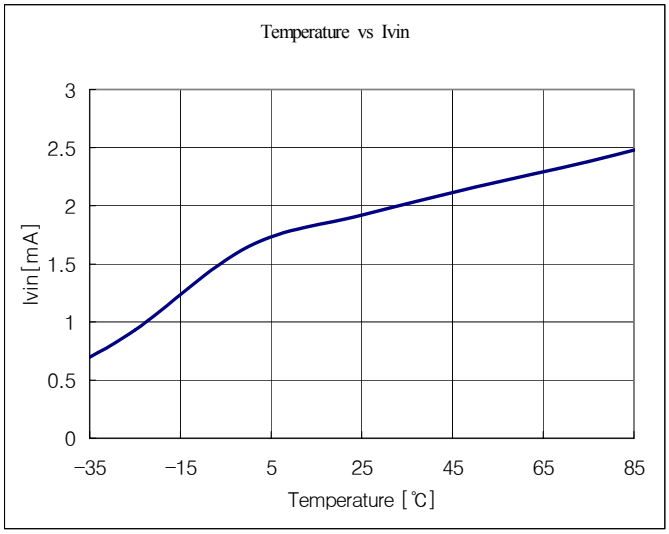
The following pins are all power supply pins.

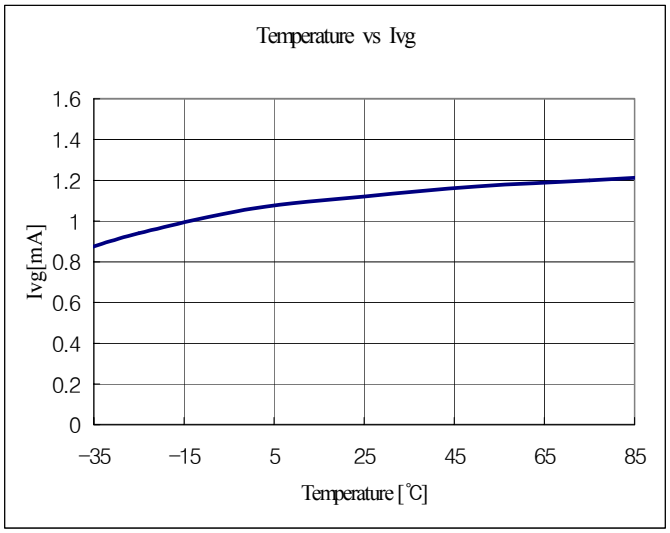
VIN(pin18), DCIN(pin24) and PVCC(pin42)

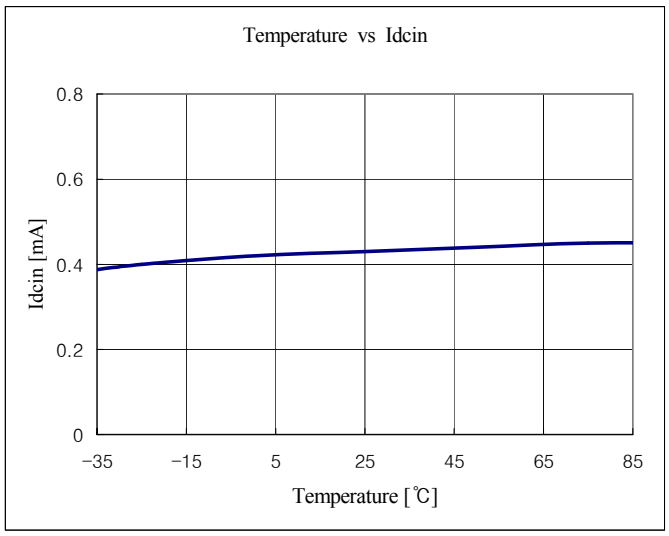
Note)

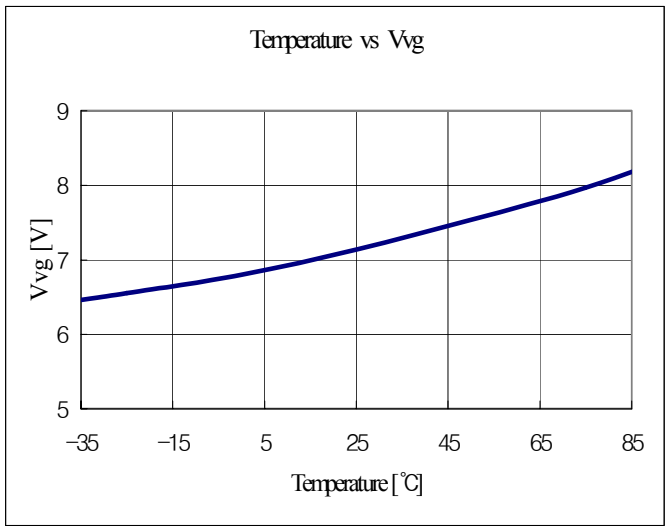
This document provides reference information on the use of this IC, which does not, however, guarantee the proper operation of any applications employing this IC. Constantly or values provided in this document are reference values and not guaranteed values.

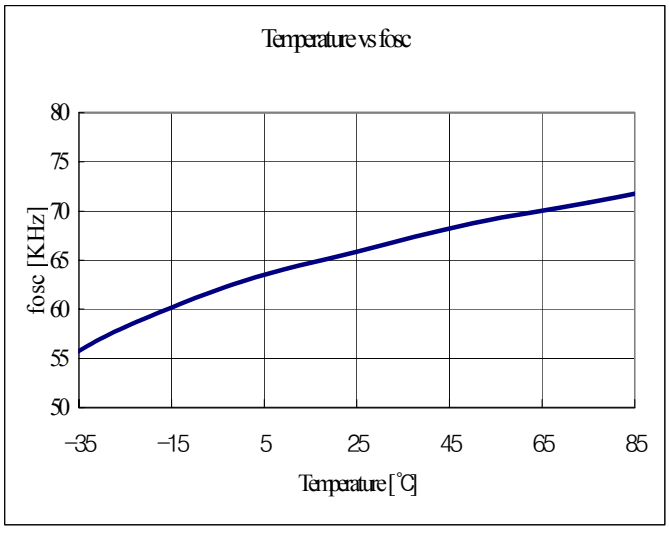
Typical Performance Characteristics

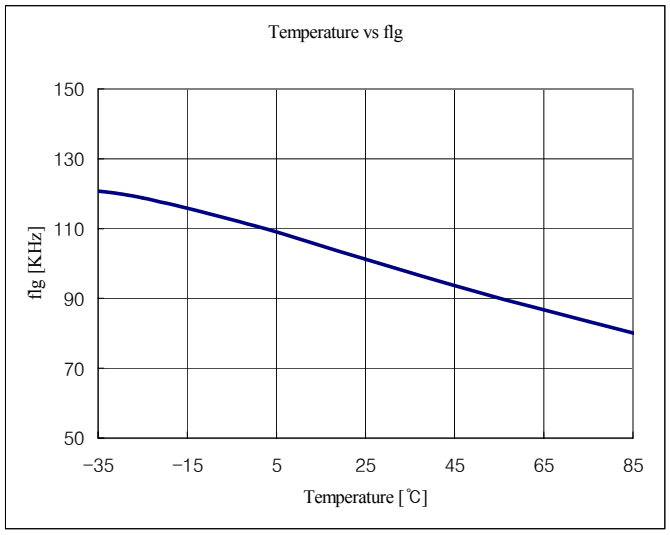




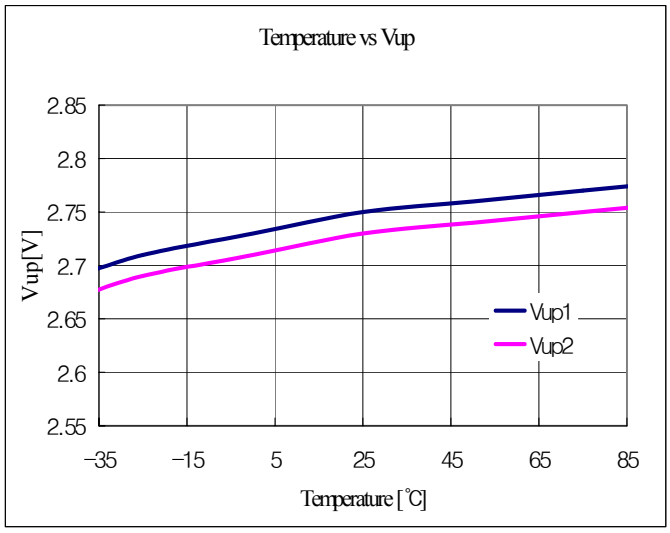


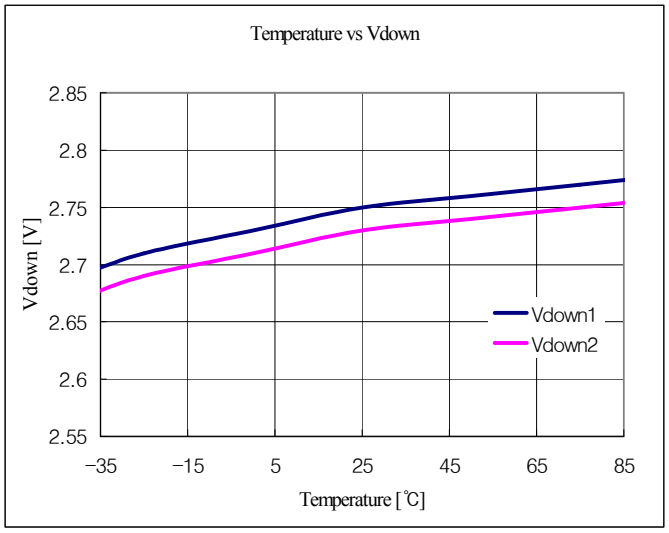


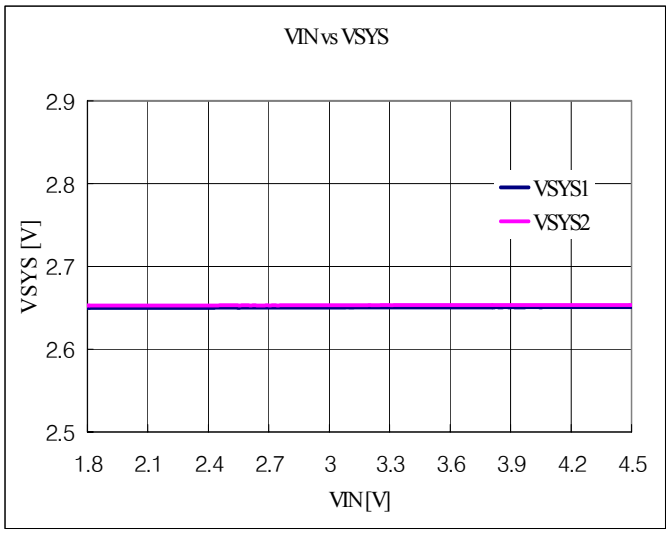


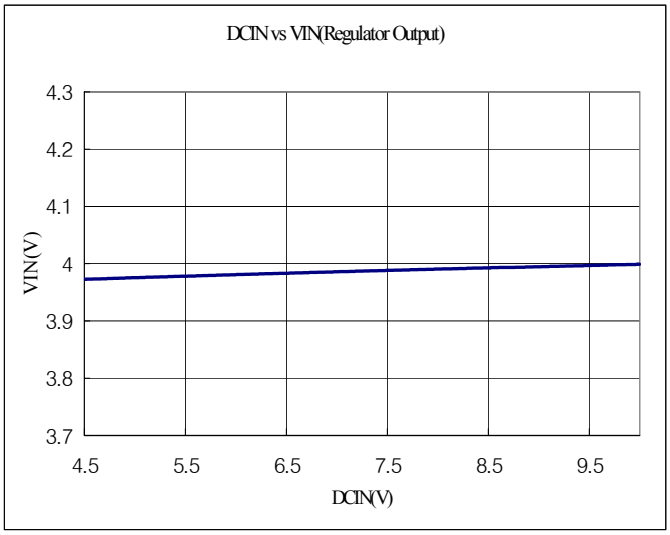


Typical Performance Characteristics

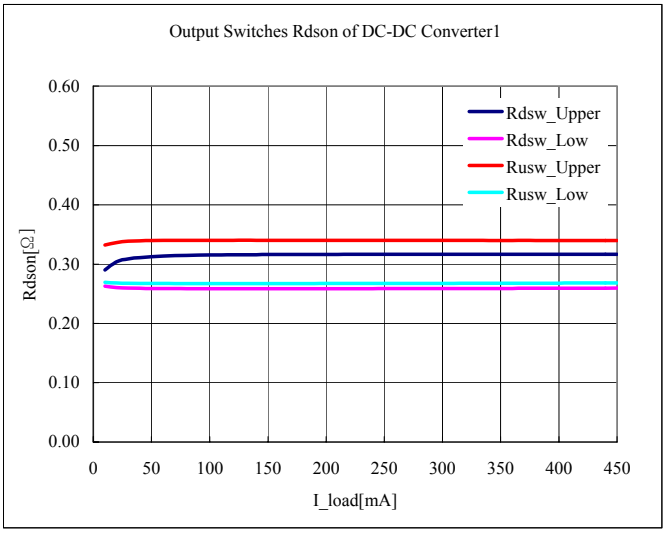


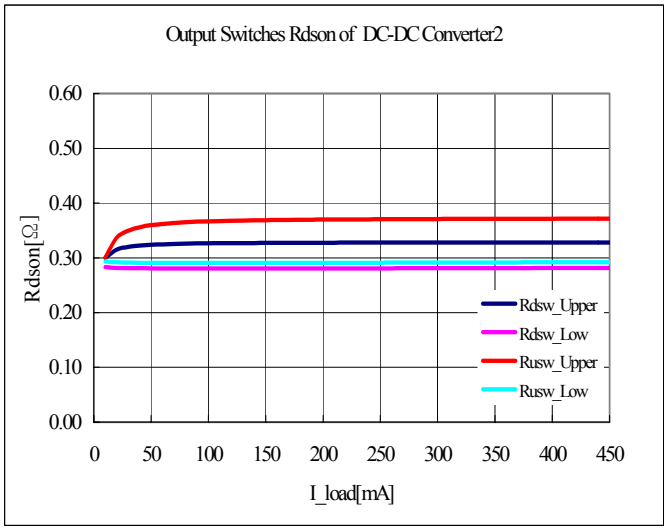


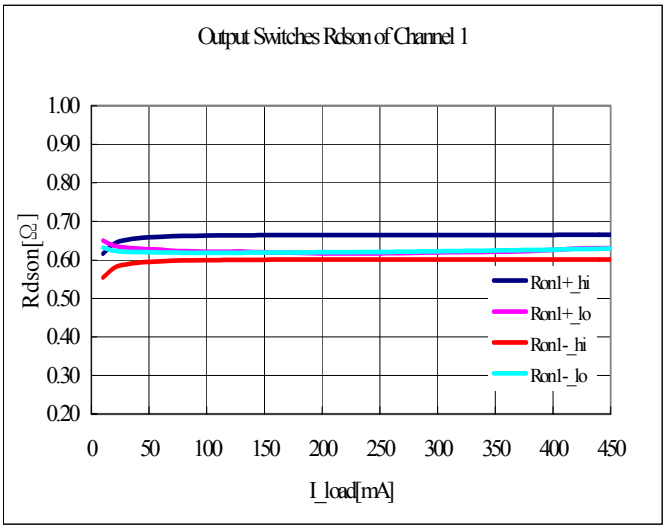


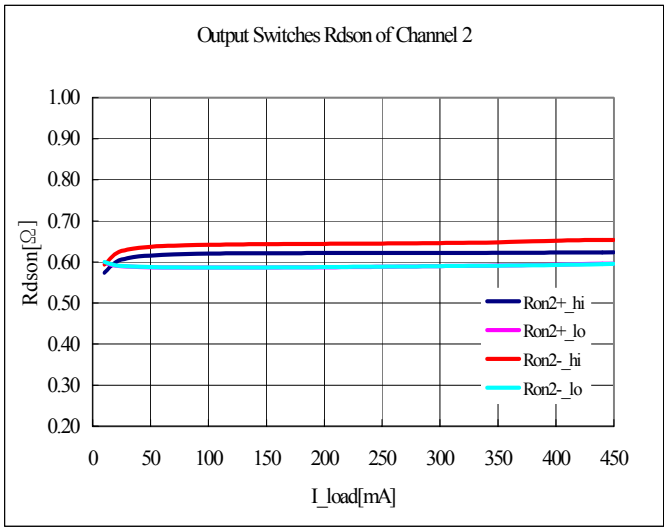


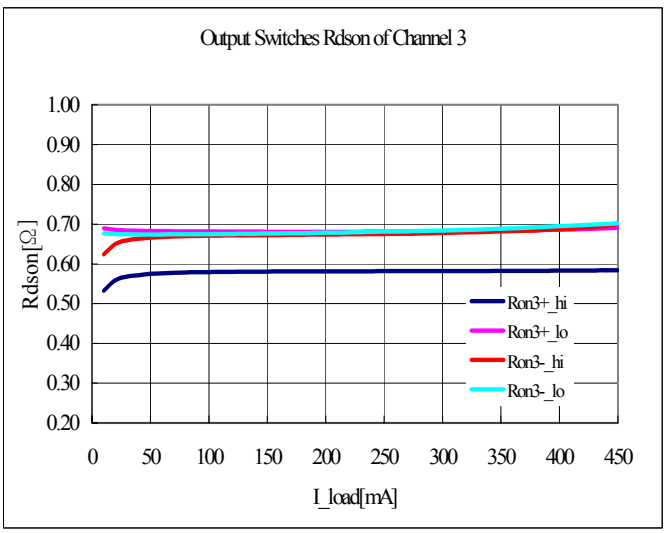
Typical Performance Characteristics (Continued)

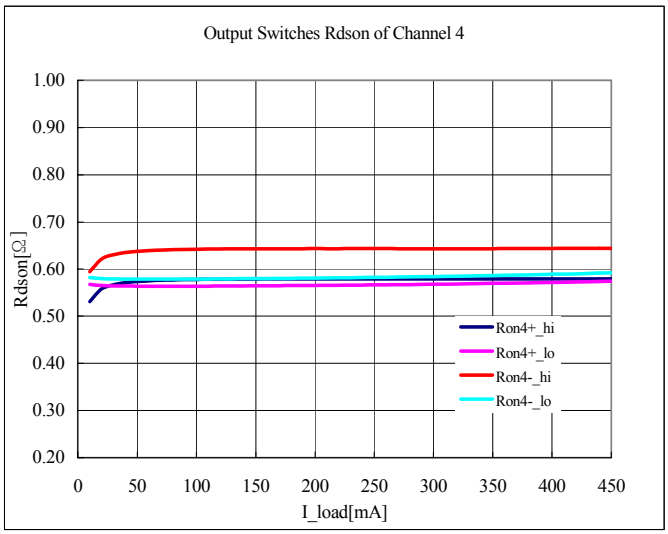




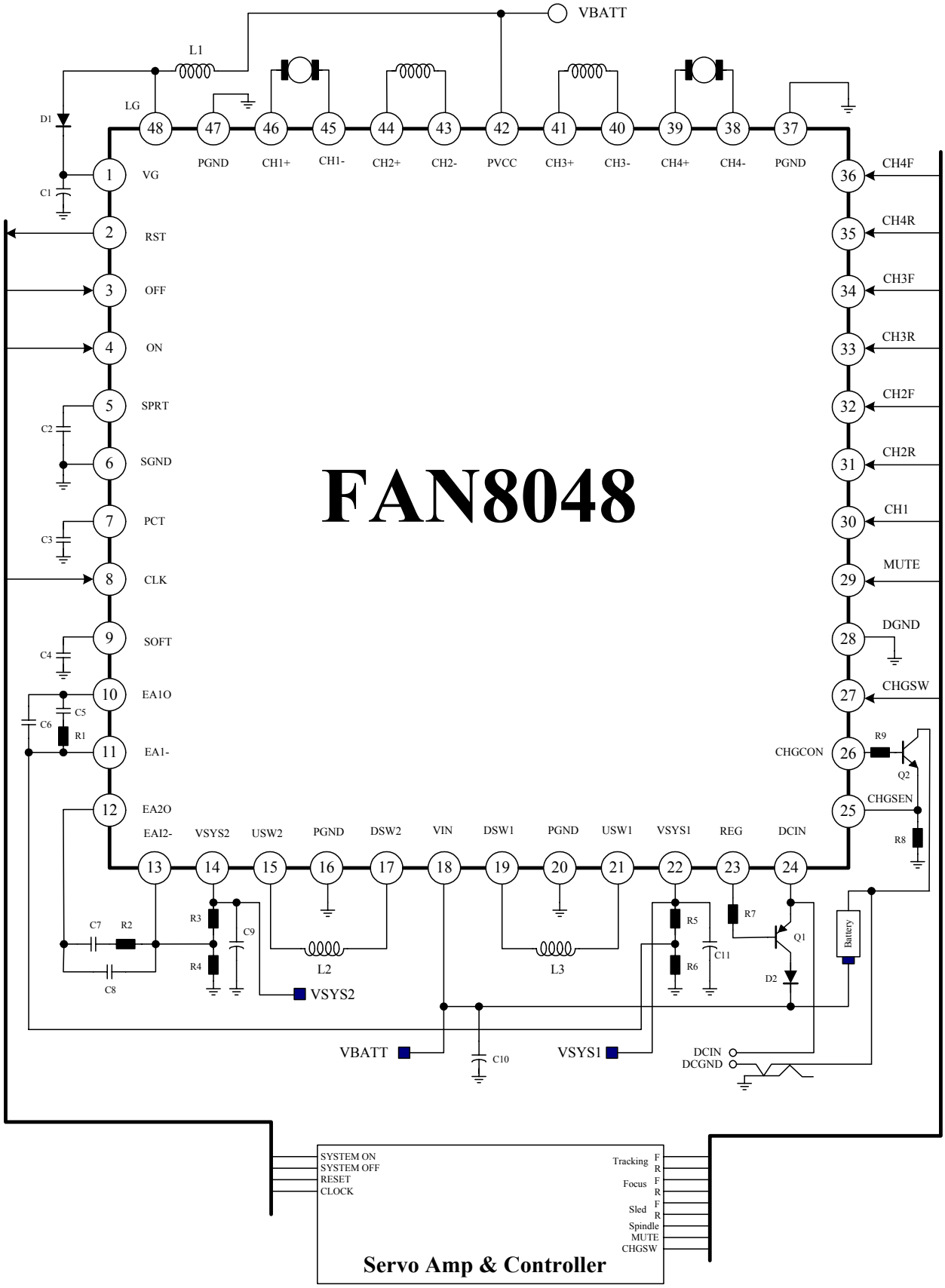






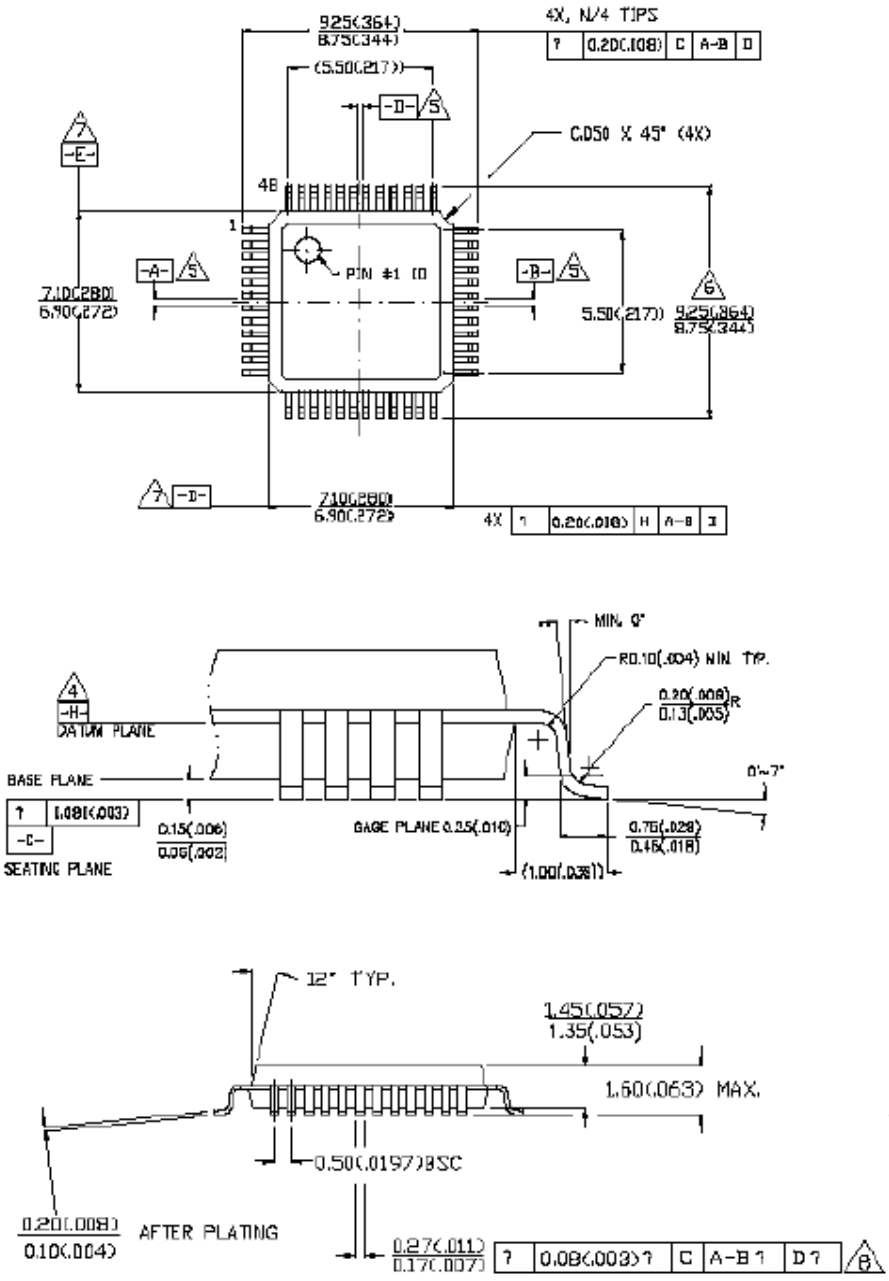


Typical Application Circuits



Package Dimensions

48-LQFP-0707



DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.