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FAN8400D (FAN8400BD3)

3-Phase BLDC Motor Driver with PLL

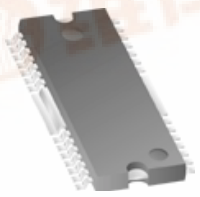
Features

- 3-Phase BLDC motor driver IC with speed control
- Phase Locked Loop (PLL) speed control
- Built-in phase locked detector output
- Current linear drive scheme
- External clock for arbitrary motor speed
- Built-in FG amplifier and integrating amplifier
- Auto Gain Control (AGC) circuit for compensation hall amplifier
- Built-in protection circuits (over-current limit, under voltage limit, thermal shut down)

Description

The FAN8400D is a monolithic integrated circuit. it is one driver for laser beam printer (LBP) polygon mirror motor, which has single chip implementation of all circuits. For extremely high rotational precision, it employs the phase locked loop (PLL) speed control scheme.

28-SSOPH-375SG2



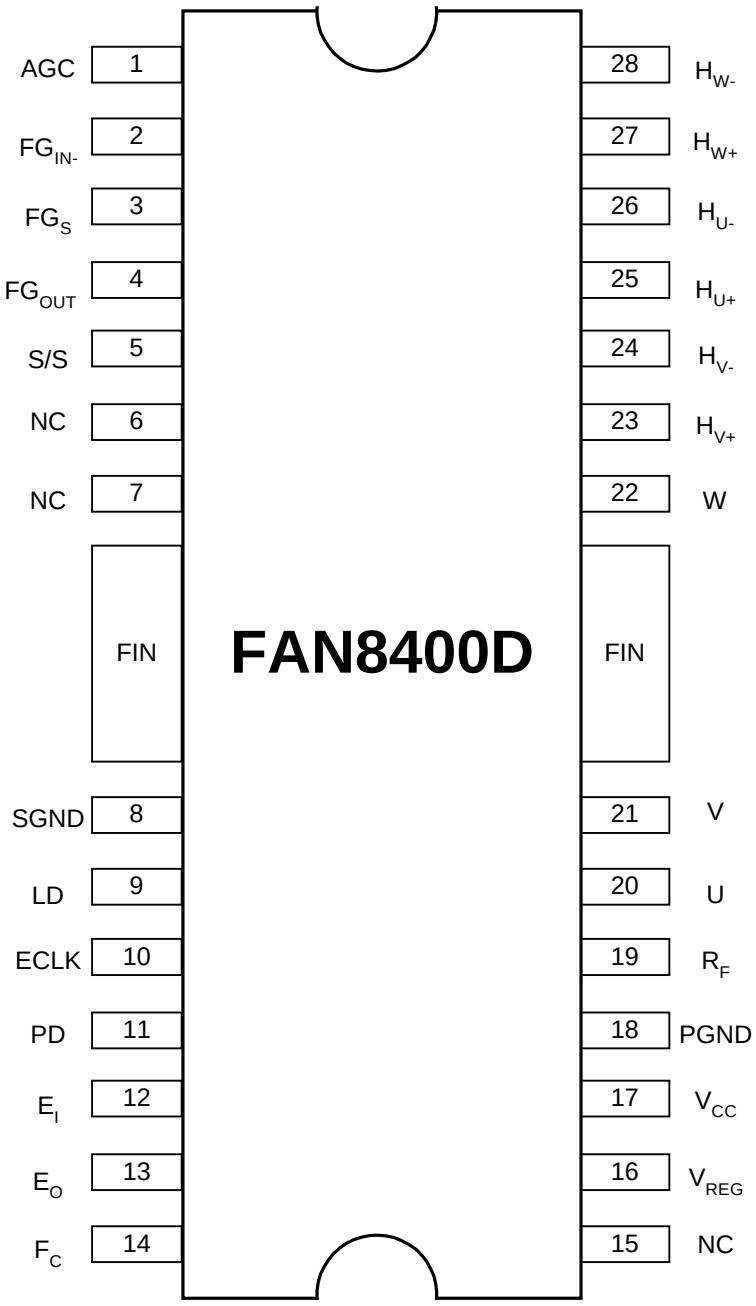
Typical application

- Polygon mirror motor drive IC for laser beam printer
- Polygon mirror motor drive IC for facsimile
- Polygon mirror motor drive IC for duplicator
- Polygon mirror motor drive IC for multi function printer
- General 3 phase BLDC motor drive IC

Ordering Information

Device	Package	Operating Temp
FAN8400BD3	28-SSOPH-375SG2	–20°C ~ +80°C
FAN8400BD3TF	28-SSOPH-375SG2	–20°C ~ +80°C

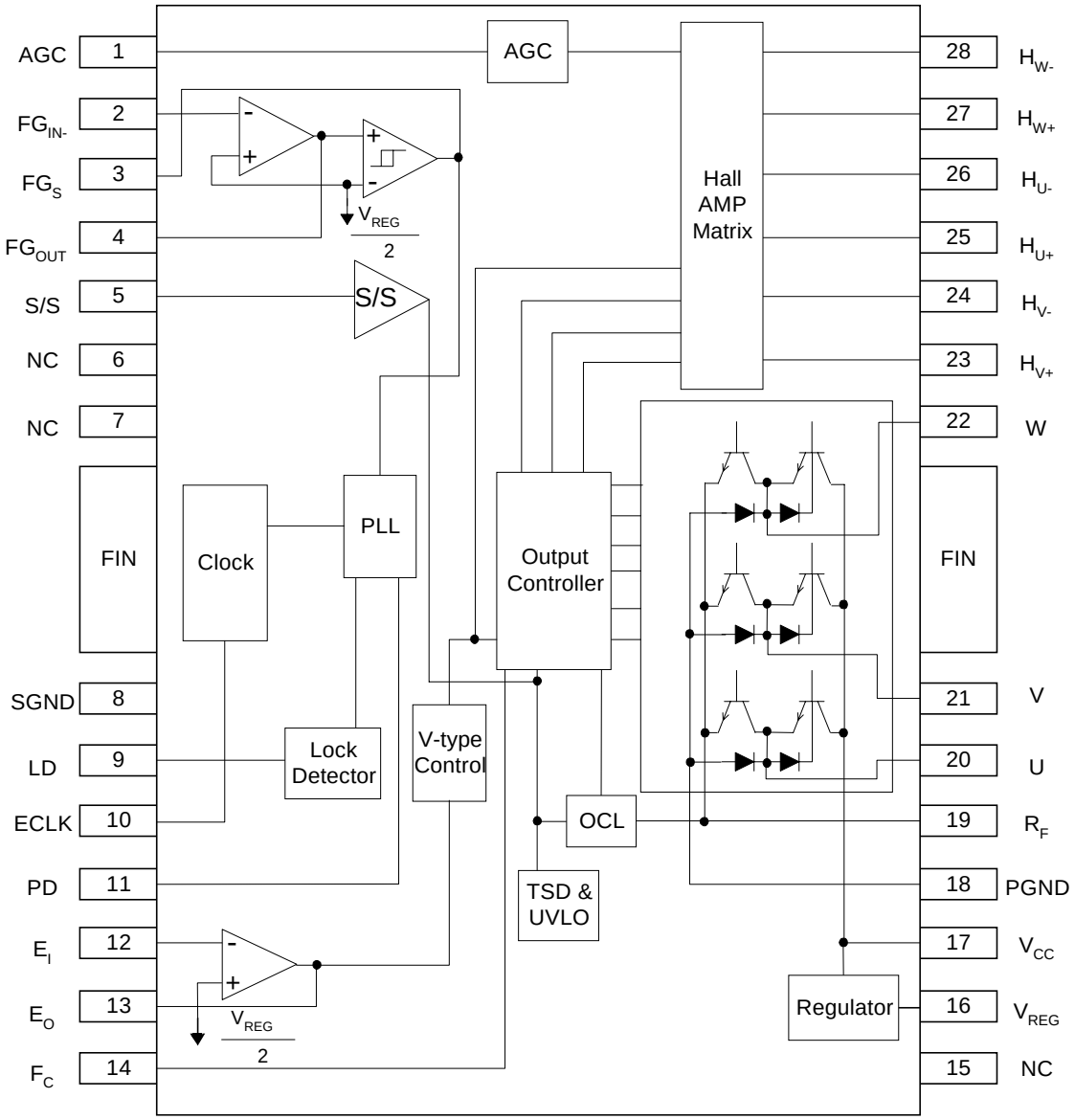
Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	AGC	AGC amplifier frequency characteristics correction
2	FG_{IN-}	FG amplifier inverting input
3	FG_S	FG pulse output
4	FG_{OUT}	FG amplifier output
5	S/S	Stop and start
6	NC	-
7	NC	-
8	SGND	Signal ground
9	LD	Phase locked loop detector output
10	ECLK	External clock
11	PD	Phase locked loop detector output
12	E_I	Error amplifier inverting input
13	E_O	Error amplifier output
14	F_C	Control amplifier frequency correction
15	NC	-
16	V_{REG}	Regulator voltage stabilization output
17	V_{CC}	Power supply
18	PGND	Power ground
19	R_F	Output current detection
20	U	U output
21	V	V output
22	W	W output
23	H_{V+}	V hall amplifier non inverting input
24	H_{V-}	V hall amplifier inverting input
25	H_{U+}	U hall amplifier non inverting input
26	H_{U-}	U hall amplifier inverting input
27	H_{W+}	W hall amplifier non inverting input
28	H_{W-}	W hall amplifier inverting input

Internal Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit	Remark
Maximum supply voltage	V_{CCMAX}	30	V	-
Maximum output current	I_{OMAX}	0.6	A	-
Power dissipation	Pd	1.7	W	-
Operating temperature	T_{OPR}	–20 ~ +80	°C	-
Storage temperature	T_{STG}	–50 ~ +150	°C	-

Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating voltage range	V_{CC}	20	24	28	V

Electrical Characteristics (Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
POWER SUPPLY CURRENT						
Low power supply current	I_{CCL}	Stop mode, V_{CC}=20V	20	30	40	mA
Typical power supply current	I_{CCT}	Stop mode, V_{CC}=24V	21	31	41	mA
High power supply current	I_{CCH}	Stop mode, V_{CC}=28V	22	32	42	mA
OUTPUT POWER TRANSISTOR CHARACTERISTICS (V_{AGC} = 3.5V)						
U source saturation voltage (1)	V_{SATUU1}	I_O=0.6A, R_F=0Ω	-	1.8	2.5	V
U source saturation voltage (2)	V_{SATUU2}	I_O=0.3A, R_F=0Ω	-	1.6	2.3	V
U sink saturation voltage (1)	V_{SATUL1}	I_O=0.6A, R_F=0Ω	-	0.5	1.0	V
U sink saturation voltage (2)	V_{SATUL2}	I_O=0.3A, R_F=0Ω	-	0.25	0.7	V
V source saturation voltage (1)	V_{SATVU1}	I_O=0.6A, R_F=0Ω	-	1.8	2.5	V
V source saturation voltage (2)	V_{SATVU2}	I_O=0.3A, R_F=0Ω	-	1.6	2.3	V
V sink saturation voltage (1)	V_{SATVL1}	I_O=0.6A, R_F=0Ω	-	0.5	1.0	V
V sink saturation voltage (2)	V_{SATVL2}	I_O=0.3A, R_F=0Ω	-	0.25	0.7	V
W source saturation voltage (1)	V_{SATWU1}	I_O=0.6A, R_F=0Ω	-	1.8	2.5	V
W source saturation voltage (2)	V_{SATWU2}	I_O=0.3A, R_F=0Ω	-	1.6	2.3	V
W sink saturation voltage (1)	V_{SATWL1}	I_O=0.6A, R_F=0Ω	-	0.5	1.0	V
W sink saturation voltage (2)	V_{SATWL2}	I_O=0.3A, R_F=0Ω	-	0.25	0.7	V
U output leakage current	I_{OLEAKU}	V_{CC}=28V, U=28V	-	-	100	μA
V output leakage current	I_{OLEAKV}	V_{CC}=28V, V=28V	-	-	100	μA
W output leakage current	I_{OLEAKW}	V_{CC}=28V, W=28V	-	-	100	μA
UNDER VOLTAGE LIMIT						
UVLO operating voltage	V_{SD}	-	7.0	7.6	8.2	V
UVLO hysteresis	HV_{SD}	-	1.0	1.3	1.6	V
REGULATOR VOLTAGE OUTPUT						
Regulator output voltage	V_{REG}	-	5.8	6.3	6.8	V
Power supply variation	H_{VREG1}	V_{CC}=20~28V	-	-	100	mV
Load variation	H_{VREG2}	I_{LOAD}=0~10mA	-	-	100	mV
HALL AMPLIFIER INPUT BLOCK						
H_{U+} hall AMP input bias current	I_{BHA1+}	-	-	2	10	μA
H_{U-} hall AMP input bias current	I_{BHA1-}	-	-	2	10	μA
H_{V+} hall AMP input bias current	I_{BHA2+}	-	-	2	10	μA
H_{V-} hall AMP input bias current	I_{BHA2-}	-	-	2	10	μA
H_{W+} hall AMP input bias current	I_{BHA3+}	-	-	2	10	μA
H_{W-} hall AMP input bias current	I_{BHA3-}	-	-	2	10	μA
Hall differential input range	V_{HIN}	Sine wave input	50	-	350	mVp-p
Hall common input range	V_{ICM}	Differential input : 50mVp-p	3.5	-	V_{CC}-3.5	V

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
FG AMPLIFIER BLOCK						
FG AMP. input bias current	I_{BFG}	-	-1	-	1	µA
FG AMP. DC bias level	V_{BFG}	-	2.90	3.15	3.40	V
FG output high level voltage	V_{OHFG}	No external load	V_{REG}-1.1V	-	-	V
FG output low level voltage	V_{OLFG}	No external load	-	0.8	1.2	V
FG SCHMIDT COMPARATOR BLOCK						
FGS high / low input hysteresis	V_{SHL}	-	-50	0	50	mV
FGS low / high input hysteresis	V_{SLH}	-	100	150	200	mV
FGS hysteresis	V_{FGL}	-	100	-	200	mV
FGS input operating level	V_{FGSIL}	-	400	-	-	mVp-p
FGS output saturation voltage	V_{FGSSAT}	I_{FGS}=4mA	-	0.2	0.4	V
FGS output leakage current	$I_{FGSLEAK}$	V_{CC}=28V	-	-	10	µA
ERROR AMPLIFIER BLOCK						
Error AMP. input bias current	I_{BER}	-	-1	-	1	µA
Error AMP. DC bias level	V_{BER}	-	2.90	3.15	3.40	V
Error output high level voltage	V_{OHER}	No external load	V_{REG}-1.1V	-	-	V
Error output low level voltage	V_{OLER}	No external load	-	-	1.0	V
CURRENT LIMIT OPERATION						
R_F output voltage limit	V_{RF}	-	0.55	0.60	0.65	V
CONTROLLER BLOCK						
Dead zone	V_{DZ}	-	50	100	300	mV
Output idle voltage	V_{ID}	-	-	-	5	mV
Forward gain	G_{DF+}	-	0.4	0.5	0.6	-
Reverse gain	G_{DF-}	-	-0.6	-0.5	-0.4	-
Accelerate command voltage	V_{STA}	-	V_{REG}-1.1V	-	-	V
Decelerate command voltage	V_{STO}	-	-	0.8	1.5	V
Forward limit voltage	V_{L+}	R_F=22Ω	-	0.60	-	V
Reverse limit voltage	V_{L-}	R_F=22Ω	-	0.60	-	V
PHASE COMPARATOR OUTPUT BLOCK						
PD output high level voltage	V_{PDH}	No external load	5.2	-	-	V
PD output low level voltage	V_{PDL}	No external load	-	-	0.7	V
PD output source current	I_{PD+}	V_{PD}=0.5*V_{REG}	-	-	-0.6	mA
PD output sink current	I_{PD-}	V_{PD}=0.5*V_{REG}	1.0	-	-	mA
PHASE LOCKED LOOP DETECTOR OUTPUT BLOCK						
LD output saturation voltage	V_{LDSAT}	I_{LD}=5mA	-	0.1	0.4	V
LD output leakage current	I_{LDLEAK}	V_{CC}=28V	-	-	10	µA

Electrical Characteristics (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
EXTERNAL CLOCK INPUT BLOCK						
External input frequency	F_{CLK}	External clock mode	0.5	-	7.0	KHz
ECLK input open voltage	V_{IOCLK}	-	3.7	4.2	4.7	V
ECLK input high level current	I_{IHCLK}	$V_{CLK}=V_{REG}$	100	150	200	µA
ECLK input low level current	I_{ILCLK}	$V_{CLK}=0V$	-400	-300	-200	µA
S/S BLOCK						
S/S input high level voltage	V_{IHSS}	-	3.0	-	V_{REG}	V
S/S input low level voltage	V_{ILSS}	-	0	-	1.5	V
S/S hysteresis	V_{ISSS}	-	0.3	0.5	0.7	V
S/S input open voltage	VIOSS	-	3.7	4.2	4.7	V
S/S input high level current	I_{IHSS}	$V_{SS}=V_{REG}$	100	150	200	µA
S/S input low level current	I_{ILSS}	$V_{SS}=0V$	-400	-300	-200	µA

Application Information

1. Output Block

- 3 Phase power transistor and free wheeling diodes
- Reverse active type upper side diodes and parasitic lower side diodes
- full wave current linear drive with current feedback
- Connection with external capacitor to prevent voltage spike and oscillation by current drive
- Output transistor commutation by "Winner takes all" method
- Built in over current limit (OCL) circuit

2. Hall AMP Block

- Detection of rotor position using 3 phase hall sensors
- Determination of output commutation by hall signal

Hall U	Hall V	Hall W	Forward torque [Reverse torque]		
			Output U	Output V	Output W
H	L	H	L [H]	H [L]	M [M]
H	L	L	L [H]	M [M]	H [L]
H	H	L	M [M]	L [M]	H [L]
L	H	L	H [L]	L [H]	M [M]
L	H	H	H [L]	M [M]	L [H]
L	L	H	M [M]	H [L]	L [H]

3. AGC Block

- This block is remained output amplitude.
- It is controlled by envelope through hall signals.

$$V_{AGC} \propto \frac{1}{H_{NI} - H_I}$$

NOTES:

V_{AGC} is voltage of AGC output.
H_{NI} is hall non inverting input voltage.
H_I is hall inverting voltage.

4. Speed Control Block

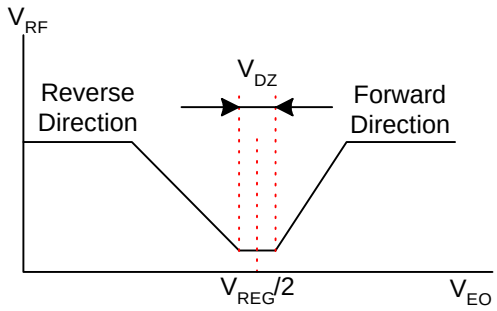
- Digital phase locked loop (PLL) circuit
- Generating error pulse between rising edge of clock and falling edge of FG signal.
- High precision stable speed control

5. FG AMP & FG Schmidt Comparator Block

- This block measures of motor rotation speed and controls motor speed.
- It is determined FG AMP gain and filter by external component.
- FG schmidt block change sine wave form to square wave form

6. Error AMP Block

- It composes of dumping filter and ripple filter by external component.
- It determines output amplitude of error AMP by width error pulse.
- It is determined output current by output amplitude of error AMP.
- Bidirectional torque control



7. Regulator Block

- Power supply of control circuits in inside.
- Band gap reference circuits.

8. Lock Detector

- It is low when FG frequency reaches capture range of clock frequency.
- Open correct

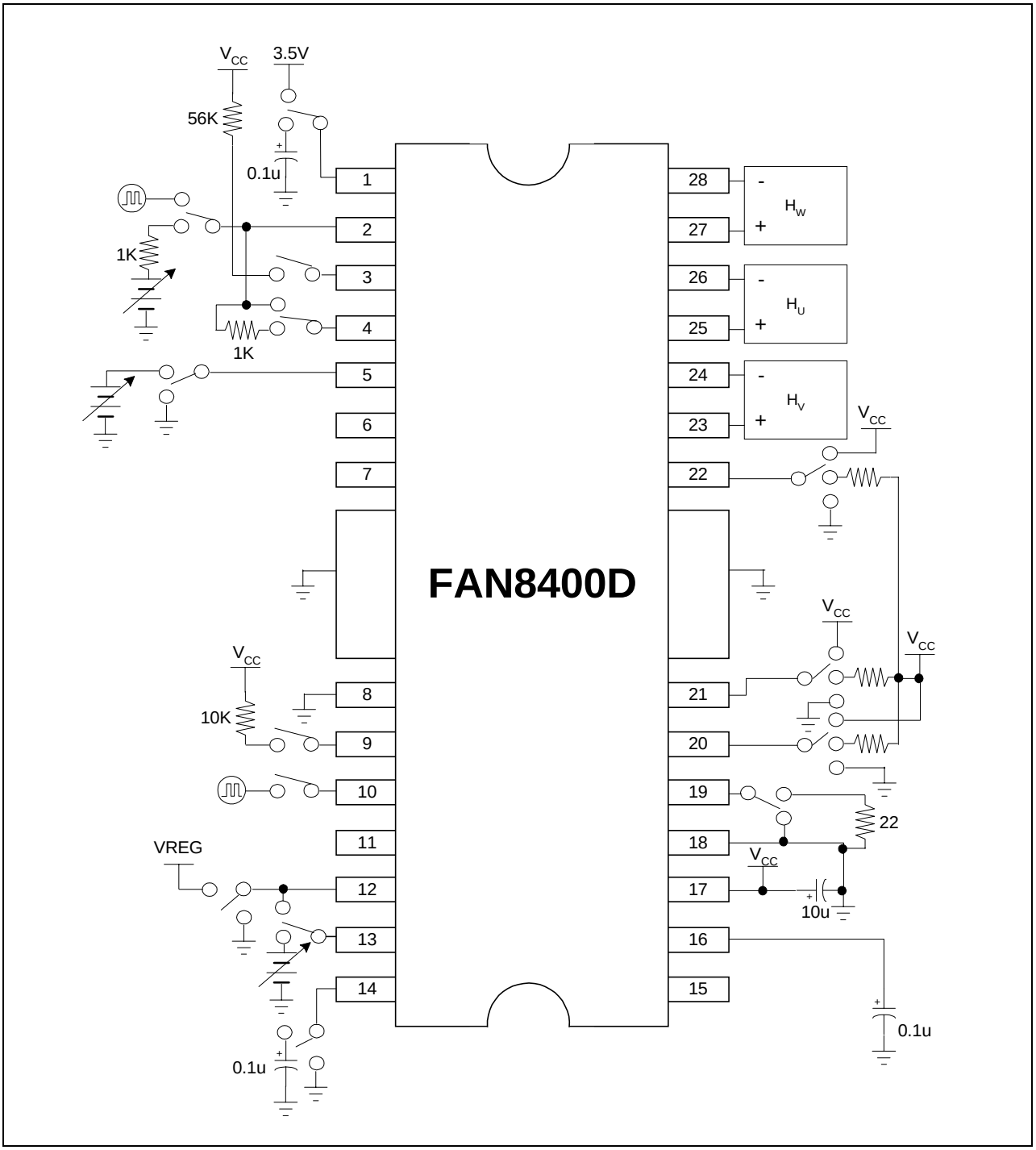
9. FG Pulse Output

- Monitoring pin for motor rotative speed
- Open correct

10. Stop And Start

- Stop mode: Open or high voltage
- Start mode: Low voltage

Test Circuits



Typical Application Circuits