

FAN8460MTC/FAN8460MP

Single Phase Full Wave BLDC Motor Driver with Variable Speed Control

Features

- Output direct PWM drive for speed control
- Selectable PWM frequency : internal or external
- Versatile speed control inputs: A thermistor or PWM input.
- A wide range of operating voltage: 3.2V to 28V
- Locked rotor protection with open collector output and auto retry
- Open collector hall output for speed feedback
- Adjustable minimum speed
- Thermistor disconnection protection
- TSD protection.

Description

The FAN8460MTC/FAN8460MP is a single phase BLDC motor driver with variable speed control using output direct PWM method and it's typical application is DC cooling fans with wide range of supply voltage(5/12/24V). This approach eliminates the need for external pass devices such as BJT, MOSFET. This solution also offers other advantages over commonly used external PWM turning fan's power on and off at fixed frequency. The external PWM increases stress on fan and needs level translation in speed and alarm output because these outputs share the fan's negative terminal. In case of CPU cooling, digital controller can give speed control command with PWM signal adjusting the duty. If a system has no digital controller, the NTC thermistor input mechanism can control fan speed with local or ambient temperature sensing. These two kinds of input schemes can meet various system requirements and applications.

14-TSSOP



14-MLP 4X4



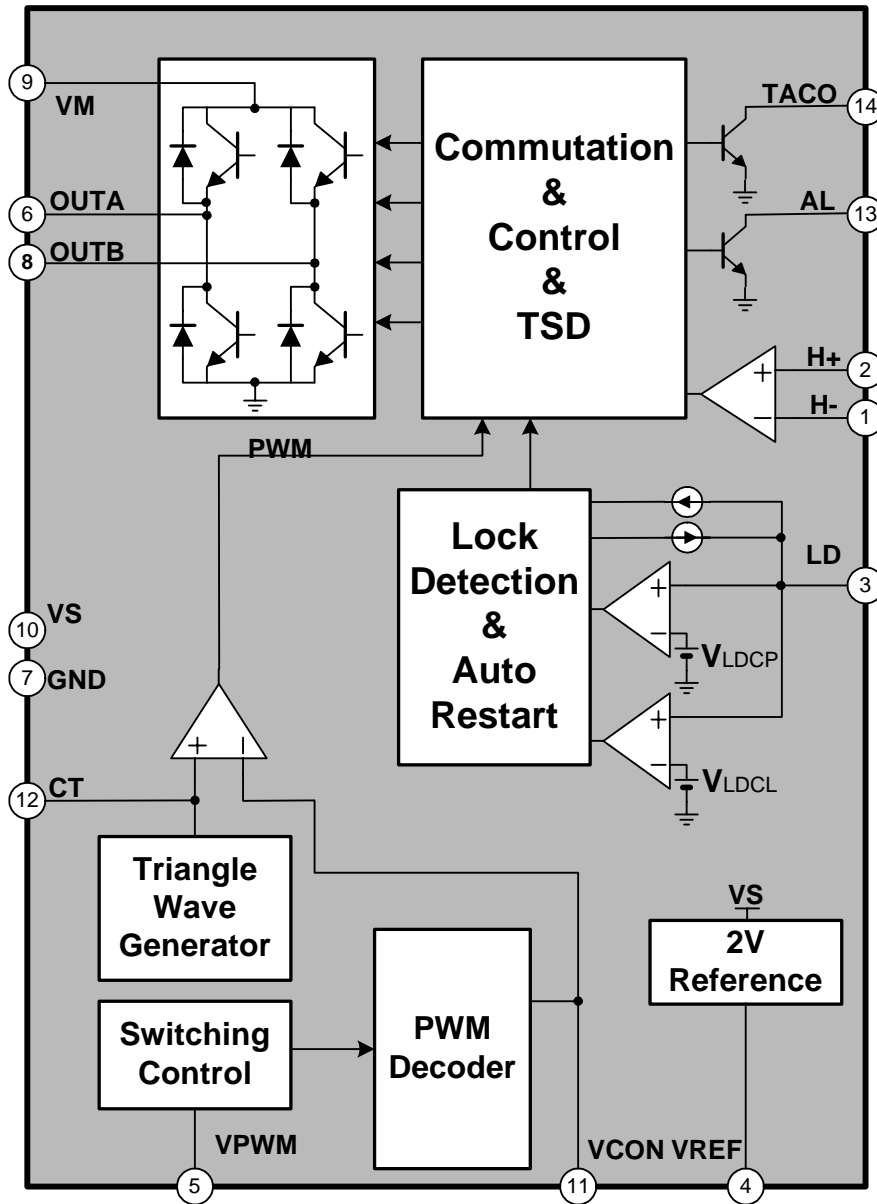
Typical Applications

- CPU Cooling Fans
- Instrumentation Fans
- Desktop PC Fans

Ordering Information

Device	Package	Operating Temp.
FAN8460MTC	14-TSSOP	-30°C ~ 90°C
FAN8460MTCX	14-TSSOP	-30°C ~ 90°C
FAN8460MPX	14-MLP 4x4	-30°C ~ 90°C

Block Diagram

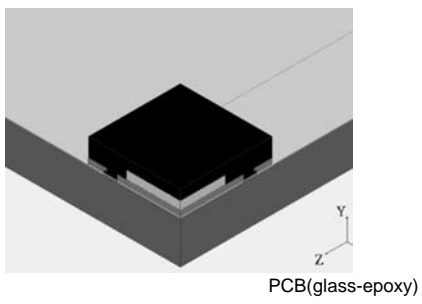
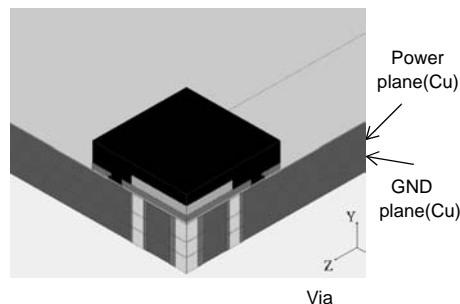


Pin Definitions

Pin Number	Pin Name	I/O	Pin Function Description	Remark
1	H-	A	Hall input -	
2	H+	A	Hall input +	-
3	LD	A	Sawtooth wave generator for lock detector and automatic restart	-
4	VREF	A	Reference voltage output	
5	VPWM	I	PWM input for speed control	-
6	OUTA	A	Motor output A	-
7	GND	P	Ground	-
8	OUTB	A	Motor output B	-
9	VM	P	Power supply for output stage	-
10	VS	P	Power supply for signal block	
11	VCON	A	Speed control signal	
12	CT	A	Triangle waveform out	-
13	AL	O	Alarm output	Open collector
14	TACO	O	Speed output	Open collector

Absolute Maximum Ratings (Ta = 25°C)

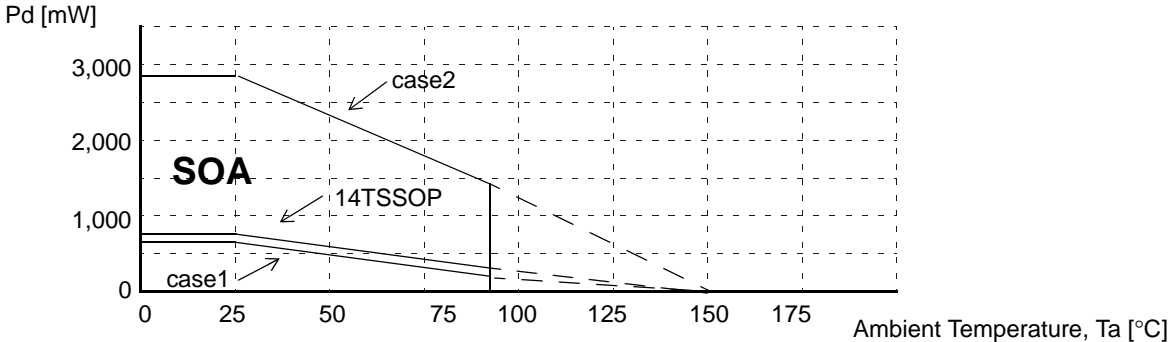
Parameter	Symbol	Value	Unit
Maximum power supply voltage	VSMAX, VMMAX	32	V
Thermal resistance	Rja	143 (FAN8460MTC)	°C/W
		150 (FAN8460MP case1)	°C/W
		45 (FAN8460MP case2)	°C/W
Maximum power dissipation	PDMAX	870 (FAN8460MTC)	mW
		800 (FAN8460MP case1)	mW
		2700 (FAN8460MP case2)	mW
Maximum output voltage	VOMAX	36	V
Maximum output current	IOMAX	0.8 ^{note}	A
Maximum output peak current	IOPEAK	1.2 ^{note}	A
Maximum Taco/Alarm output current	ITACO/AL	5	mA
Taco/Alarm output sustain voltage	VTACO/AL	36	V
Hall output withstanding voltage	VHO	36	V
VPWM Input voltage	VVPWM	-0.3~ VS	V
Operating temperature	TOPR	-30 ~ 90	°C
Storage temperature	TSTG	-55 ~ 150	°C

Case 1	Case 2	Remark
 <p style="text-align: center;">Pd= 0.8W</p>	 <p style="text-align: center;">Pd= 2.7W</p>	Pd is measured base on the JEDEC/STD(JESD 51-2)

note :

1. Refer: EIA/JESD 51-2 & EIA/JESD 51-3 & EIA/JESD 51-5 & EIA/JESD 51-7
2. Case 1: Single layer PCB with 1 signal plane only, PCB size 76mm × 114mm × 1.6mm.
3. Case 2: Multi layer PCB with 1 signal, 1 power and 1 ground planes, PCB size 76mm × 114mm × 1.6mm, Cu plane sizes for power and ground 74mm × 74mm × 0.035mm, thermal via hole pitch 0.9mm, via hole φ size 0.3mm, 6 via hole.
4. Should not exceed Pd or ASO value.
5. IOPEAK time is within 2us.

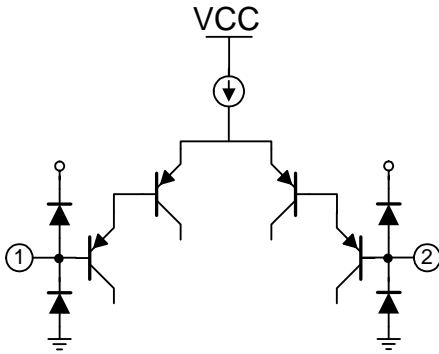
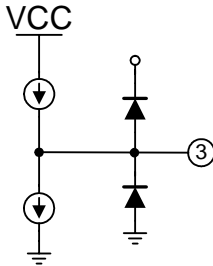
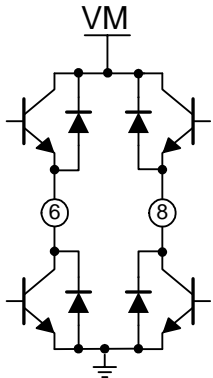
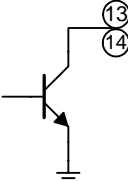
Power Dissipation Curve



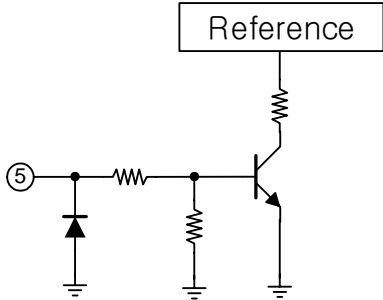
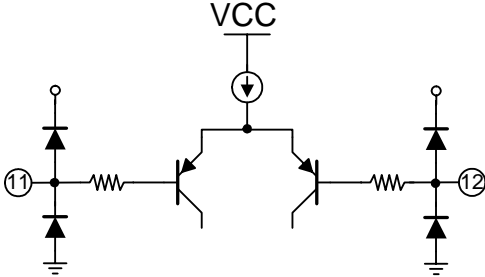
Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage for signal block	VS	3.2	–	28	V
Supply voltage for output stage	VM	3.2	–	28	V

Equivalent Circuits

Description	Pin No.	Internal Circuit
Hall input	1, 2	
LD	3	
Output	6, 8	
AL/TACO	13, 14	

Equivalent Circuits

Description	Pin No.	Internal Circuit
<p>VPWM</p>	<p>5</p>	
<p>VCON/CT</p>	<p>11/12</p>	

FAN8460MTC/FAN8460MP Electrical Characteristics

(Ta = 25°C, VS = 12V unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Common Block						
Supply current	ICC		-	4.5	7	mA
Reference output voltage	VREF1	Iref=200uA	1.85	2.0	2.15	V
Reference output voltage	VREF2	Iref=2mA	1.75	1.94	2.13	V
Lock Detector & Auto Restart						
LD charging current	ILDCL	VLD=0V-->1.5V, VLD=1.5V	1.4	2.2	2.9	μA
LD discharging current	ILDD	VLD=3V-->1.5V, VLD=1.5V	0.15	0.33	0.50	μA
LD clamp voltage	VLDCL	-	2.3	2.6	2.9	V
LD comparator voltage	VLDCLP	-	0.4	0.6	0.8	V
Triangle Wave Generator						
CT discharging current	ICTD	VCT=2.0V-->1.2V, VCT=1.2V	-7.2	-6	-4.8	μA
CT charging current	ICTC	VCT=0.5V-->1.2V, VCT=1.2V	4.8	6	7.2	μA
CT valley voltage	VCTMIN	-	0.71	0.8	0.89	V
CT peak voltage	VCTMAX	-	1.7	1.8	1.9	V
Speed Control Voltage						
VCON output current	IVCON	VVCON=2V, PWM=H	180	200	220	μA
Output OFF VCON low voltage	VCONL		-	-	300	mV
VPWM Input						
VPWM low Voltage	VPWML			-	0.5	V
VPWM high Voltage	VPWMH		2.8	-	-	V
VPWM input current	IPWML	VVPWM=5V	-	70	100	μA
Output Stage						
High side output saturation voltage	VOSH	IO=200mA	-	0.9	1.1	V
Low side output saturation voltage	VOSL	IO=200mA		0.2	0.3	V
Speed output (TACO) & Lock Detection Output (AL)						
TACO output saturation voltage	VTACOS	ITACO=5mA	-	0.1	0.3	V
TACO output leakage current	ITACO	VTACO=12V	-	0.1	10	μA
AL output saturation voltage	VALS	I _{AL} =5mA	-	0.1	0.3	V
AL output leakage current	I _{AL}	V _{AL} =12V	-	0.1	10	μA
Hall Amplifier						
Input range	V _{HDC}	-	0	-	V _S -2.8	V
Input offset	V _{HOF}	-	-10	-	10	mV

Application Information

1 Direct output PWM for FAN Motor Speed Control

Direct output PWM method is used to control driving power to a fan motor and thus fan motor speed. A motor current, and thus fan motor speed is proportional to duty-cycle of output PWM signal in FAN8460MTC/FAN8460MP. The internal PWM signal is driven by comparing a triangle wave (PWM oscillator output, V_{CT}) and a control DC voltage V_{VCON}). Figure.1 illustrates the relationships among oscillator output (V_{CT}), speed control voltage (V_{VCON}), motor current, and output PWM duty.

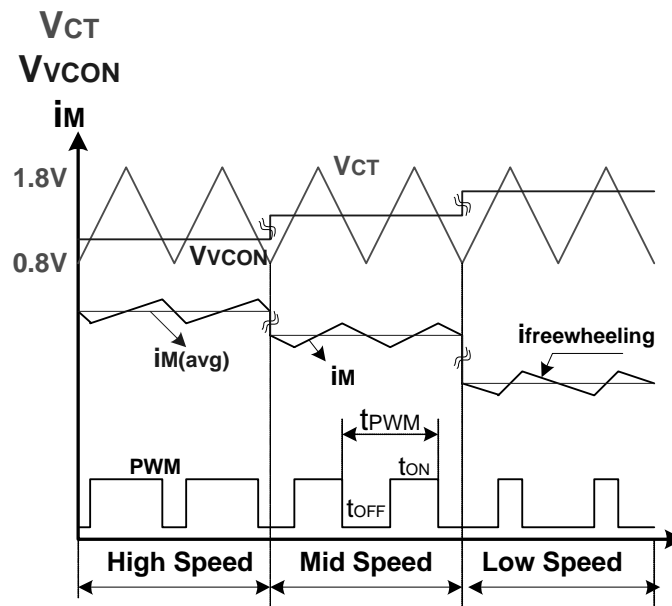


Figure 1. Basic Speed Control Concept

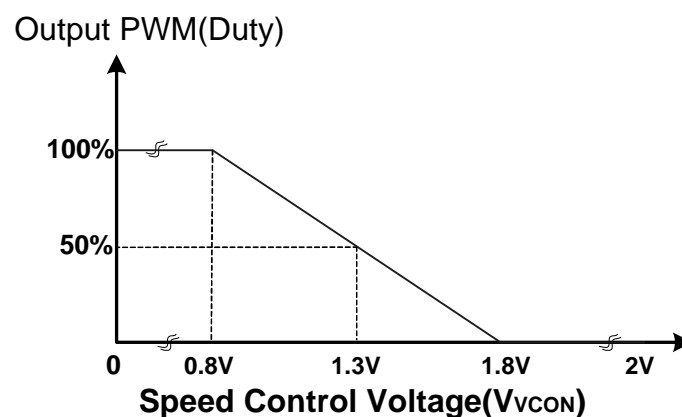


Figure 2. The Relationship Between Speed Control Voltage and Output PWM Duty

As shown in figure2, the output PWM duty-cycle can be decreased as V_{VCON} is increased. The effective range of speed control voltage (V_{VCON}) is 0.8 ~1.8V(typical) which represents a duty-cycle range of 0% to 100% on PWM signal. When V_{VCON} is 1.3V, the output PWM duty becomes 50%.

2 H-bridge motor driver (OUTA, OUTB)

Using an H-bridge to drive a single-phase BLDC motor provides several advantages for DC fans over a two phase motor commonly driven by two commutated low-side switches. A single phase motor has only two connections; hence, the H-bridge topology requires only two output terminals and two traces are needed on the fan PCB. Generally, this H-bridge method with single phase motor increases fan motor torque density over a typical unipolar drive method. In addition, the H-bridge topology eliminates the number of external component for snubbing and allows recirculation of winding current to maintain energy in a

motor while PWM switching occurs. PWM occurs on the high side, and the freewheeling current flow on the low side during T_{OFF} .

3 Triangle Waveform Generator (PWM Oscillator)

The PWM oscillator output (V_{CT}) sets output PWM frequency using external capacitor (C_T). When V_{CT} reaches the upper threshold(1.8V typical) by internal current source(6uA typical), C_T begins to be discharged by internal current sink(-6uA typical) until the low threshold(0.8V typical). It repeats the charging and discharging cycle. To have a desired PWM frequency, f_{CT} , can be calculated as follows;

$$C_T = \frac{I_{CTC}}{2f_{CT} \times (V_{CTMAX} - V_{CTMIN})}$$

For example, $C_T = 100\text{pF}$, then f_{CT} is about 25KHz.

4. Speed Control Voltage (V_{CON}) and Active Filter (PWM Decoder)

In general, many PC super IO and hardware monitoring ICs provide one of two fan speed control output to provide variable fan speed control without an external drive power stage. FAN8460MTC/FAN8460MP have two type of input stage scheme. This means an end user can control the fan speed with a PWM signal or a DC control voltage (typically thermistor input). Figure.3 shows two kind of input stages; ambient temperature based input stage using thermistor(figure.3a) and digital PWM input stage(figure.3b).

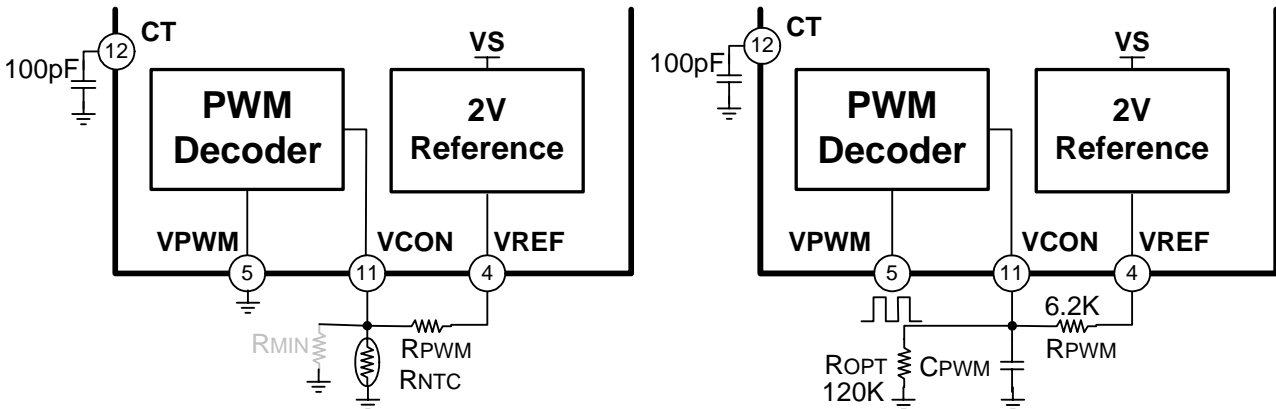


Figure 3. Input Stages and Speed Control Voltage Output

4.1 NTC Thermistor based Speed Control(Scheme 1)

When the ambient temperature based speed control is used, the $VPWM$ pin must be connected with ground as shown figure.3a. The V_{CON} will be adjusted automatically by ambient temperature with NTC thermistor. When the ambient temperature increases, decreased thermistor resistance results in low V_{CON} and high fan motor speed. An optional resistor, R_{MIN} , is set to a minimum speed when thermistor is accidentally disconnected.

The V_{CON} is calculated as follows;

$$V_{CON} = \frac{(R_{MIN} \parallel R_{NTC})}{(R_{MIN} \parallel R_{NTC}) + R_{PWM}} \times V_{VREF}$$

For example, $R_{PWM} = 3\text{K}$, $R_{MIN} = \text{open}$, $R_{NTC} = 10\text{K}$, the V_{CON} is shown in fig4.a. When the temperature is higher than 65, motor will run at full speed. In case, the temperature is under 5°C, no drive will be present. But the practical motor stop temperature is slightly higher than 5°C because motor needs minimum starting torque depending on mechanics, motor size. In case, the R_{MIN} is not used, fan motor runs at full speed when the thermistor is accidentally disconnected.

Another example is usage of optional resistor R_{MIN} to limit minimum motor speed. For example, $R_{PWM} = 1.5\text{K}$, $R_{MIN} = 3.3\text{K}$, $R_{NTC} = 10\text{K}$, fig4.b shows the resultant V_{CON} voltage is under 1.3V and thus the minimum PWM duty will be over 0.5. It means motor will runs at medium speed even if NTC is disconnected accidentally.

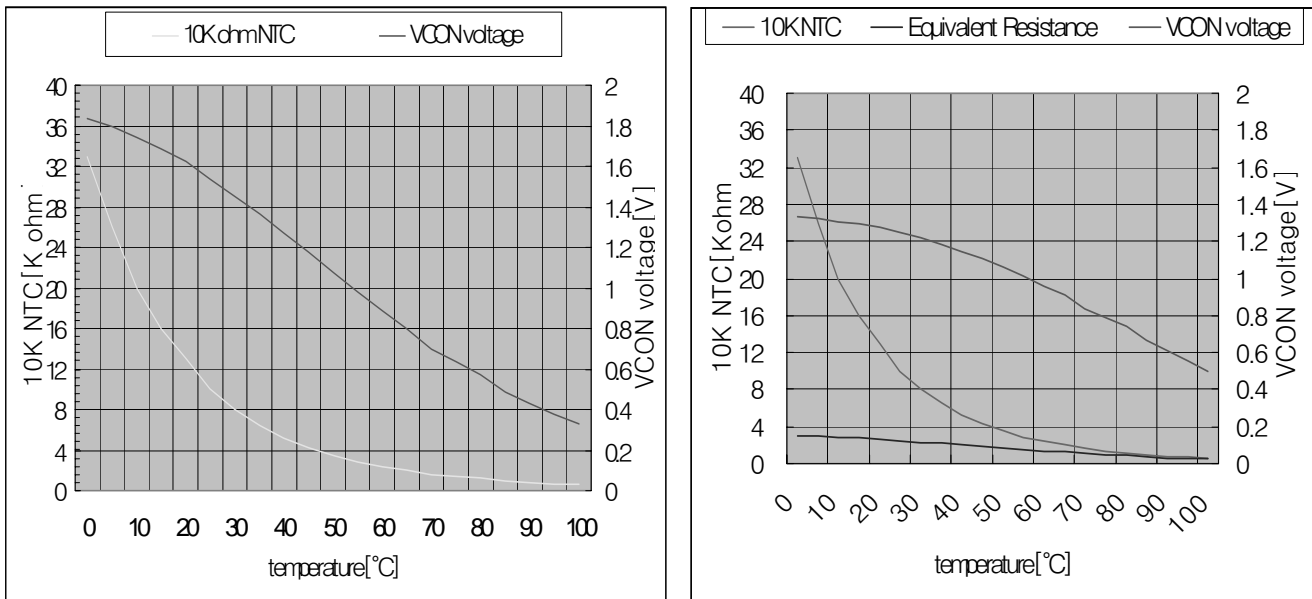


Figure 4. Sensed temperature and speed control voltage

4.2 PWM Speed Control using Internal Oscillator(Scheme 2)

A digital PWM input applied to VPWM pin is converted to analog DC voltage by PWM decoder and external RC filter. The external filter capacitor, CPWM, eliminates high frequency AC component in VVCON. If a large value of CPWM is used, VVCON has smaller value of AC component (ripple), but larger time delay can be occurred in VVCON with some fixed input frequency. The lower frequency of digital PWM input needs the larger value of CPWM. External resistor RPWM, RPWM define the VVCON range as follow;

$$V_{VCON(ON)} = \{V_{REF} - (R_{PWM} \times I_{VCON})\} \times \frac{R_{OPT}}{R_{OPT} + R_{PWM}}$$

$$V_{VCON(OFF)} = V_{VREF} \times R_{OPT} / (R_{PWM} + R_{OPT})$$

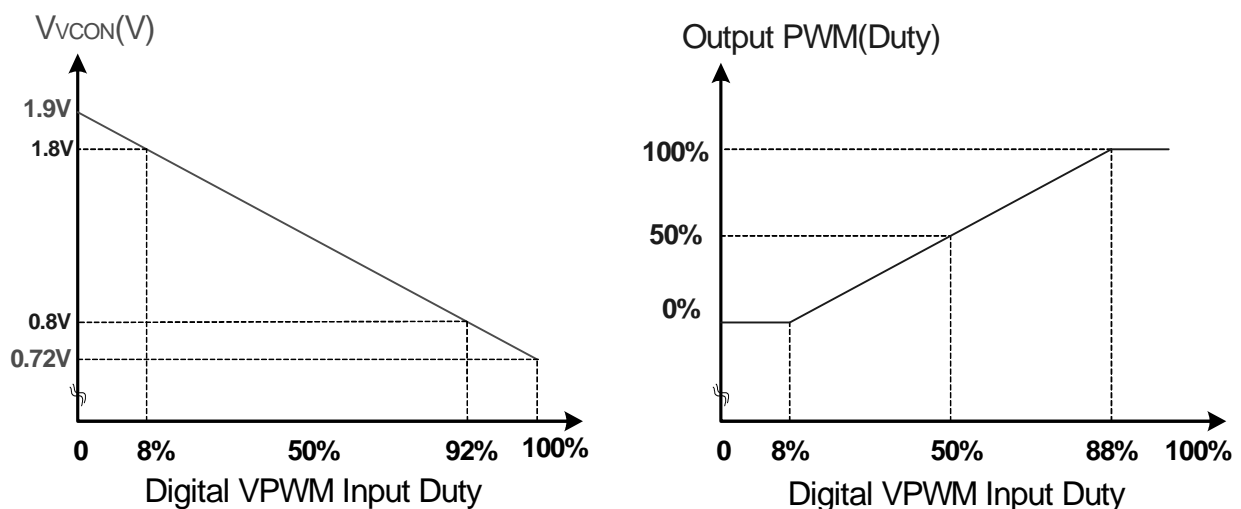


Figure 5. The Relationship Digital PWM Input Duty VS VVCON and Output PWM Duty

For example, RPWM = 6.2K and ROPT = 120K, VVCON become between 0.72V and 1.9V, because VVREF = 2V, IVCON = 200uA. For some design margin, under the 8% duty of digital PWM input, fan motor stops because the output PWM duty is 0. If the duty of digital PWM input is larger than 0.92, then output PWM duty is 100%. It means fan motor is operated in full speed. Figure5.a shows the relationship between digital PWM input and active filter out (VVCON) and figure5.b illustrates the

output PWM duty is proportional to input PWM duty with some dead band. The output PWM frequency is defined by external capacitor, CT. So there is no relationship between VPWM input frequency and output PWM frequency. Table 1 summarizes the motor speed according to digital VPWM input and VCON

Table 1. . Operation Tables

Mode	VPWM	VCON	Speed Condition
PWM Input	H	L	Full Speed
	L	H	Stop
	H/L	Depend on mother board PWM signal	proportional to PWM input duty
Thermistor Input	GND	Depend on thermistor resistance	The higher TEMP, the faster fan speed

4.3 PWM Speed Control using External PWM Input(Scheme 3)

This scheme indicates that digital PWM input signal becomes directly output PWM signal. In other word, frequency and duty of output PWM driving signal is the same as this digital PWM input. In case input PWM frequency is very low, active filter needs large value of capacitor to make speed control voltage in scheme 2. This scheme dosen't need filter capacitor and has good input/output characteristics. This means that there is no deadband and output signals are synchronized with input VPWM signal as shown in figure6.

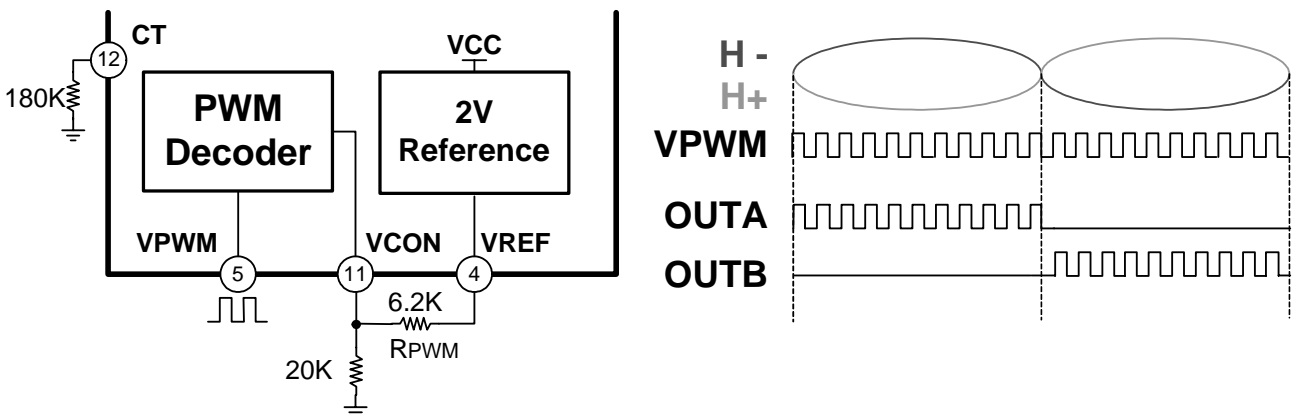


Figure 6. Interface and it's Related Waveforms Scheme3

4.4 Offset comparator(Thermistor open protection)

If under 100mV difference between VREF and VCON, fan motor runs at full speed.

5 Locked Rotor Protection with Open Collector Output and Automatic Restart

When the rotor is locked, there is no change in input signal of hall amplifier and thus a internal TZERO pulse is not observed. A capacitor (CLD) connected LD pin is continually charged by internal current source (iLDC) to the internal threshold (VLDCL) resulting from no Tzero pulse. When the voltage, VCLD on LD pin, reaches VLDCL, high side output power TR is turned-off to protect motor during TOFF and the alarm output (AL) becomes floating high. When the VCLD reaches upper threshold, VLDCL, VCLD starts to decrease with internal current sink (iLDD) to the low threshold, VLDCL. At that time, the VCLD ramps up again and one of two outputs is turned on depending on locked rotor position during TON. The charging and discharging repeat until locked condition is removed, or FAN8460MTC/FAN8460MP is powered down. The overall time chart is shown in figure.6. The auto- retry time (TON), the motor protection time (TOFF) and the locked rotor detection time (TLOCK) are proportional to external capacitor, CLD. Each value can be calculated as follows;

$$T_{ON} = \frac{C_{LD} \times (V_{LDCL} - V_{LDCLP})}{i_{LDC}}$$

$$T_{OFF} = \frac{C_{LD} \times (V_{LDCL} - V_{LDCLP})}{i_{LDD}}$$

$$T_{LOCK} = \frac{C_{LD} \times V_{LDCL}}{i_{LDC}}$$

For example, $C_{LD} = 0.33\mu F$, then $T_{ON} = 0.3\text{Sec}$, $T_{OFF} = 2\text{Sec}$, $T_{LOCK} = 0.4\text{Sec}$. This AL output can be used to inform a locked rotor condition to super IO or system controller. Because the AL output is open collector type, end user can pull up this pin with a external resistor to the supply voltage of their choice (that is 5 or 3.3V).

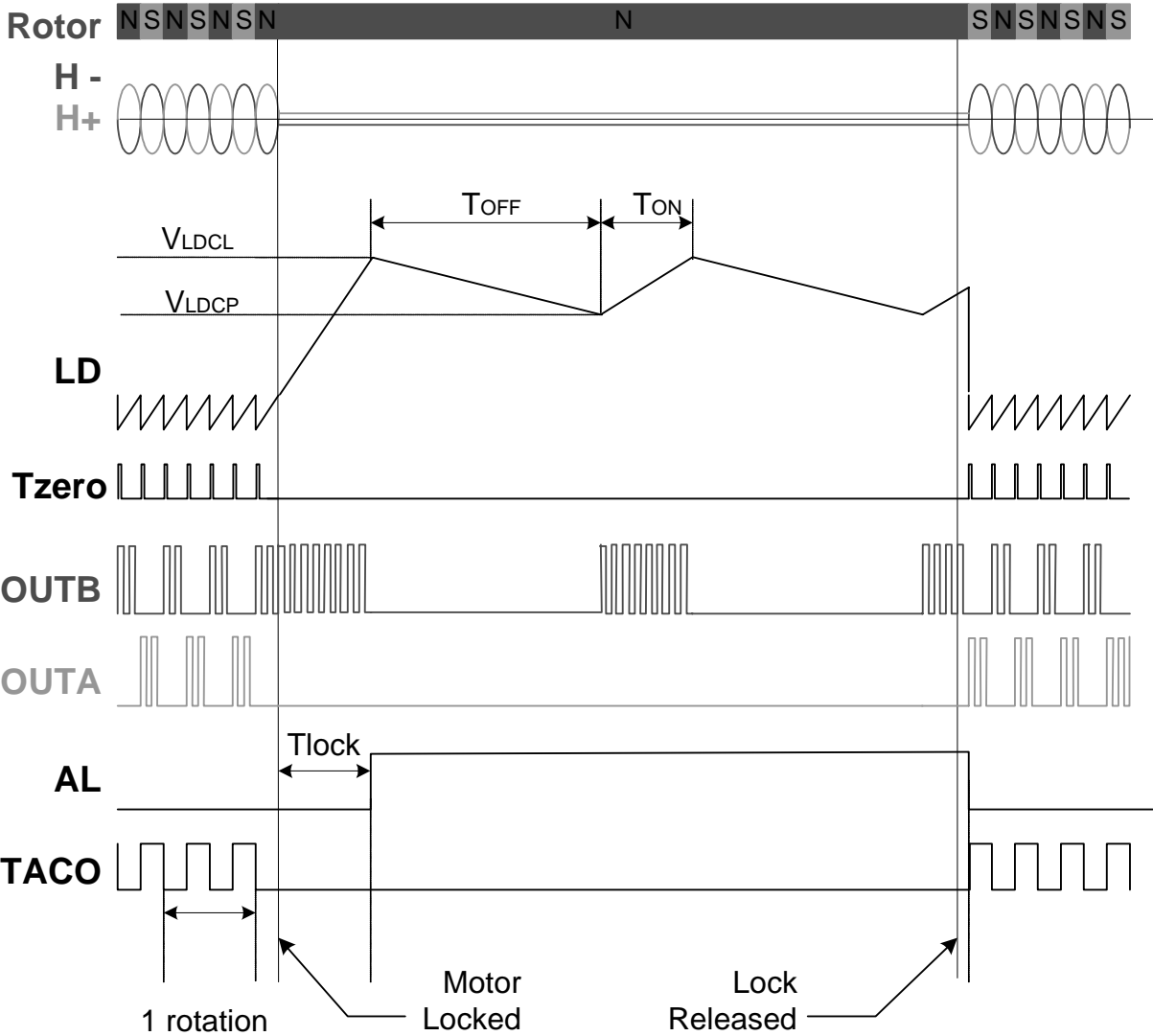


Figure 7. Overall Timing Chart

6. Hall Sensor Amplifier

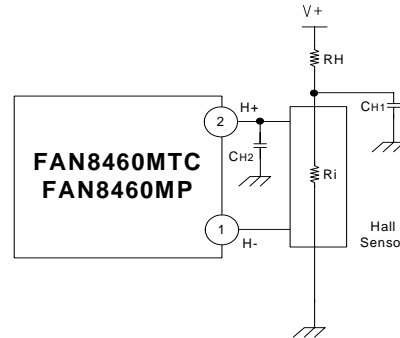


Figure 1. Hall Sensor Interface

The hall current (I_H) is determined as follows;

$$I_H = \frac{V_{CC}}{(R_H + R_i)}$$

Where, R_H is an external limiting resistor and R_i is input impedance of hall sensor. An external capacitor, CH_1 , can be used to reduce a power supply noise. CH_2 can reduce the instant peak current using H-bridge's commutation. The input range of hall amplifier is between 0V and $V_{CC}-2.8V$ as shown in following figure.

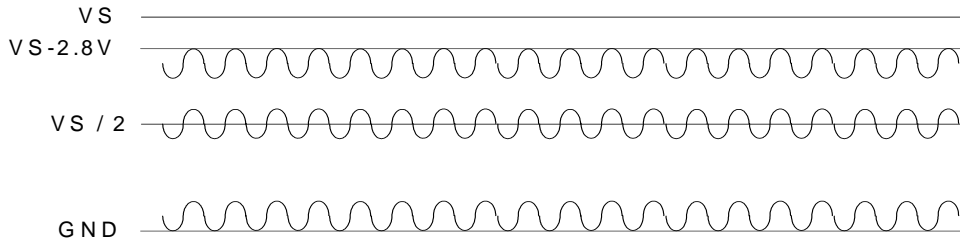


Figure 2. Hall Amplifier Input Range

Table 1. Hall Sensor Outputs and Related Pin outputs

(H+) -(H-)	LD	OUT A	OUT B	AL	TACO	Remark
Positive	Low Level	L	PWM	L	L	ROTATING
Negative	Low Level	PWM	L	L	H	
-	-	-	-	H	L or H	LOCK

7 Open Collector TACO Output for Speed Feedback

The TACO output comes from the hall amplifier output. Because the TACO output is open collector type, end user can pull up this pin with a external resistor to the supply voltage of their choice (that is 5 or 3.3V). This resulting output signal has two pulses per revolution on a four pole motor.

9 Supply Voltage Consideration

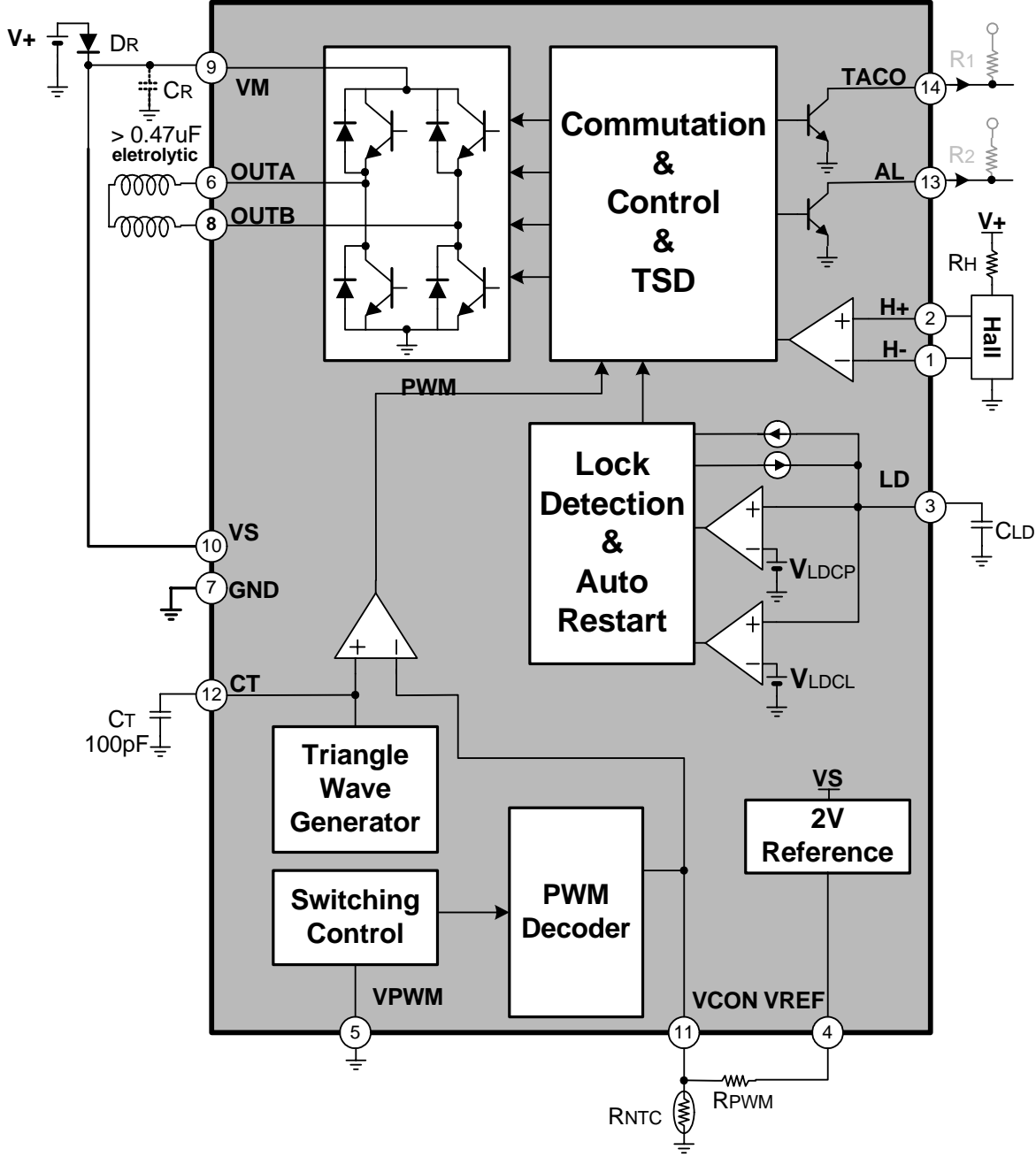
A supply sustain capacitor (C_R) should be placed as close to VM pin with GND as layout permits. A reverse supply protection diode (DR) prevent motor current from recirculating to power source when PWM operation and phase commutation occur. This results in increasing VM and VS pin voltage. This capacitor absorbs motor recirculating current and limits VM and VCC pin voltage. In general, large motor winding inductance and current need large value of C_R .

9. Thermal Shutdown

TSD on: Two high side output TR are off.(Typ. 175°C)

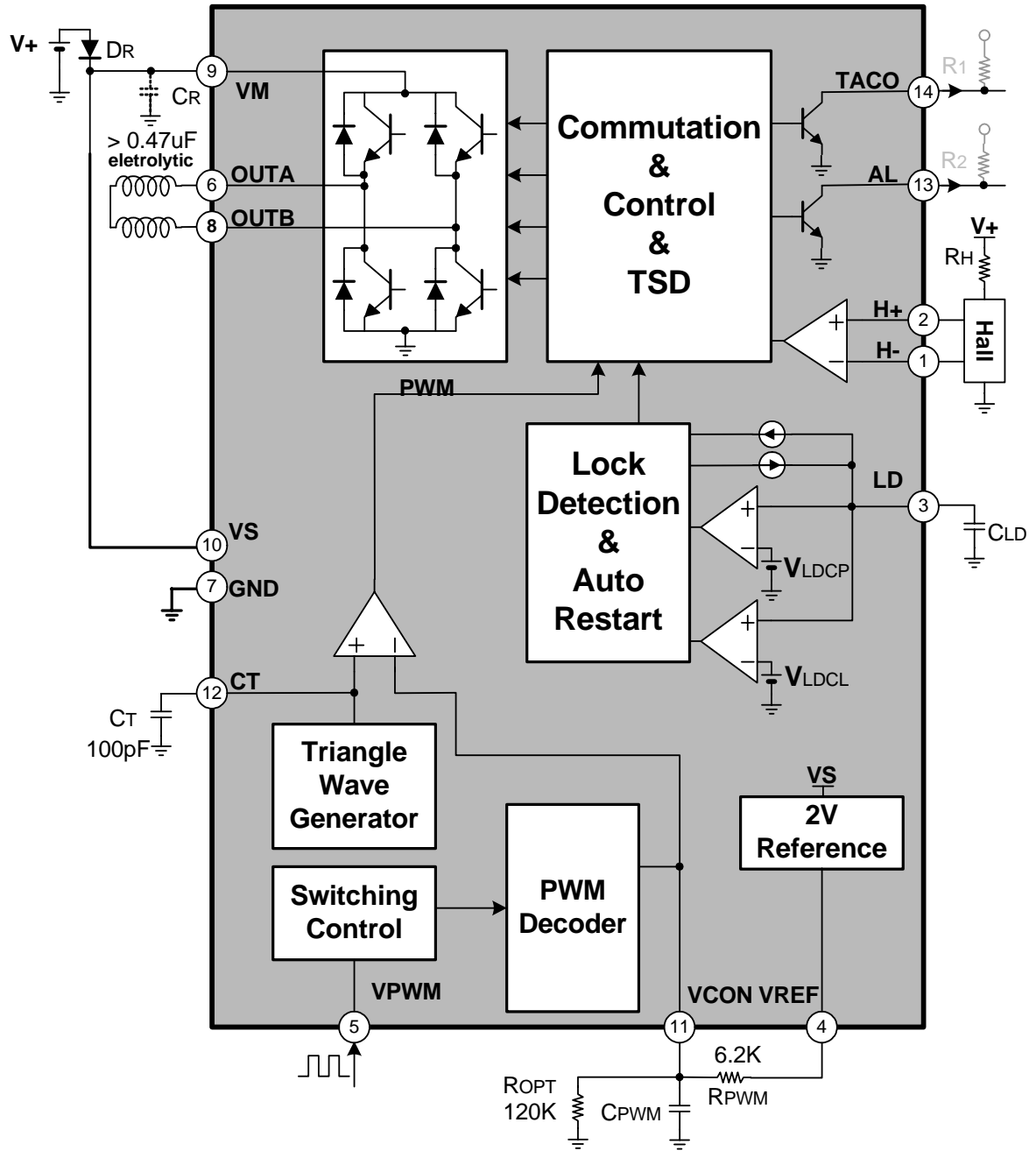
TSD off: The circuit can be reactivated and begin to operate in a normal condition. (Typ. 150°C)

Typical Application Circuits 1 (NTC Thermistor based Speed Control)



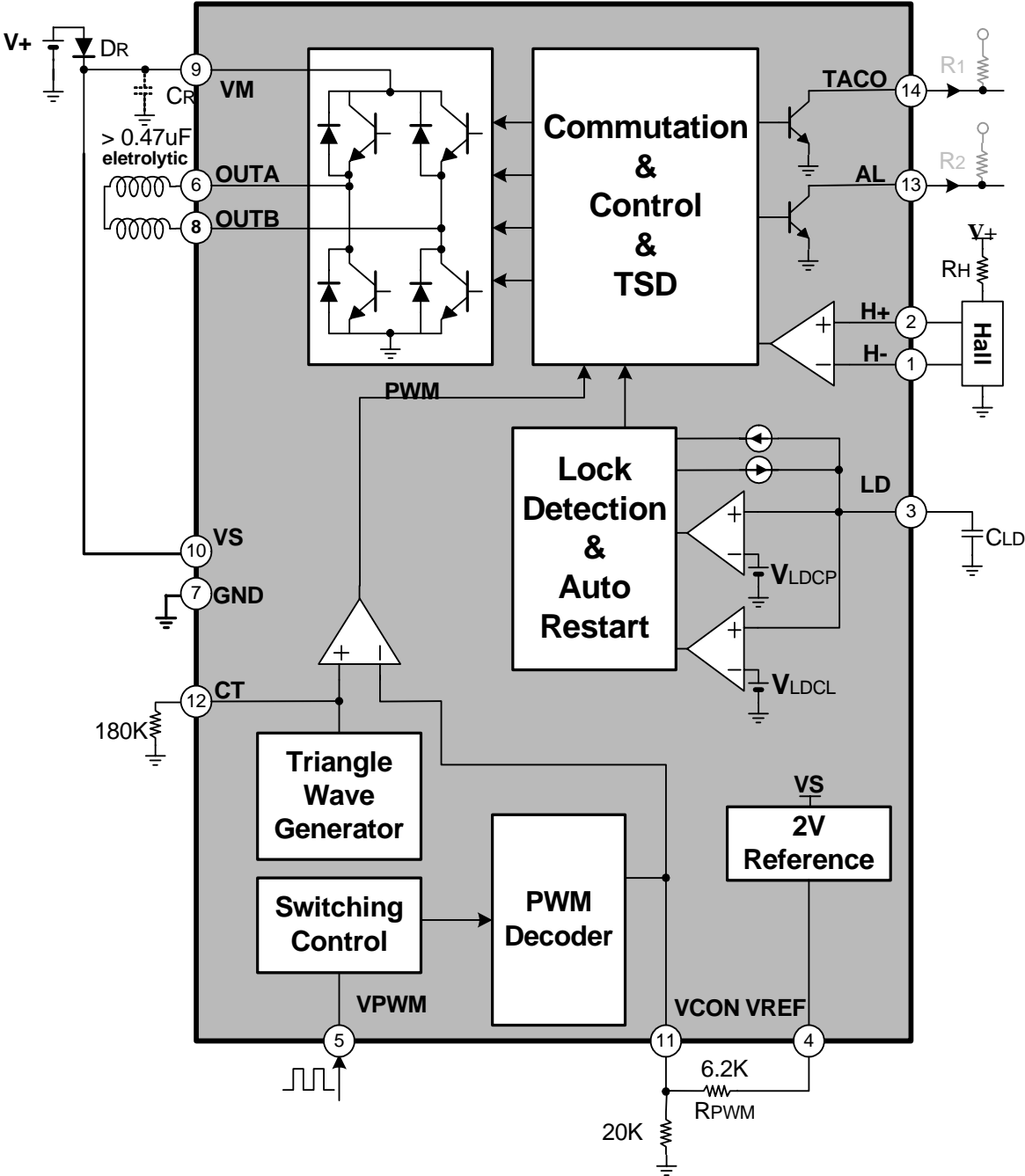
Mode	VPWM	VCON	Speed Condition
Thermistor Input	GND	Depend on thermistor resistance	The higher TEMP, the faster fan speed

Typical Application Circuits 2 (PWM Input Speed Control using Internal Oscillator)



Mode	VPWM	VCON	Speed Condition
PWM Input	H	L	Full Speed
	L	H	Stop
	L/H	H/L	proportional to PWM duty (Duty range:0.15 ~ 0.85)

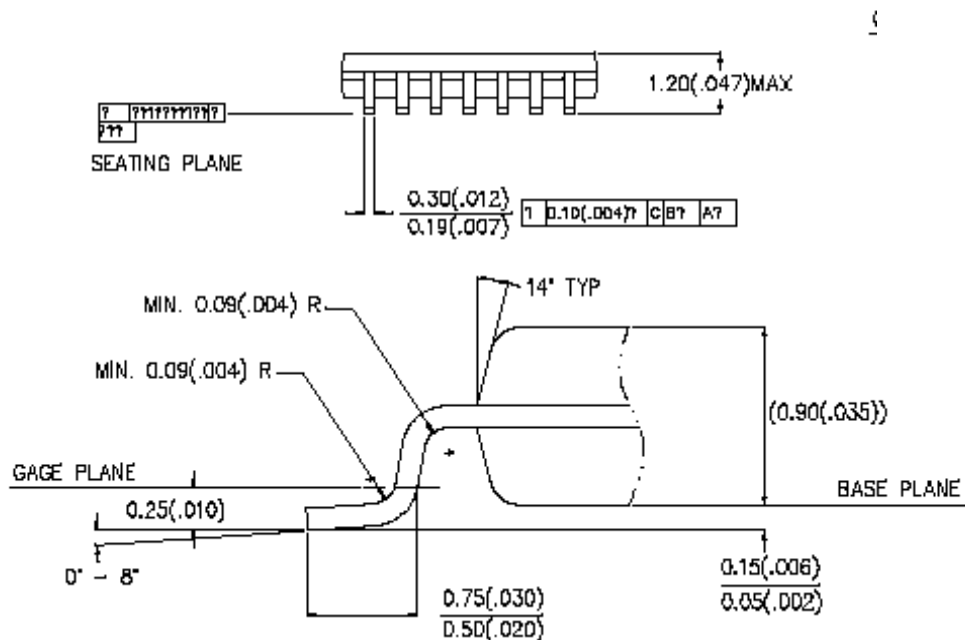
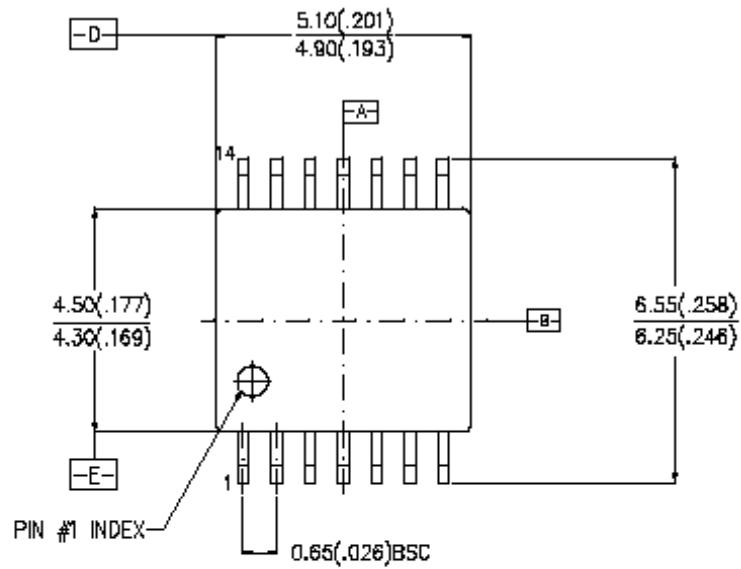
Typical Application Circuits 3 (PWM Input Speed Control using External PWM Input)



Mode	VPWM	VCON	Speed Condition
PWM Input	H	L	Full speed
	L	H	Stop
	H/L	L/H	proportional to PWM Duty

Package Dimensions (Unit: mm)

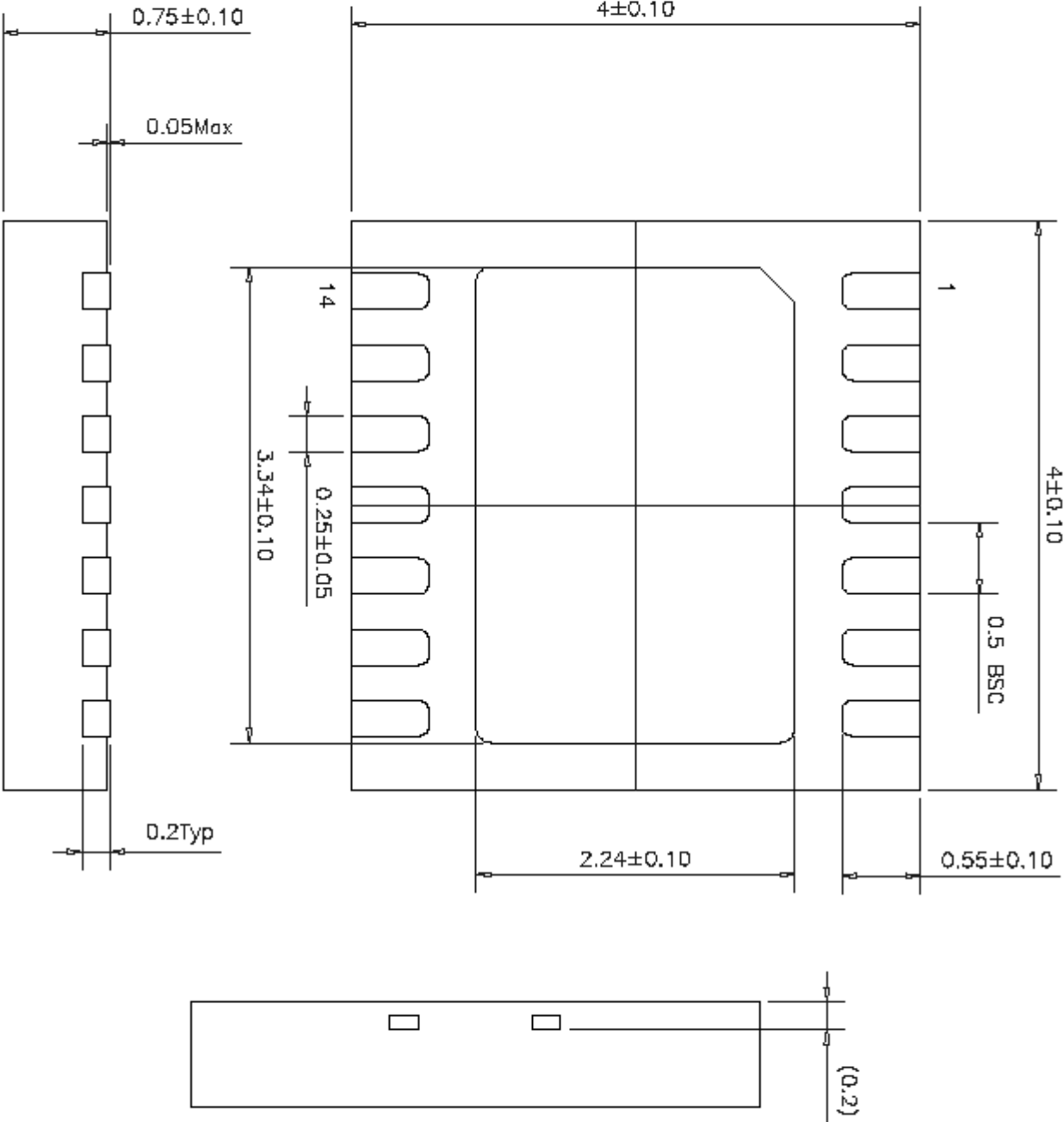
14-TSSOP



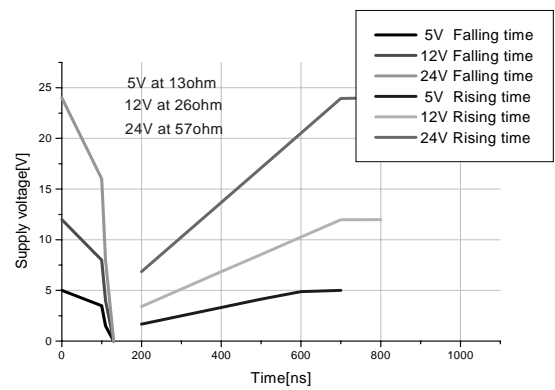
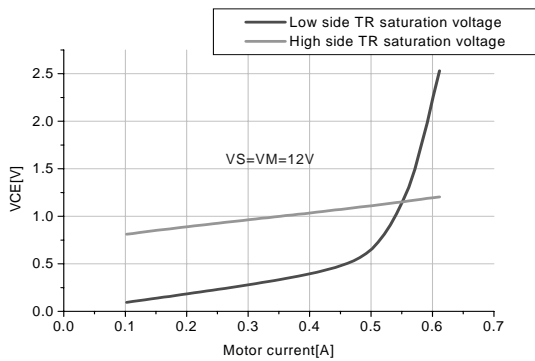
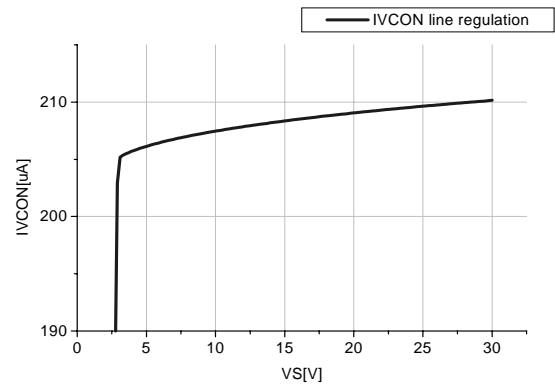
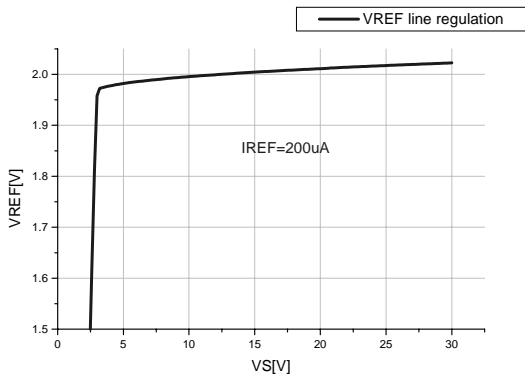
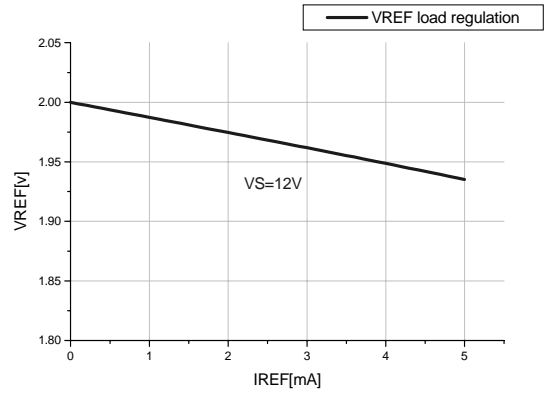
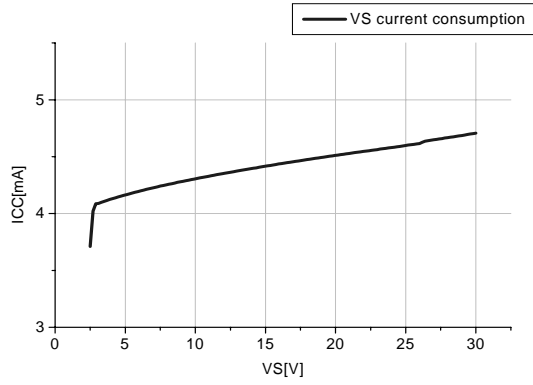
Package Dimensions (Unit: mm)

14-MLP 4X4

Pad size
3.34X2.24
Bottom view



Typical Performance characteristics



DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.