PD- 94207

International
IOR Rectifier

SMPS MOSFET

IRFB61N15D

HEXFET® Power MOSFET

Applications
- High frequency DC-DC converters
- Motor Control
- Uninterruptible Power Supplies

V_{DSS}	$R_{DS(on)}$ max	I_D
150V	**0.032Ω**	**60A**

Benefits
- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C_{OSS} to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current

TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	60	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	42	
I_{DM}	Pulsed Drain Current ①	250	
P_D @T_A = 25°C	Power Dissipation	2.4	W
P_D @T_C = 25°C	Power Dissipation	330	
	Linear Derating Factor	2.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	3.7	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torqe, 6-32 or M3 screw⑥	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.45	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

Notes ① through ⑤ are on page 8

5/3/01

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.032	Ω	V_{GS} = 10V, I_D = 36A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.5	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 150V, V_{GS} = 0V
		—	—	250		V_{DS} = 120V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V

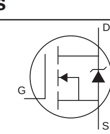
Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	22	—	—	S	V_{DS} = 50V, I_D = 37A
Q_g	Total Gate Charge	—	95	140	nC	I_D = 37A
Q_{gs}	Gate-to-Source Charge	—	26	39		V_{DS} = 120V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	45	68		V_{GS} = 10V,
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	V_{DD} = 75V
t_r	Rise Time	—	110	—		I_D = 37A
$t_{d(off)}$	Turn-Off Delay Time	—	28	—		R_G = 1.8Ω
t_f	Fall Time	—	51	—		V_{GS} = 10V ④
C_{iss}	Input Capacitance	—	3470	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	690	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	150	—		ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	4600	—		V_{GS} = 0V, V_{DS} = 1.0V, ƒ = 1.0MHz
C_{oss}	Output Capacitance	—	310	—		V_{GS} = 0V, V_{DS} = 120V, ƒ = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	580	—		V_{GS} = 0V, V_{DS} = 0V to 120V ⑤

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	520	mJ
I_{AR}	Avalanche Current①	—	37	A
E_{AR}	Repetitive Avalanche Energy①	—	33	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	60	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	250		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 37A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	180	270	ns	T_J = 25°C, I_F = 37A
Q_{rr}	Reverse RecoveryCharge	—	1340	2010	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

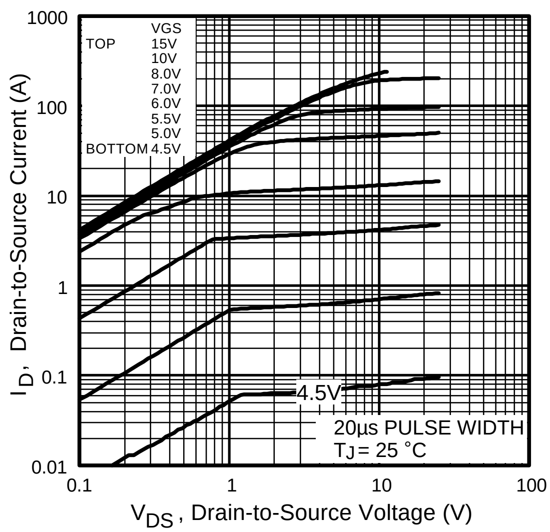


Fig 1. Typical Output Characteristics

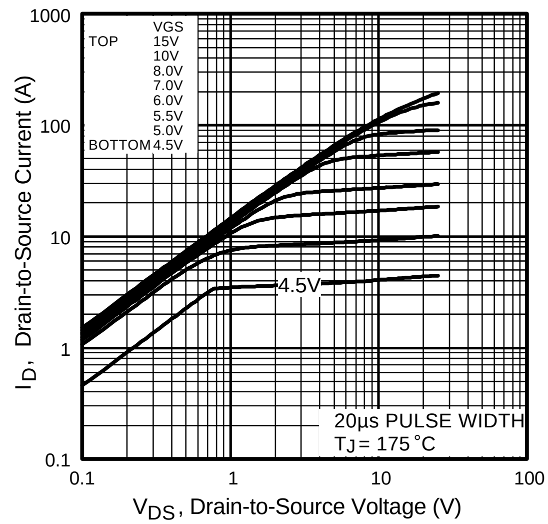


Fig 2. Typical Output Characteristics

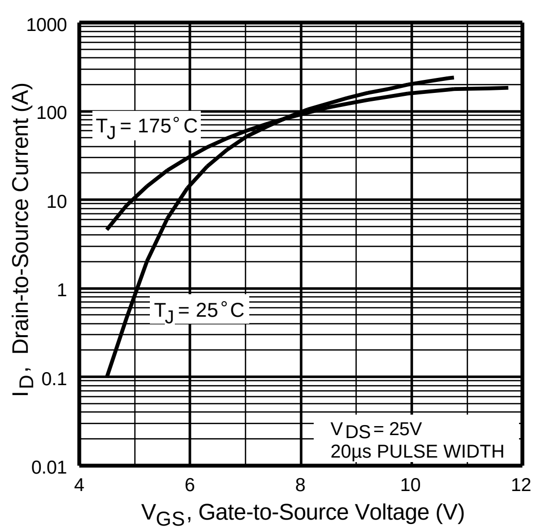


Fig 3. Typical Transfer Characteristics

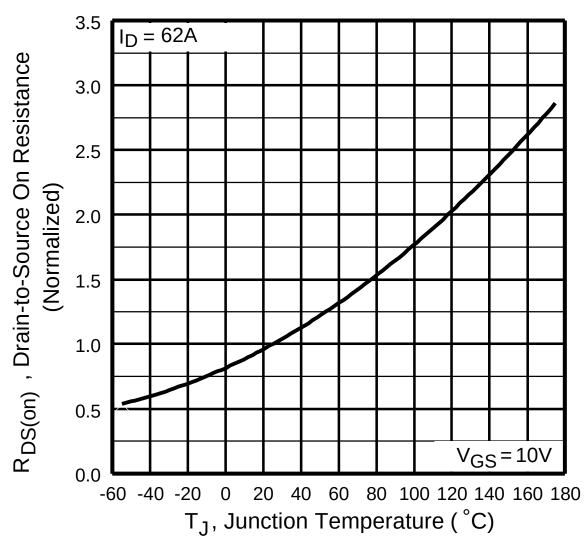


Fig 4. Normalized On-Resistance Vs. Temperature

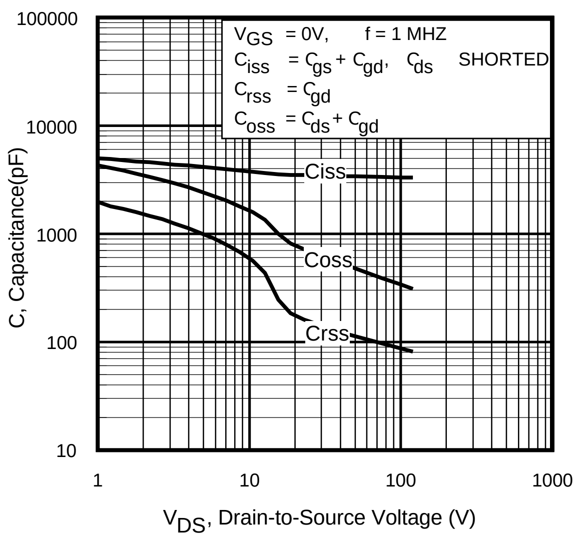


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

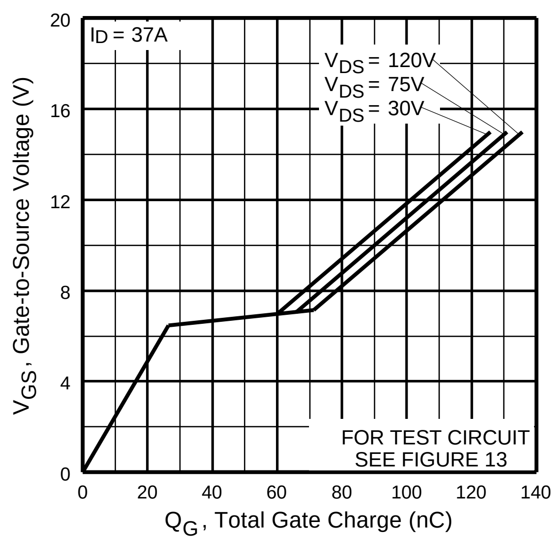


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

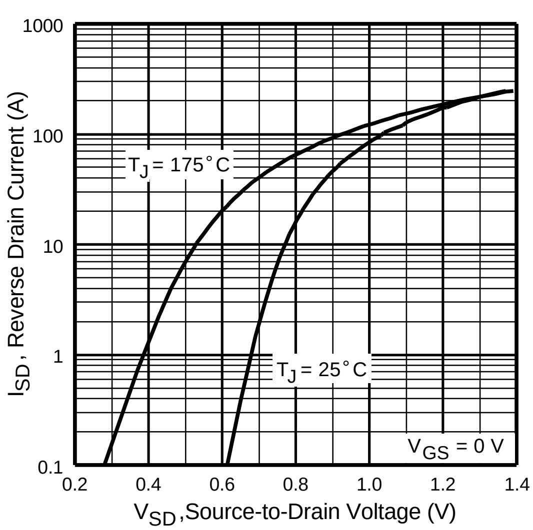


Fig 7. Typical Source-Drain Diode Forward Voltage

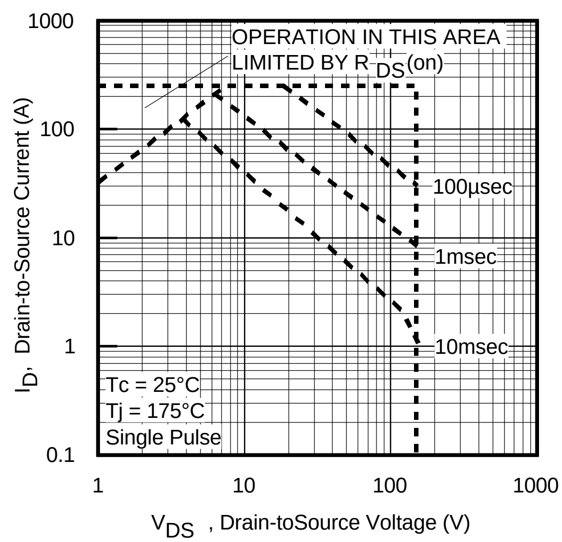


Fig 8. Maximum Safe Operating Area

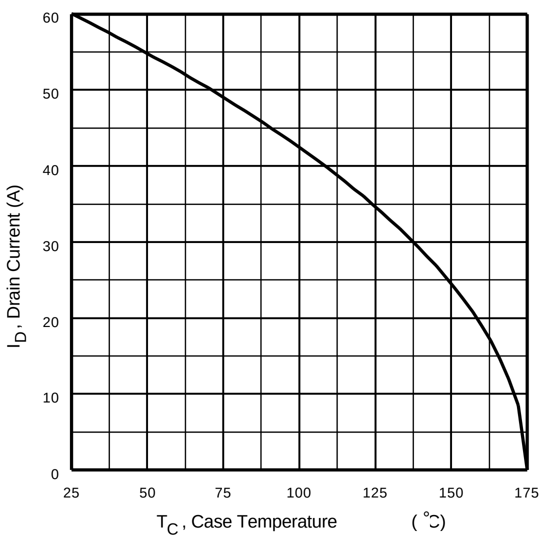


Fig 9. Maximum Drain Current Vs. Case Temperature

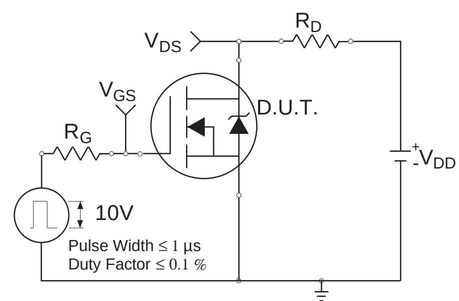


Fig 10a. Switching Time Test Circuit

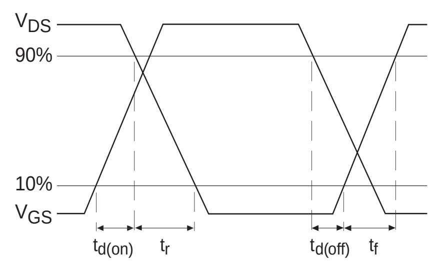


Fig 10b. Switching Time Waveforms

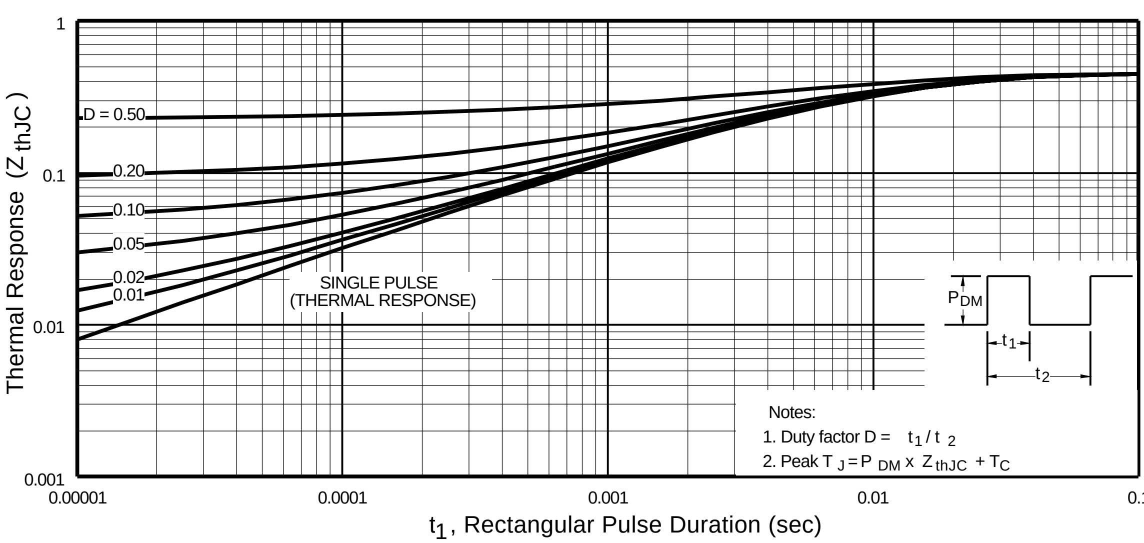


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

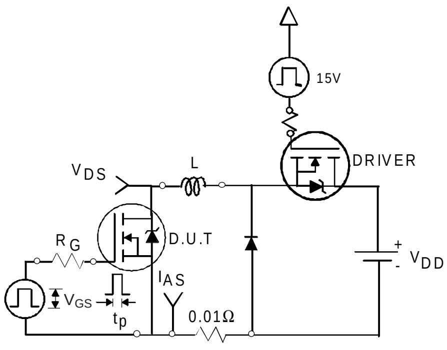


Fig 12a. Unclamped Inductive Test Circuit

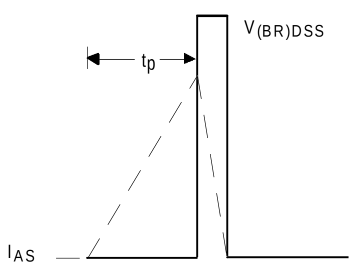


Fig 12b. Unclamped Inductive Waveforms

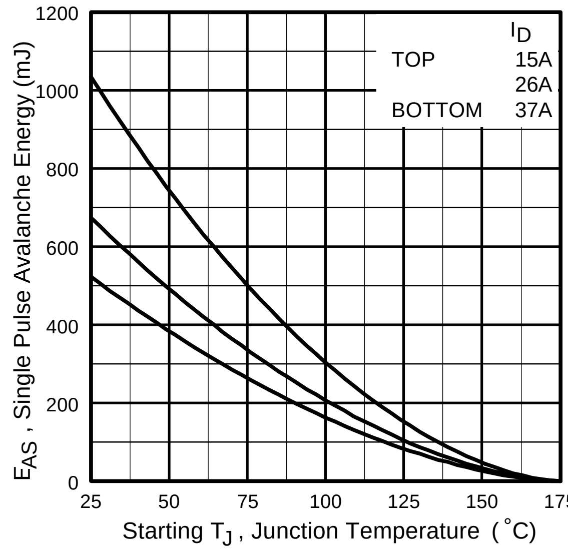


Fig 12c. Maximum Avalanche Energy
Vs. Drain Current

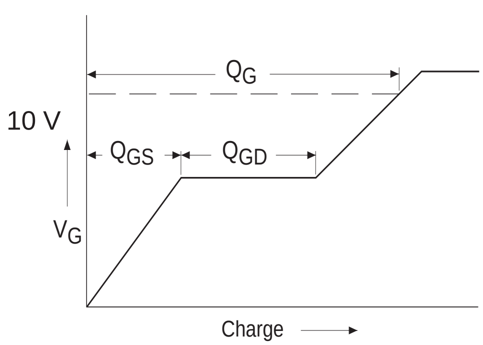


Fig 13a. Basic Gate Charge Waveform

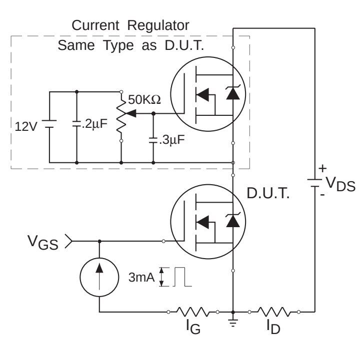
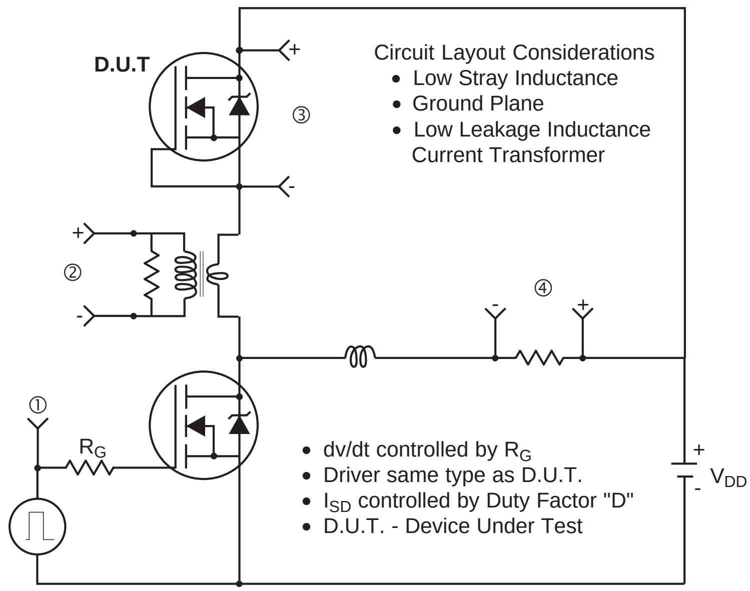
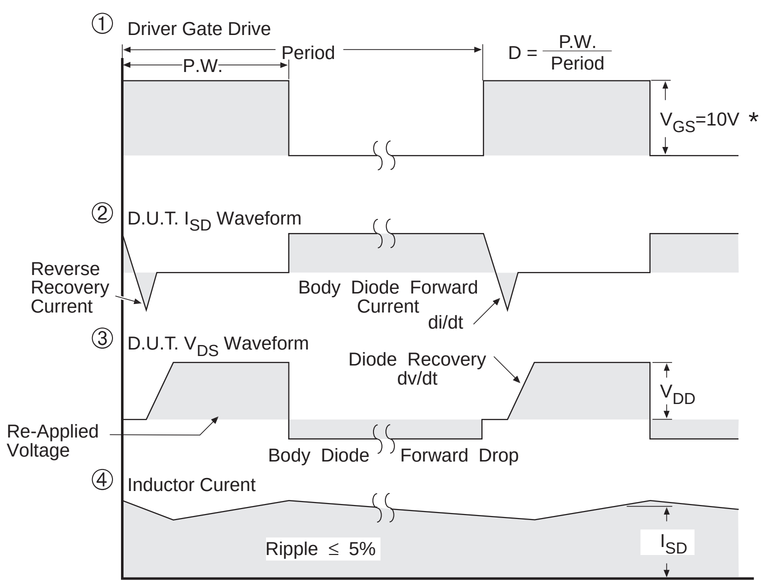


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



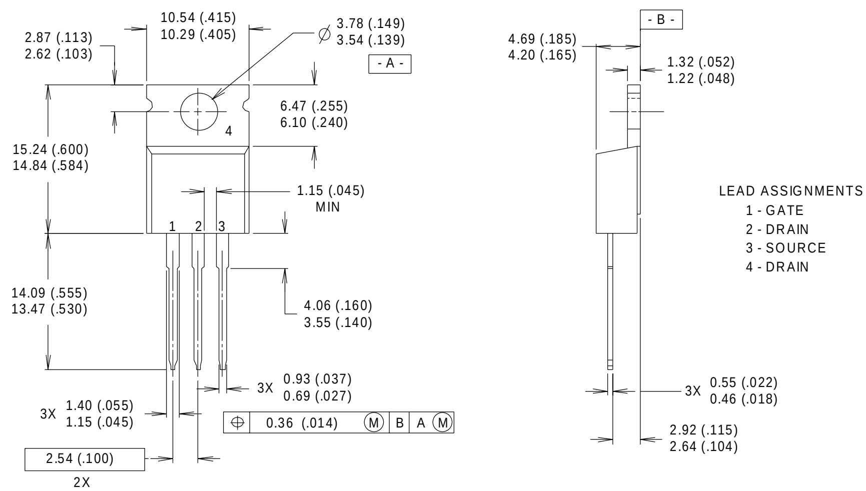


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

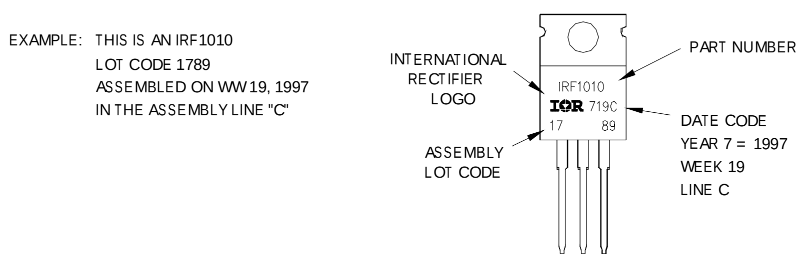
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

TO-220AB Part Marking Information



Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 0.98mH R_G = 25Ω, I_{AS} = 37A, V_{GS}=10V

③ $I_{SD} \leq 37A$, di/dt ≤ 170A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.5/01