FAIRCHILD SEMICONDUCTOR®

January 2005

FCAS50SN60

Smart Power Module for SRM

Features

- Very low thermal resistance due to using DBC
- 600V-50A single-phase asymmetric bridge IGBT converter for SRM drive including control ICs for gate driving and protection
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Switching frequency of 2.2~8kHz
- Isolation rating of 2500Vrms/min.

Applications

- AC 200V ~ 242V single-phase SRM drives for home application vacuum cleaner.

General Description

FCAS50SN60 is an advanced smart power module for SRM drive that Fairchild has newly developed and designed to provide very compact and high performance SRM motor drives mainly targeting low-power inverter-driven SRM application especially for a vacuum air cleaner. It combines optimized circuit protection and drive matched to low-loss IGBTs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. The high speed built-in HVIC provides opto-coupler-less IGBT gate driving capability that further reduce the overall size of the inverter system design. In addition the incorporated HVIC facilitates the use of single-supply drive topology enabling the FCAS50SN60 to be driven by only one drive supply voltage without negative bias. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.

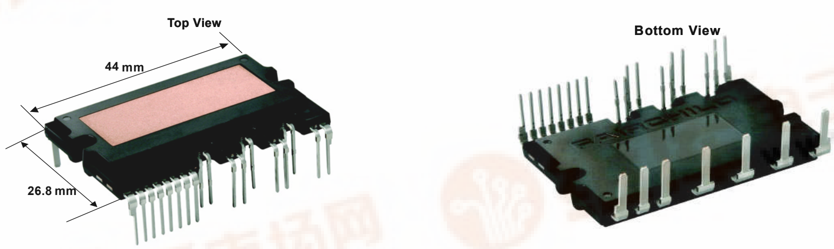


Figure 1.

Integrated Power Functions

- 600V-50A IGBT asymmetric converter for single-phase SRM drives (Please refer to Figure 3)

Integrated Drive, Protection and System Control Functions

- For high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
  Control circuit under-voltage (UV) protection
  Note) Available bootstrap circuit example is given in Figures 10.
- For low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
  Control supply circuit under-voltage (UV) protection
- Fault signaling: Corresponding to a UV fault (Low-side supply)
- Input interface: 5V CMOS/LSTTL compatible, Schmitt trigger input

Pin Configuration

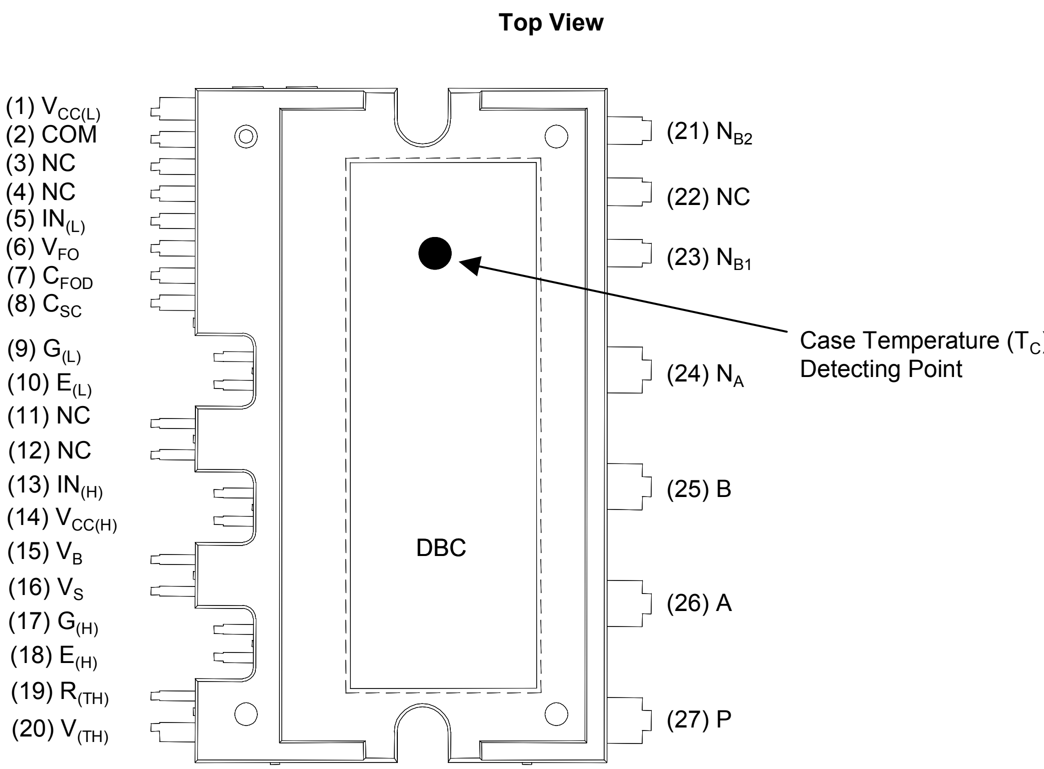
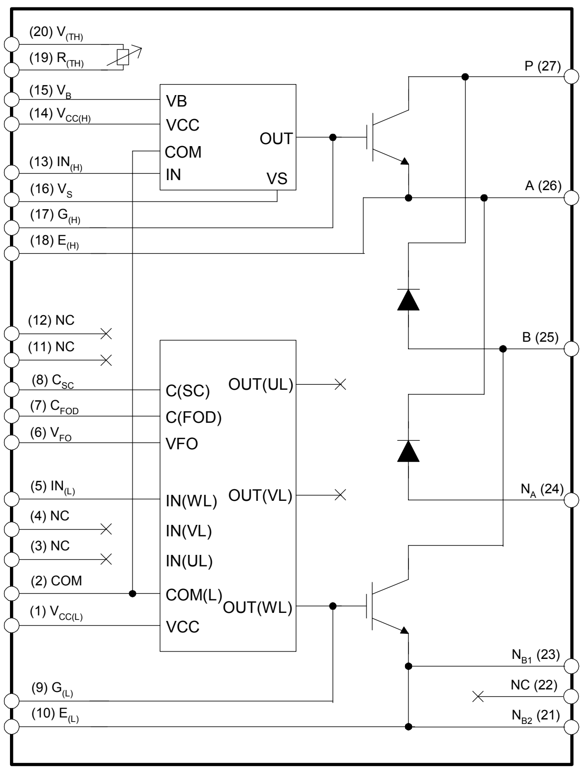


Figure 2.

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	NC	Dummy Pin
4	NC	Dummy Pin
5	$IN_{(L)}$	Signal Input for Low-side IGBT
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection
9	$G_{(L)}$	Gate terminal of low-side IGBT
10	$E_{(L)}$	Emitter terminal of low-side IGBT
11	NC	Dummy Pin
12	NC	Dummy Pin
13	$IN_{(H)}$	Signal Input for High-side IGBT
14	$V_{CC(H)}$	High-side Bias Voltage
15	V_B	High-side Bias Voltage for Gate Driving
16	V_S	High-side Bias Voltage Ground for Gate Driving
17	$G_{(H)}$	Gate terminal of the High-side IGBT
18	$E_{(H)}$	Emitter terminal of the High-side IGBT
19	$R_{(TH)}$	Thermistor Series Resistor
20	$V_{(TH)}$	Thermistor Bias Voltage
21	N_{B2}	Negative DC–Link Input for B Leg (Should be shorted with N_{B1} externally)
22	NC	Dummy Pin
23	N_{B1}	Negative DC–Link Input for B Leg (Should be shorted with N_{B2} externally)
24	N_A	Negative DC–Link Input for A Leg
25	B	Output for B Leg
26	A	Output for A Leg
27	P	Positive DC–Link Input

Internal Equivalent Circuit and Input/Output Pins



Note:

1. The low-side is composed of one IGBT and freewheeling diode and one control IC which has gate driving and protection functions.
2. The power side is composed of four dc-link input terminals and two output terminals.
3. The high-side is composed of one IGBT and freewheeling diode and one drive IC for high-side IGBT.

Figure 3.

Absolute Maximum Ratings (T_J = 25°C, Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Conditions	Rating	Units
$V_{PN(Surge)}$	Supply Voltage (Surge)	Applied between P- N_A, N_{B1}, N_{B2}	550	V
V_{CES}	Collector-emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	T_C = 25°C	50	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	T_C = 25°C, Under 1ms Pulse Width	100	A
P_C	Collector Dissipation	T_C = 25°C per One IGBT	110	W
T_J	Operating Junction Temperature	(Note 1)	-20 ~ 125	°C

Note:

1. The maximum junction temperature rating of the power chips integrated within the module is 150 °C(@$T_C \le$ 100°C). However, to insure safe operation, the average junction temperature should be limited to $T_{J(ave)} \le$ 125°C (@$T_C \le$ 100°C)

Control Part

Symbol	Parameter	Conditions	Rating	Units
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM	20	V
V_{BS}	High-side Control Bias Voltage	Applied between V_B - V_S	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(H)}$, $IN_{(L)}$ - COM	-0.3~5.5	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} - COM	-0.3~V_{CC}+0.3	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	5	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3~V_{CC}+0.3	V

Total System

Symbol	Parameter	Conditions	Rating	Units
$V_{PN(PROT)}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	V_{CC} = V_{BS} = 13.5 ~ 16.5V T_J = 125°C, Non-repetitive, less than 6μs	400	V
T_C	Module Case Operation Temperature		-20 ~ 95	°C
T_{STG}	Storage Temperature		-40 ~ 125	°C
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, AC 1 minute, Connection Pins to DBC	2500	V_{rms}

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Each IGBT under Operating Condition	-	-	0.90	°C/W
$R_{th(j-c)F}$		Each FWDi under Operating Condition	-	-	2.2	°C/W

Note:

2. For the measurement point of case temperature (T_C), please refer to Figure 2.

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Inverter Part

Symbol		Parameter	Conditions		Min.	Typ.	Max.	Units
$V_{CE(SAT)}$		Collector-Emitter Saturation Voltage	V_{CC} = V_{BS} = 15V V_{IN} = 5V	I_C = 50A, T_J = 25°C	-	1.6	2.3	V
V_{FM}		FWDi Forward Voltage	V_{IN} = 0V	I_C = 50A, T_J = 25°C	-	2.1	3.0	V
HS	t_{ON}	Switching Times	V_{PN} = 300V, V_{CC} = V_{BS} = 15V I_C = 50A V_{IN} = 0V ↔ 5V, Inductive Load $R_{E(H)}$ = 10Ω (Note 3)		-	0.8	-	µs
	$t_{C(ON)}$				-	0.6	-	µs
	t_{OFF}				-	1.5	-	µs
	$t_{C(OFF)}$				-	0.8	-	µs
	t_{rr}				-	0.08	-	µs
LS	t_{ON}		V_{PN} = 300V, V_{CC} = V_{BS} = 15V I_C = 50A V_{IN} = 0V ↔ 5V, Inductive Load (Note 3)		-	1.1	-	µs
	$t_{C(ON)}$				-	0.9	-	µs
	t_{OFF}				-	1.5	-	µs
	$t_{C(OFF)}$				-	0.8	-	µs
	t_{rr}				-	0.05	-	µs
	I_{CES}	Collector - Emitter Leakage Current	V_{CE} = V_{CES}		-	-	250	µA

Note:

3. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

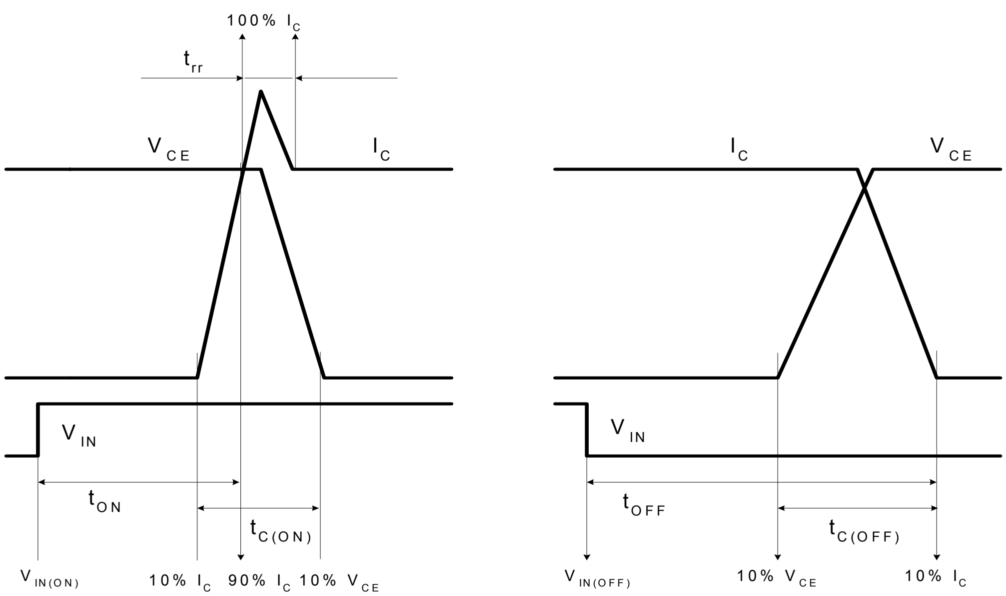


Figure 4. Switching Time Definition

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Control Part

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
I_{QCCL}	Quiescent V_{CC} Supply Current	V_{CC} = 15V $IN_{(L)}$ = 0V	$V_{CC(L)}$ - COM	-	-	40	mA
I_{QCCH}		V_{CC} = 15V $IN_{(H)}$ = 0V	$V_{CC(H)}$ - COM	-	-	80	μA
I_{QBS}	Quiescent V_{BS} Supply Current	V_{BS} = 15V $IN_{(H)}$ = 0V	V_B - V_S	-	-	100	μA
V_{FOH}	Fault Output Voltage	V_{SC} = 0V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		4.5	-	-	V
V_{FOL}		V_{SC} = 1V, V_{FO} Circuit: 4.7kΩ to 5V Pull-up		-	-	0.8	V
$V_{SC(ref)}$	Short Circuit Trip Level	V_{CC} = 15V (Note 4)		0.45	0.5	0.55	V
UV_{CCD}	Supply Circuit Under-Voltage Protection	Detection Level	Applied between $V_{CC(L)}$ - COM	10.5	-	12.5	V
UV_{CCR}		Reset Level		11.0	-	13	V
UV_{BSD}		Detection Level	Applied between V_B - V_S	10.0	-	12.5	V
UV_{BSR}		Reset Level		10.5	-	13.0	V
t_{FOD}	Fault-out Pulse Width	C_{FOD} = 33nF (Note 5)		1.4	1.8	2.0	ms
V_{IH}	ON Threshold Voltage	Logic'1' input voltage	Applied between $IN_{(H)}$, $IN_{(L)}$ - COM	3.0	-	-	V
V_{IL}	OFF Threshold Voltage	Logic'0' input voltage		-	-	0.8	V
$I_{INH(ON)}$	Input Bias Current	$IN_{(H)}$ = 5V	Applied between $IN_{(H)}$, $IN_{(L)}$ - COM	0.9	-	2.2	mA
$I_{INL(ON)}$		$IN_{(L)}$ = 5V		0.9	-	2.4	mA
R_{TH}	Resistance of Thermistor	@ T_C = 25°C (Note Fig. 10)		-	50	-	kΩ
		@ T_C = 80°C (Note Fig. 10)		-	5.76	-	kΩ

Note:

4. Short-circuit current protection is functioning only at the low-sides.

5. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$[F]

Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P - N_A, N_{B1}, N_{B2}	-	300	450	V
V_{CC}	Control Supply Voltage	Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM	13.5	15	16.5	V
V_{BS}	High-side Bias Voltage	Applied between V_B - V_S	13.5	15	18.5	V
f_{PWM}	PWM Input Signal	$T_C \leq 100$°C, $T_J \leq 125$°C	-	3	-	kHz
$V_{IN(ON)}$	Input ON Voltage	Applied between $IN_{(H)}$, $IN_{(L)}$ - COM	4 ~ 5.5			V
$V_{IN(OFF)}$	Input OFF Voltage	Applied between $IN_{(H)}$, $IN_{(L)}$ - COM	0 ~ 0.65			V

Mechanical Characteristics and Ratings

Parameter	Conditions		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw - M3		5.17	6.29	7.30	Kg•cm
			0.51	0.62	0.72	N•m
Surface Flatness		Note Figure 5.	0	-	120	um
Weight			-	15.0	-	g

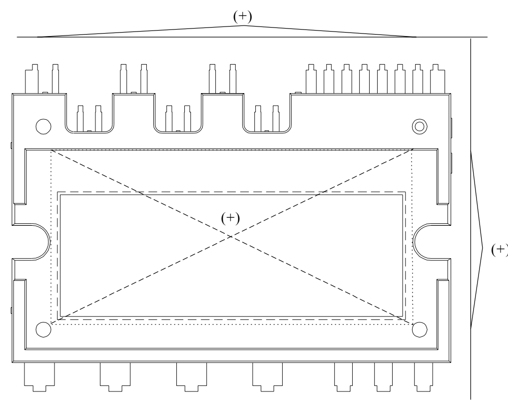
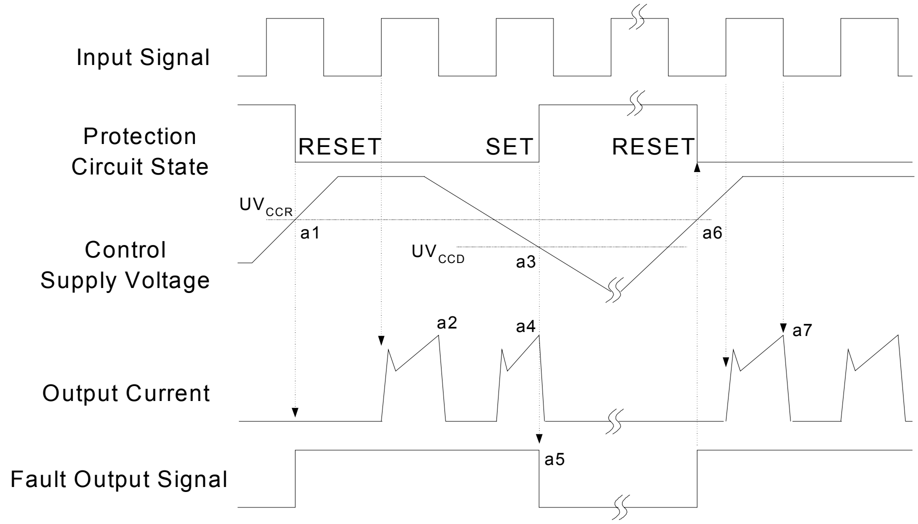


Figure 5. Flatness Measurement Position

Time Charts of Protective Function



a1 : Control supply voltage rises: After the voltage rises UV_{CCR}, the circuits start to operate when next input is applied.

a2 : Normal operation: IGBT ON and carrying current.

a3 : Under voltage detection (UV_{CCD}).

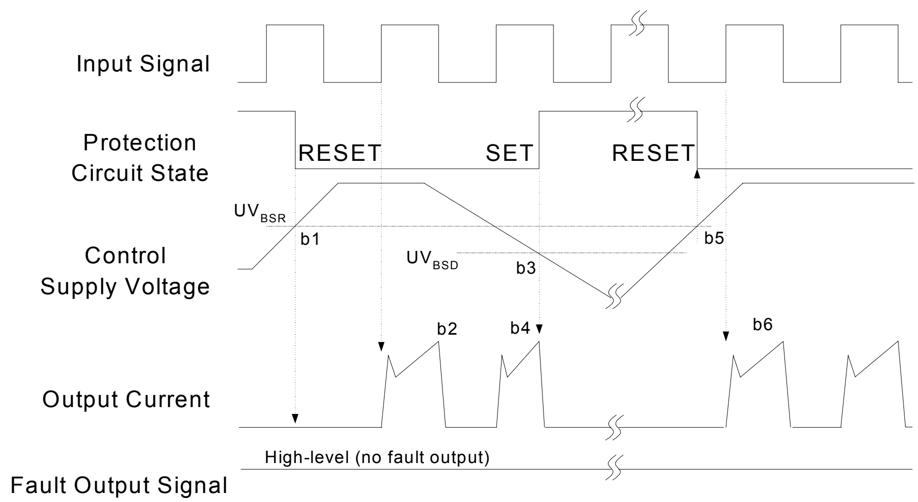
a4 : IGBT OFF in spite of control input condition.

a5 : Fault output operation starts.

a6 : Under voltage reset (UV_{CCR}).

a7 : Normal operation: IGBT ON and carrying current.

Fig. 6. Under-Voltage Protection (Low-side)



b1 : Control supply voltage rises: After the voltage reaches UV_{BSR}, the circuits start to operate when next input is applied.

b2 : Normal operation: IGBT ON and carrying current.

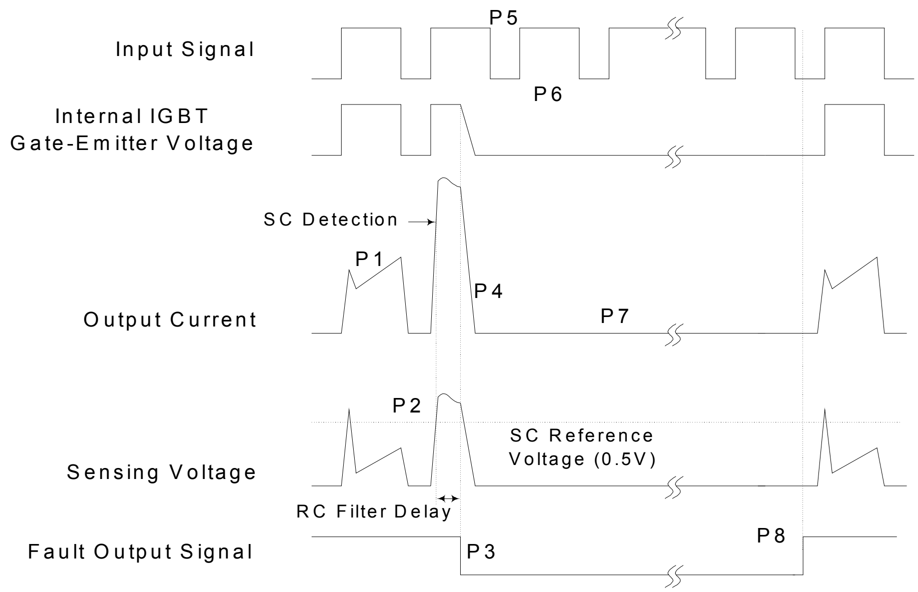
b3 : Under voltage detection (UV_{BSD}).

b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.

b5 : Under voltage reset (UV_{BSR})

b6 : Normal operation: IGBT ON and carrying current

Fig. 7. Under-Voltage Protection (High-side)



(with the external shunt resistance and CR connection)

c1 : Normal operation: IGBT ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : Hard IGBT gate interrupt.

c4 : IGBT turns OFF.

c5 : Fault output timer operation starts: The pulse width of the fault output signal is set by the external capacitor C_{FO}.

c6 : Input “L” : IGBT OFF state.

c7 : Input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.

c8 : IGBT OFF state

Fig. 8. Short-Circuit Current Protection (Low-side Operation only)

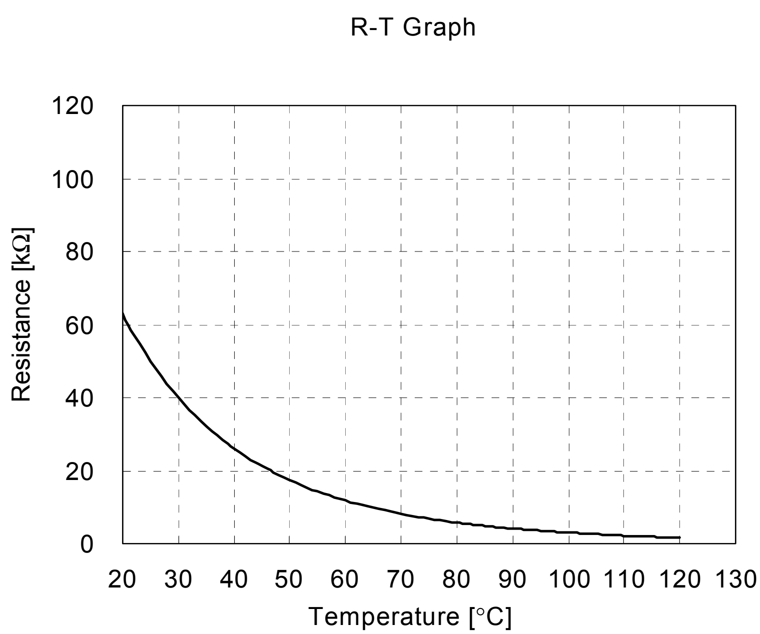
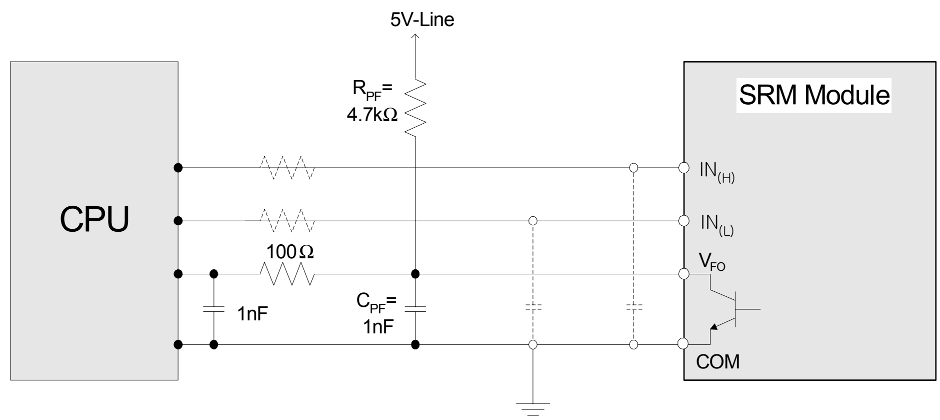


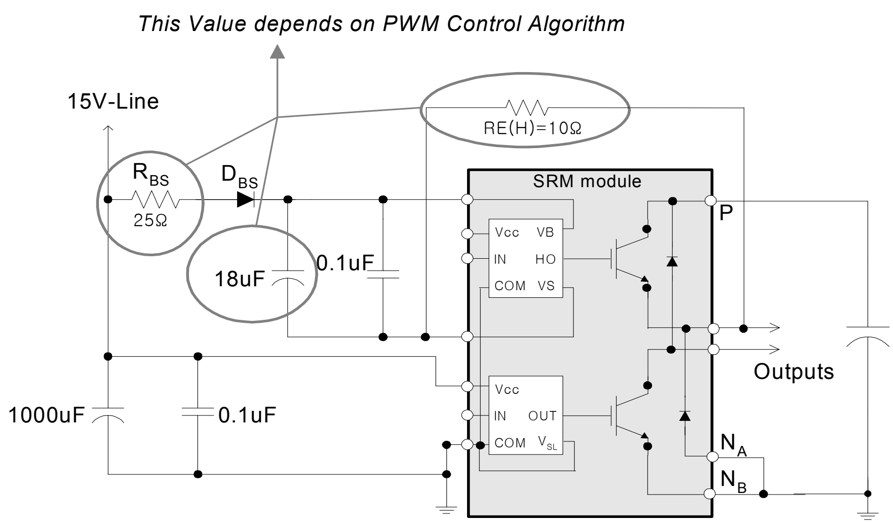
Fig. 9. R-T Curve of the Built-in Thermistor



Note:

1. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section integrates 3.3kΩ(typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.
2. The logic input is compatible with standard CMOS or LSTTL outputs.

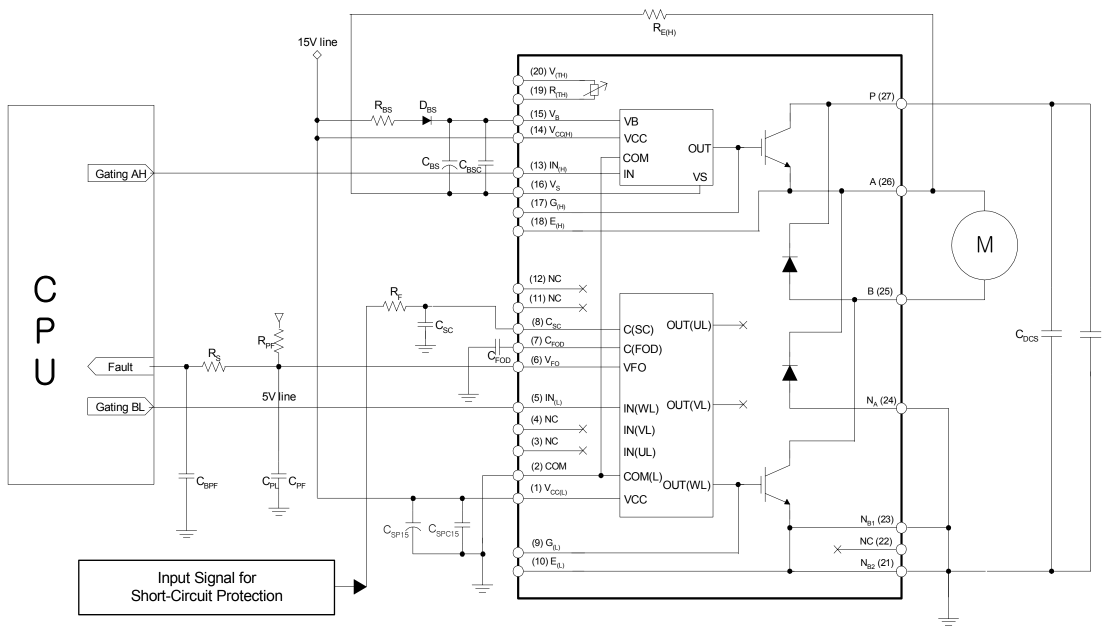
Figure 10. Recommended CPU I/O Interface Circuit



Note:

It would be recommended that the bootstrap diode, D_{BS}, has soft and fast recovery characteristics. R_{BS} should be 2.5 times greater than $R_{E(H)}$

Figure 11. Recommended Bootstrap Operation Circuit and Parameters

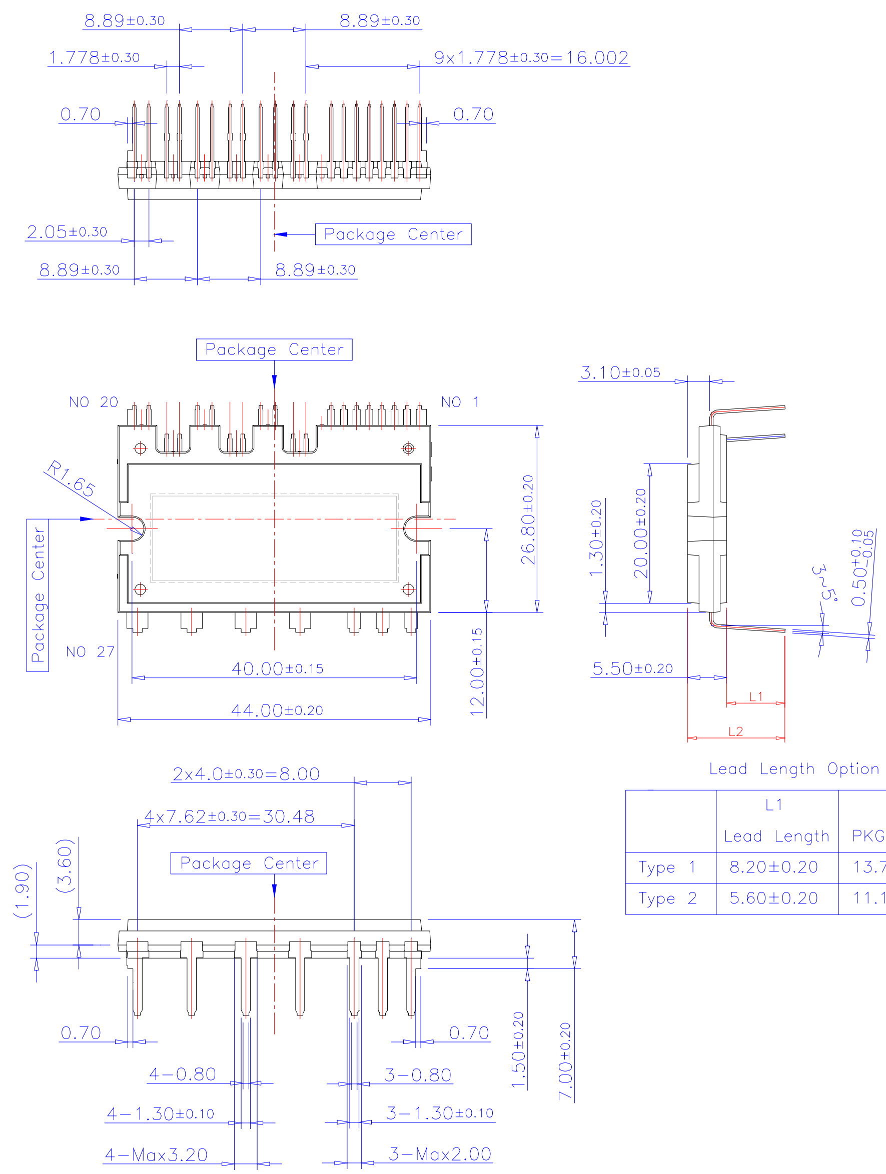


Note:

1. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)
2. By virtue of integrating an application specific type HVIC inside the Module, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. V_{FO} output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Figure 10.
4. C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.
5. V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD}(pin7) and COM(pin2). (Example : if C_{FOD} = 33 nF, then t_{FO} = 1.8ms (typ.)) Please refer to the note 6 for calculation method.
6. Input signal is High-Active type. There is a 3.3kΩ resistor inside the IC to pull down each input signal line to GND. When employing RC coupling circuits, set up such RC couple that input signal agree with turn-off/turn-on threshold voltage.
7. To prevent errors of the protection function, the wiring around R_{SC}, R_F and C_{SC} should be as short as possible.
8. In the short-circuit protection circuit, please select the $R_F C_{SC}$ time constant in the range 3~4 μs.
9. Each capacitor should be mounted as close to the pins as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22 μF between P and N pins is recommended.
11. Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays.
12. C_{SPC15} should be over 1uF and mounted as close to the pins of the module as possible.
13. N_{B1}(pin23) and N_{B2}(pin21) should be shorted externally.

Fig. 12. Application Circuit

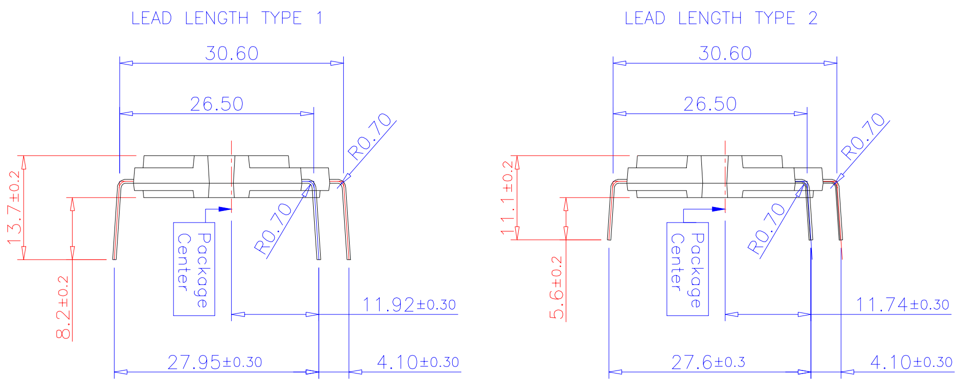
Detailed Package Outline Drawings



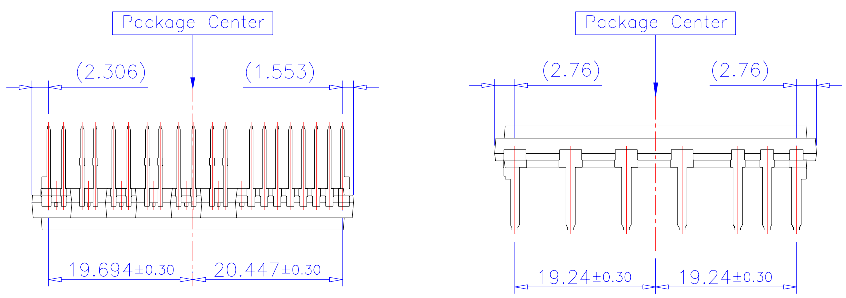
Lead Length Option

	L1 Lead Length	L2 PKG Heigth
Type 1	8.20±0.20	13.7±0.20
Type 2	5.60±0.20	11.1±0.20

Detailed Package Outline Drawings (Continued)

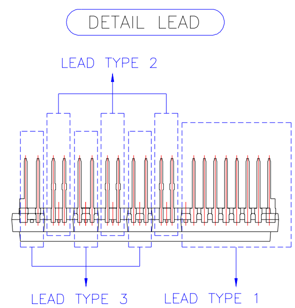


Lead Forming Dimension

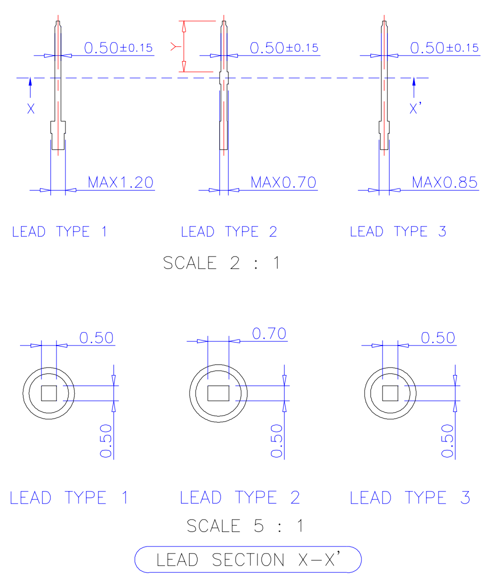


PKG Center to Lead Distance

Detailed Package Outline Drawings (Continued)



	L1 Lead Length	Y Length
Type 1	8.20±0.20	4.20±0.20
Type 2	5.60±0.20	1.60±0.20



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