

November 1999

FDP8030L/FDB8030L

N-Channel Logic Level PowerTrench® MOSFET

General Description

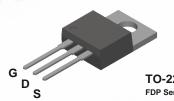
This N-Channel Logic level MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETS feature faster switching and lower gate charge than other MOSFETS with comparable $R_{\text{DS(on)}}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

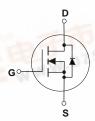
- 80 A, 30 V. $R_{DS(ON)} = 0.0035 \Omega$ @ $V_{GS} = 10 V$ $R_{DS(ON)} = 0.0045 \Omega$ @ $V_{GS} = 4.5 V$
- · Critical DC electrical parameters specified at elevated temperature
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor
- High performance trench technology for extremely low R_{DS(ON)}
- 175°C maximum junction temperature rating



TO-220 **FDP Series**



TO-263AB FDB Series



Absolute Maximum Ratings

Symbol	Parameter		Ratings	Units
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Drain Current - Continuous	(Note 1)	80	A
	- Pulsed	(Note 1)	300	DISC
P _D	Total Power Dissipation @# T _C = 25°C		187	W
	Derate al	oove 25°C	1.25	W°C
T _J , T _{STG}	Operating and Storage Junction Temperatu	ire Range	-65 to +175	°C
T _L	Maximum lead temperature for soldering pu	urposes,	275	°C

Thermal Characteristics

R _{eJC}	Thermal Resistance, Junction-to-Case	0.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	°C/W

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-Sc	ource Avalanche Ratings (Note	1)	l			
W _{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 20 \text{ V}, \qquad I_D = 80 \text{ A}$			1500	mJ
I _{AR}	Maximum Drain-Source Avalanche Current				80	Α
Off Char	acteristics					
BV _{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	30			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C		23		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			10	μA
I _{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
I _{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V}$ $V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)	1	ı			
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1	1.5	2	V
$\Delta V_{GS(th)} \over \Delta T_{,J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	· ·	- 5		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V}, \qquad I_D = 80 \text{ A} $ $T_J = 125 ^{\circ}\text{C}$		3.1 4.0	3.5 5.6	mΩ
		$V_{GS} = 4.5 \text{ V}, \qquad I_{D} = 70 \text{ A}$		3.6	4.5	
I _{D(on)}	On-State Drain Current	$V_{GS} = 10 \text{ V}, \qquad V_{DS} = 10 \text{ V}$	60			Α
g FS	Forward Transconductance	$V_{DS} = 10 \text{ V}, \qquad I_{D} = 80 \text{ A}$		170		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		10500		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		2700		pF
C _{rss}	Reverse Transfer Capacitance			1650		pF
Switchin	g Characteristics (Note 2)	•		•		
t _{D(on)}	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, \qquad I_{D} = 50 \text{ A},$		20	35	ns
t _r	Turn-On Rise Time	$V_{GS} = 4.5 \text{ V}, \qquad R_{GEN} = 10 \Omega$		185	225	ns
t _{D (off)}	Turn-Off Delay Time	$R_{GS} = 10 \Omega$		160	200	ns
t _f	Turn-Off Fall Time			200	240	ns
$\overline{Q_g}$	Total Gate Charge	V _{DS} = 15 V,		120	170	nC
Q _{gs}	Gate-Source Charge	$I_D = 80 \text{ A}, V_{GS} = 5 \text{ V}$		27		nC
Q _{gd}	Gate-Drain Charge	1		48		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings	•	•		
l _s	Maximum Continuous Drain–Source			80	Α	
I _{SM}	Maximum Pulsed Drain-Source Diode				300	Α
V _{SD}	Drain-Source Diode Forward Voltage			1	1.3	V

Notes:

^{1.} Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

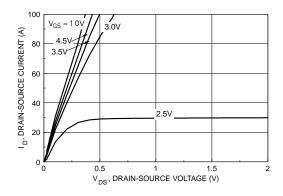
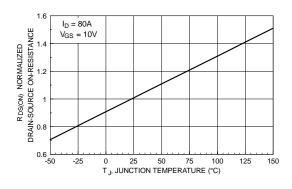


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



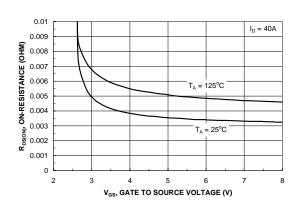
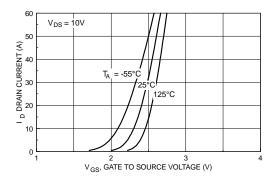


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



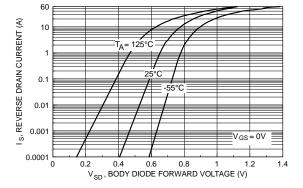
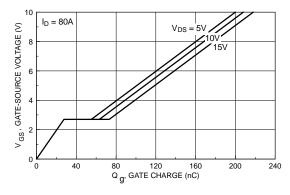


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



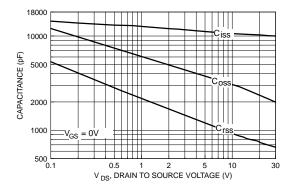
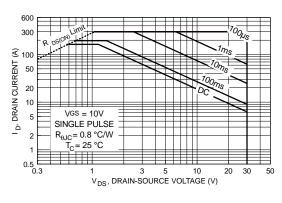


Figure 7. Gate Charge Characteristics.





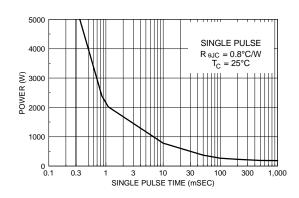


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

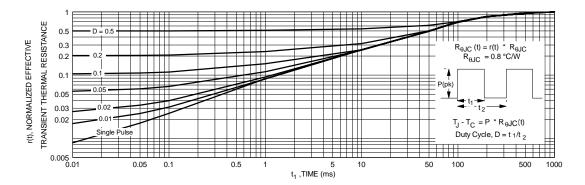
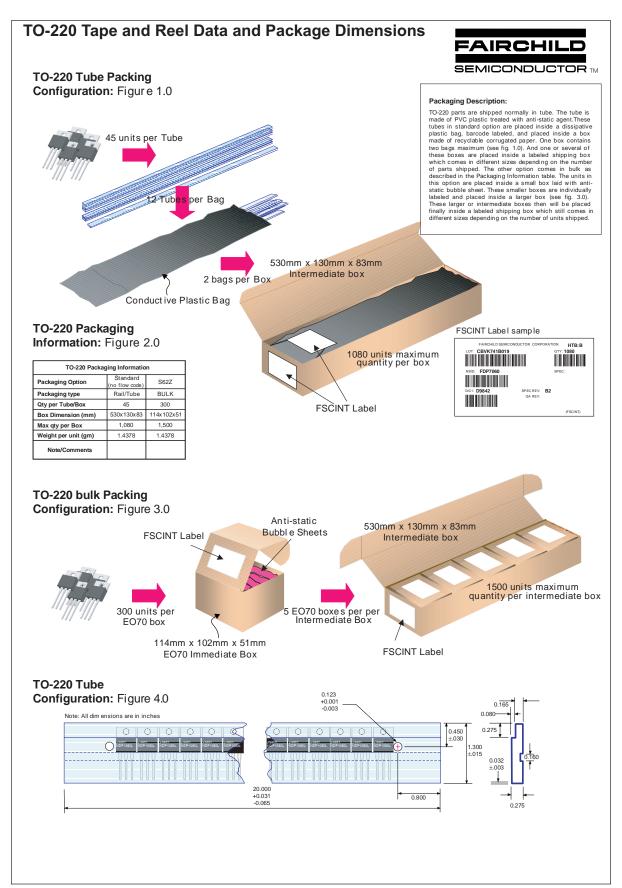


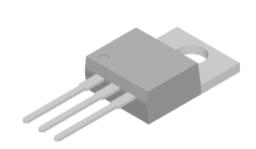
Figure 11. Transient Thermal Response Curve.

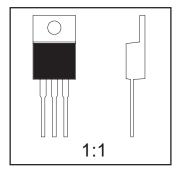
Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



TO-220 Tape and Reel Data and Package Dimensions, continued

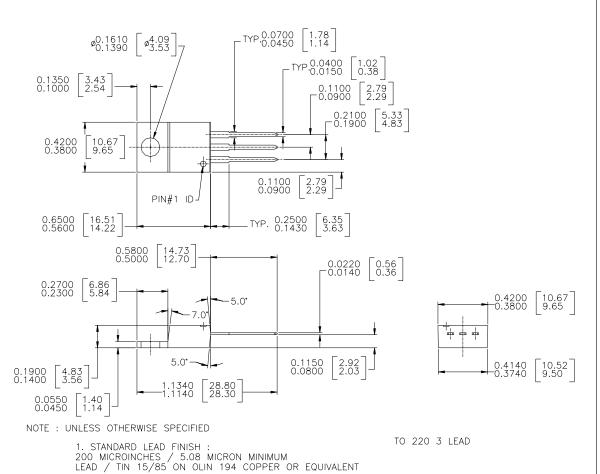
TO-220 (FS PKG Code 37)



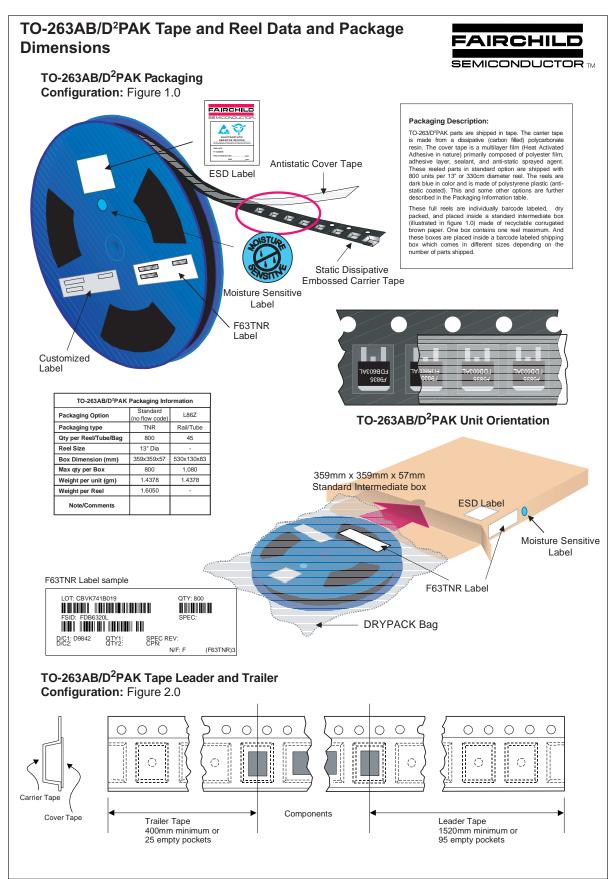


Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 1.4378

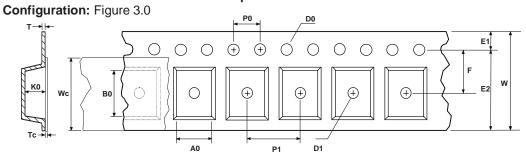


2. DIMENSION BASED ON JEDEC STANDARD TO-220 VARIATION AB, ISSUE J, DATED 3/24/87



TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

TO-263AB/D²PAK Embossed Carrier Tape



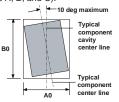
User Direction of Feed

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D ² PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

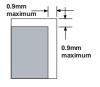
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

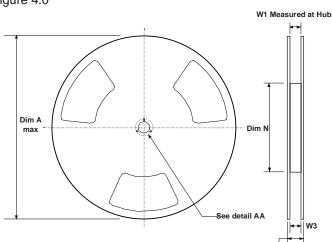


Sketch B (Top View)
Component Rotation

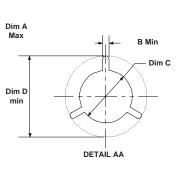


Sketch C (Top View)
Component lateral movement

TO-263AB/D²PAK Reel Configuration: Figure 4.0



13" Diameter Option



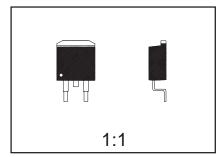
W2 max Measured at Hub

Dimensions are in inches and millimeters Reel Tape Size Dim A Dim B Dim C Dim D Dim N Dim W1 Dim W2 Dim W3 (LSL-USL) Option 512 +0.020/-0.008 13 +0.5/-0.2 0.961 +0.078/-0.000 24.4 +2/0 0.941 - 0.1.079 23.9 - 27.4 0.059 1.5 24mm 13" Dia

TO-263AB/D²PAK Tape and Reel Data and Package Dimensions, continued

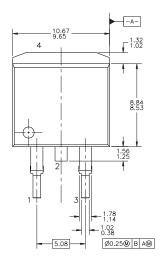
TO-263AB/D²PAK (FS PKG Code 45)

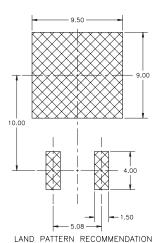


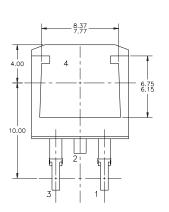


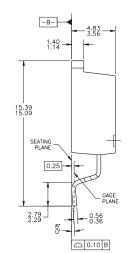
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

 A) ALL DIMENSIONS ARE IN MILLIMETERS.
 B) STANDARD LEAD FINISH:
 200 MICROINCHES / 5.08 MICROMETERS MIN.
 LEAD/TIN 15/85 ON OLIN 194 COPPER OR
 EQUIVALENT.
 C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
 TO EXCEED 0.003 INCH / 0.05mm.
 D) NO PACKAGE CHIPS, CRACKS OR SURFACE
 IDENTIFICATION ALLOWED AFTER FORMING.
 E) REFERENCE JEDEC, TO—263, ISSUE C,
 VARIATION AB, DATED 2/92.

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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