



June 2004

FDC6000NZ

Dual N-Channel 2.5V Specified PowerTrench[®] MOSFET

General Description

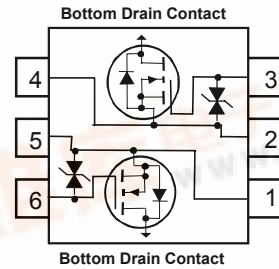
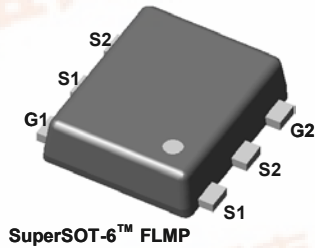
This N-Channel 2.5V specified MOSFET is a rugged gate version of Fairchild's Semiconductor's advanced PowerTrench process. It has been optimized for power management applications with a wide range of gate drive voltage (2.5V – 12V). Packaged in FLMP SSOT-6, the $R_{DS(ON)}$ and thermal properties of the device are optimized for battery power management applications.

Applications

- Battery management/Charger Application
- Load switch

Features

- 6.5 A, 20 V $R_{DS(ON)} = 20\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 28\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- ESD protection diode (note 3)
- High performance trench technology for extremely low $R_{DS(ON)}$
- FLMP SSOT-6 package: Enhanced thermal performance in industry-standard package size



MOSFET Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1a)	7.3	A
	– Pulsed	20	
P_D	Power Dissipation for Dual Operation (Note 1a)	1.6	W
	Power Dissipation for Single Operation (Note 1a)	1.8	
	(Note 1b)	1.2	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	68	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1a)	1	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.0NZ	FDC6000NZ	7"	8mm	3000 units



Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		14		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		–4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$ $V_{GS} = 4.0\text{ V}, I_D = 6.4\text{ A}$ $V_{GS} = 3.1\text{ V}, I_D = 6.3\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 5.5\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}, T_J = 125^\circ\text{C}$		16.5 16.8 19.2 22.5 22.8	20 21 24 28 30	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 6.5\text{ A}$		30		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$		840		pF
C_{oss}	Output Capacitance			210		pF
C_{rss}	Reverse Transfer Capacitance			100		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$		2.3		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 1\text{ A}, R_{GEN} = 6\ \Omega$		10	20	ns
t_r	Turn–On Rise Time			15	27	ns
$t_{d(off)}$	Turn–Off Delay Time			18	32	ns
t_f	Turn–Off Fall Time			9	18	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$		8	11	nC
Q_{gs}	Gate–Source Charge			1.5		nC
Q_{gd}	Gate–Drain Charge			2.1		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current				1.25	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.25\text{ A}$ (Note 2)		0.7	1.2	V

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Drain–Source Diode Characteristics and Maximum Ratings						
t_{rr}	Diode Reverse Recovery Time	$I_F = 6.5\text{ A}$, $d_f/d_t = 100\text{ A}/\mu\text{s}$		16		nS
Q_{rr}	Diode Reverse Recovery Charge			4.3		nC

NOTES:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $68^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper (Single Operation).

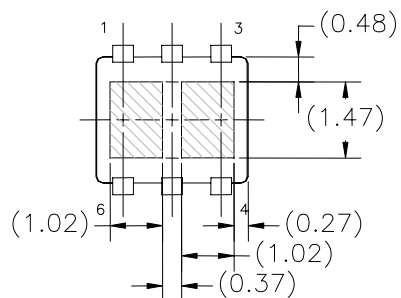


- b) $102^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper (Single Operation).

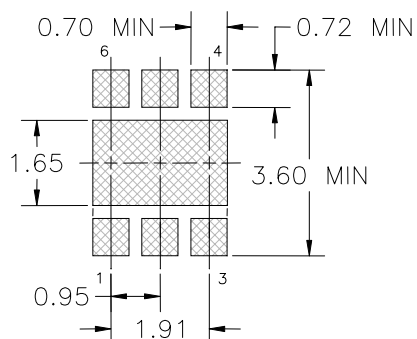
Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.
- Electrical characterization and datasheet limits was based on a single source configuration (pin 2 & 5 no connection).

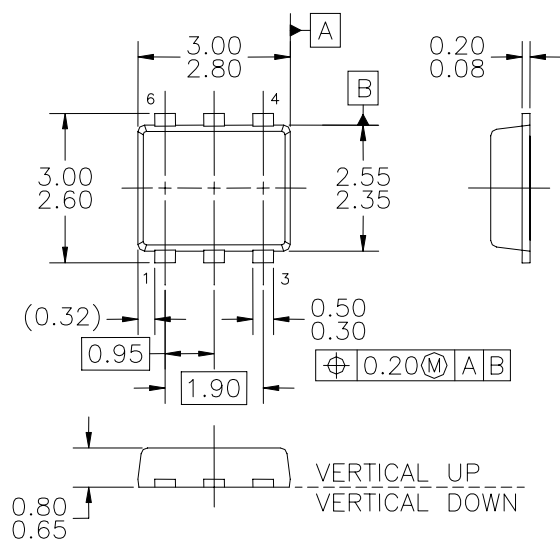
Dimensional Outline and Pad Layout



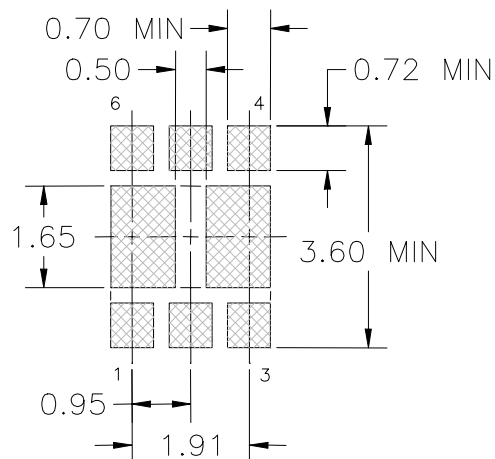
Bottom View



**Recommended Landing Pattern
For Common Drain Configuration**



Top View



**Recommended Landing Pattern
For Standard Dual Configuration**

NOTES: UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN MILLIMETERS.

Typical Characteristics

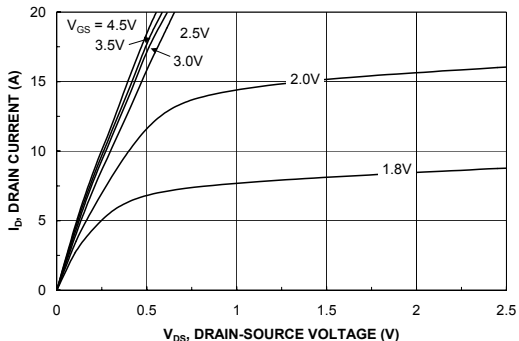


Figure 1. On-Region Characteristics.

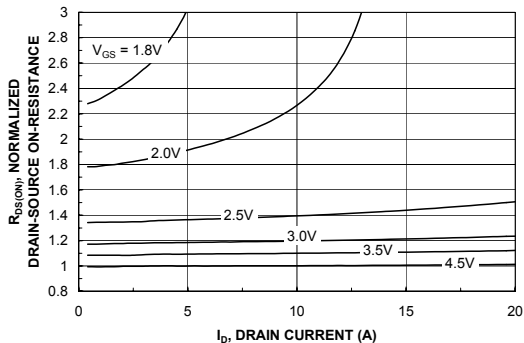


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

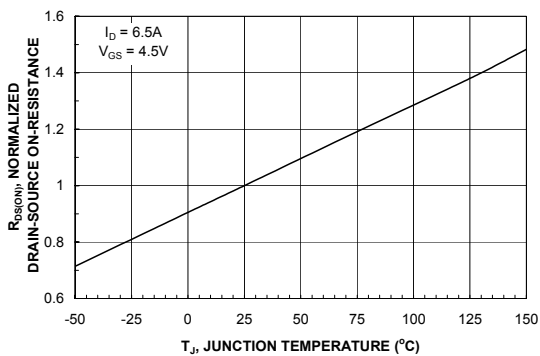


Figure 3. On-Resistance Variation with Temperature.

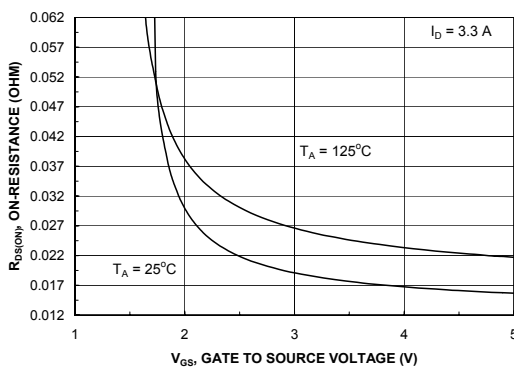


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

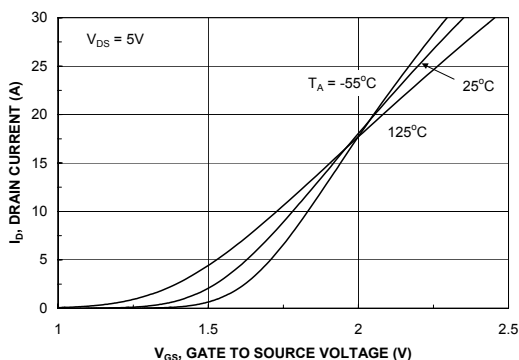


Figure 5. Transfer Characteristics.

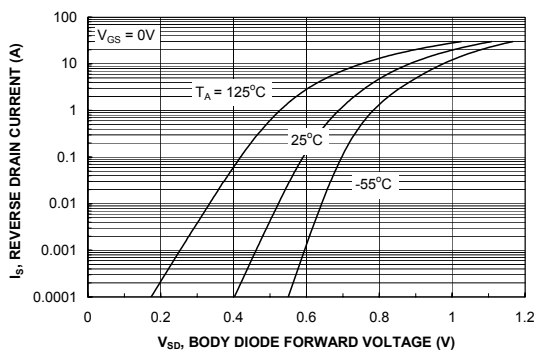


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

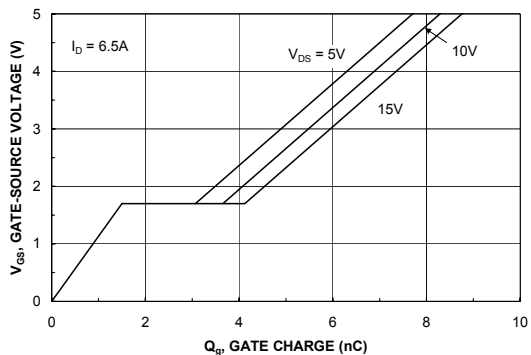


Figure 7. Gate Charge Characteristics.

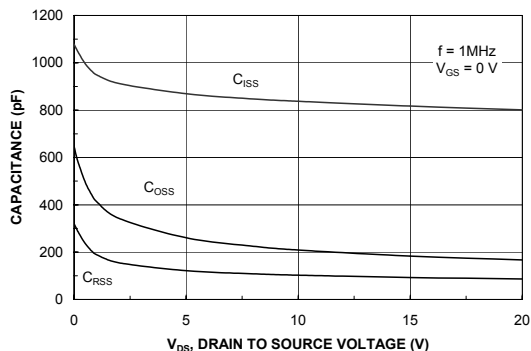


Figure 8. Capacitance Characteristics.

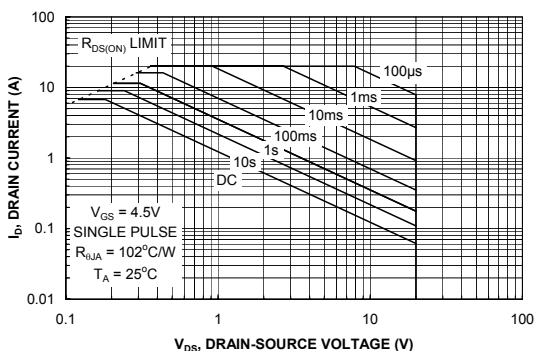


Figure 9. Maximum Safe Operating Area.

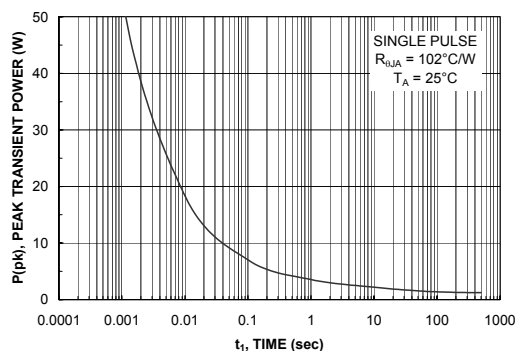


Figure 10. Single Pulse Maximum Power Dissipation.

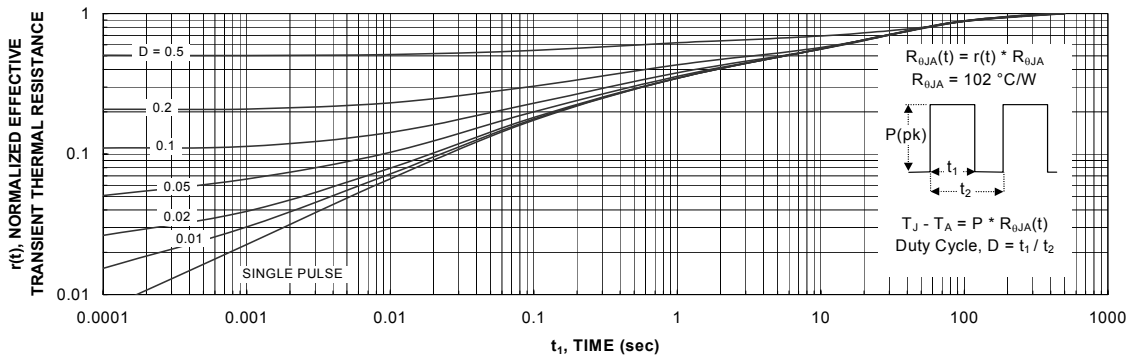


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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