



November 2003

# FDC6020C

## Complementary PowerTrench<sup>®</sup> MOSFET

### General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

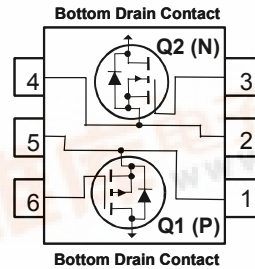
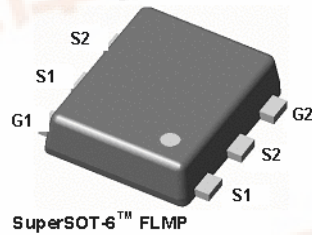
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### Applications

- DC/DC converter
- Load switch
- Motor Driving

### Features

- **Q1** -4.2 A, -20V.  $R_{DS(ON)} = 55\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$   
 $R_{DS(ON)} = 82\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
- **Q2** 5.9 A, 20V.  $R_{DS(ON)} = 27\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$   
 $R_{DS(ON)} = 39\text{ m}\Omega @ V_{GS} = 2.5\text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- FLMP SSOT-6 package: Enhanced thermal performance in industry-standard package size



### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage	-20	20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	±12	V
I <sub>D</sub>	Drain Current - Continuous (Note 1a)	-4.2	5.9	A
	- Pulsed	-20	20	
P <sub>D</sub>	Power Dissipation for Dual Operation (Note 1a)	1.6		W
	Power Dissipation for single Operation (Note 1a)	1.8		
	(Note 1b)	1.2		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	68	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1a)	1	

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.020	FDC6020C	7"	8mm	3000 units



**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

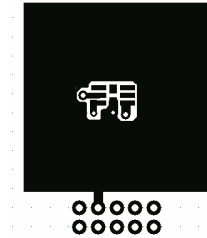
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Off Characteristics</b>							
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$ , $I_D = -250\ \mu\text{A}$ $V_{GS} = 0\text{ V}$ , $I_D = 250\ \mu\text{A}$	Q1 Q2	-20 20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		-14 12		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$ , $V_{GS} = 0\text{ V}$ $V_{DS} = 16\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			-1 1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage	$V_{GS} = +12\text{ V}$ , $V_{DS} = 0\text{ V}$ $V_{GS} = +12\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			+100 +100	nA
<b>On Characteristics (Note 2)</b>							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = -250\ \mu\text{A}$ $V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	Q1 Q2	-0.6 0.6	-1.0 1.0	-1.5 1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$ $I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	Q1 Q2		3 -3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}$ , $I_D = -4.2\text{ A}$ $V_{GS} = -2.5\text{ V}$ , $I_D = -3.4\text{ A}$ $V_{GS} = -4.5\text{ V}$ , $I_D = -4.2\text{ A}$ , $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 5.9\text{ A}$ $V_{GS} = 2.5\text{ V}$ , $I_D = 4.9\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 5.9\text{ A}$ , $T_J = 125^\circ\text{C}$	Q1 Q2		45 65 58 23 33 31	55 82 73 27 39 39	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}$ , $I_D = -4.2\text{ A}$ $V_{DS} = 5\text{ V}$ , $I_D = 5.9\text{ A}$	Q1 Q2		13 23		S
<b>Dynamic Characteristics</b>							
$C_{iss}$	Input Capacitance	Q1: $V_{DS} = -10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	Q1 Q2		753 677		pF
$C_{oss}$	Output Capacitance	Q2: $V_{DS} = 10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	Q1 Q2		163 171		pF
$C_{rss}$	Reverse Transfer Capacitance	$V_{DS} = 10\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1.0\text{ MHz}$	Q1 Q2		83 91		pF
$R_G$	Gate Resistance	$V_{GS} = 15\text{mV}$ , $f = 1.0\text{ MHz}$	Q1 Q2		8 2.2		$\Omega$
<b>Switching Characteristics</b>							
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = -10\text{ V}$ , $I_D = -1\text{ A}$ , $V_{GS} = -4.5\text{ V}$ , $R_{GEN} = 6\ \Omega$	Q1 Q2		13 11	23 20	ns
$t_r$	Turn-On Rise Time	Q2: $V_{DD} = 10\text{ V}$ , $I_D = 1\text{ A}$ , $V_{GS} = 4.5\text{ V}$ , $R_{GEN} = 6\ \Omega$	Q1 Q2		8 16	16 29	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		26 18	42 32	ns
$t_f$	Turn-Off Fall Time		Q1 Q2		14 7	52 14	ns
$Q_g$	Total Gate Charge	Q1: $V_{DS} = -10\text{ V}$ , $I_D = -4.2\text{ A}$ , $V_{GS} = -4.5\text{ V}$	Q1 Q2		7 6	10 8	nC
$Q_{gs}$	Gate-Source Charge	Q2: $V_{DS} = 10\text{ V}$ , $I_D = 5.9\text{ A}$ , $V_{GS} = 4.5\text{ V}$	Q1 Q2		1.6 1.5		nC
$Q_{gd}$	Gate-Drain Charge		Q1 Q2		1.9 1.8		nC

**Electrical Characteristics** (continued)  $T_A = 25^\circ\text{C}$  unless otherwise noted

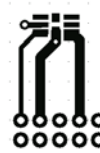
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>							
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			-1.3 1.3	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A (Note 2)}$ $V_{GS} = 0\text{ V}, I_S = 1.3\text{ A (Note 2)}$	Q1 Q2		-0.8 0.7	-1.2 1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = -4.2\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ $I_F = 5.9\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		17 15		nS
$Q_{rr}$	Diode Reverse Recovery Charge	$I_F = -4.2\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ $I_F = 5.9\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		6 4		nC

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $68^\circ\text{C/W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper (Single Operation).



b)  $102^\circ\text{C/W}$  when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

### Typical Characteristics : Q1

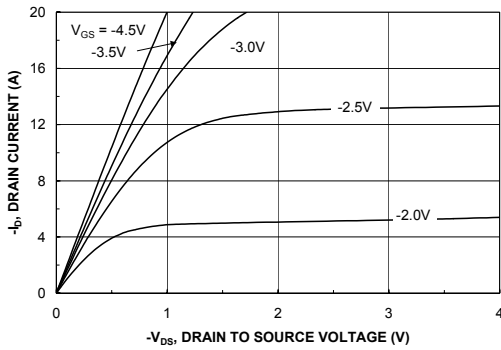


Figure 1. On-Region Characteristics.

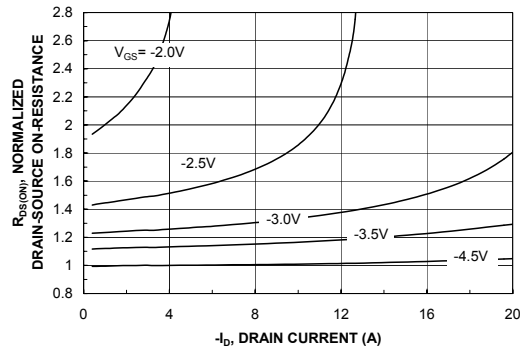


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

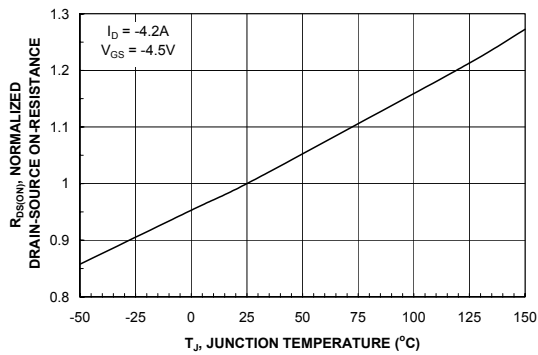


Figure 3. On-Resistance Variation with Temperature.

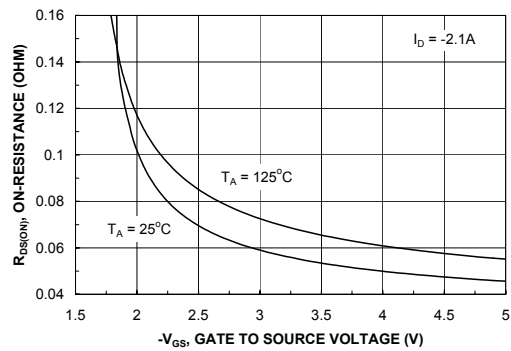


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

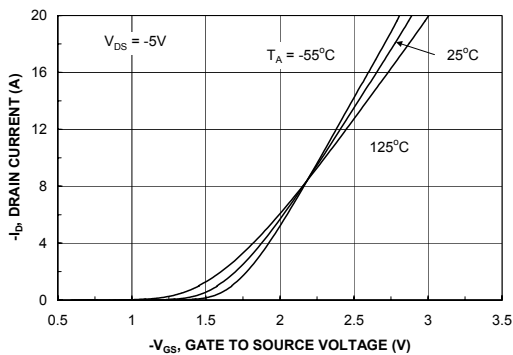


Figure 5. Transfer Characteristics.

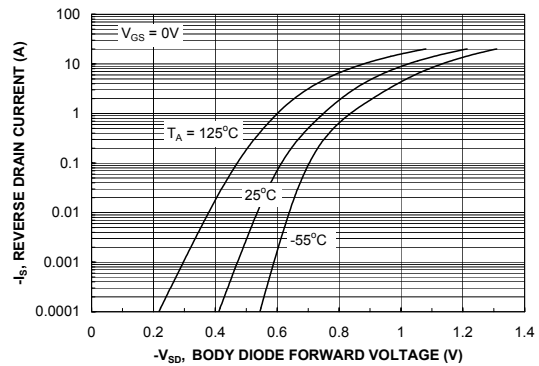
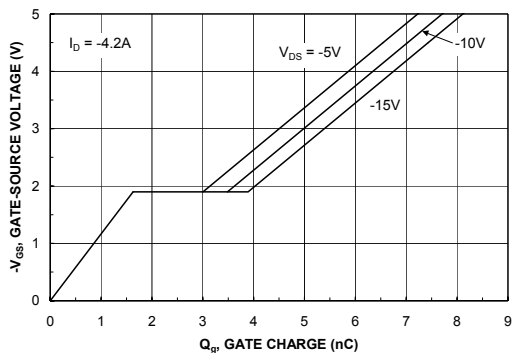
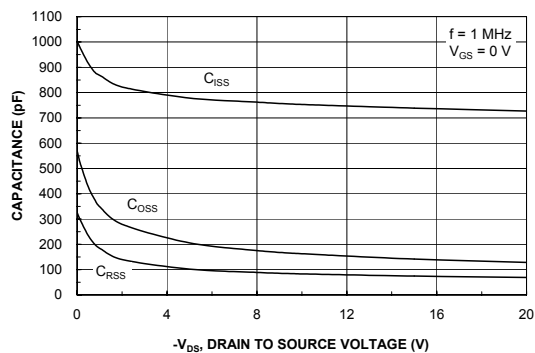


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

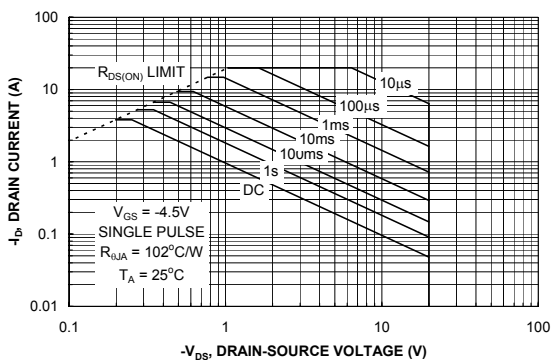
### Typical Characteristics : Q1



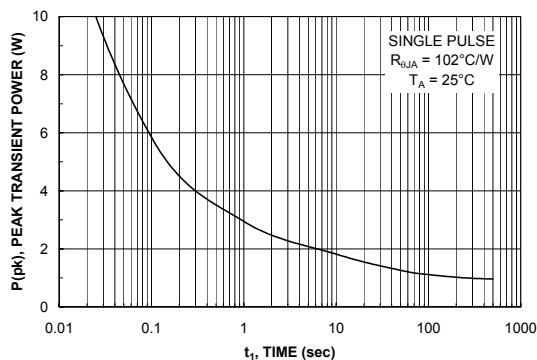
**Figure 7. Gate Charge Characteristics.**



**Figure 8. Capacitance Characteristics.**



**Figure 9. Maximum Safe Operating Area.**



**Figure 10. Single Pulse Maximum Power Dissipation.**

### Typical Characteristics : Q2

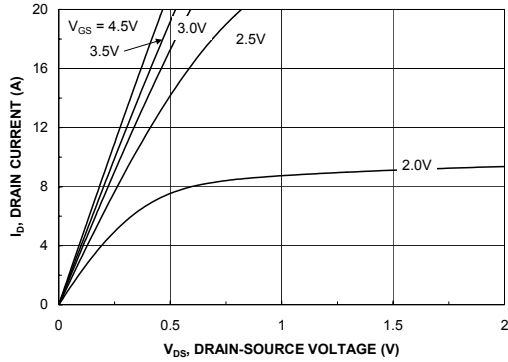


Figure 11. On-Region Characteristics.

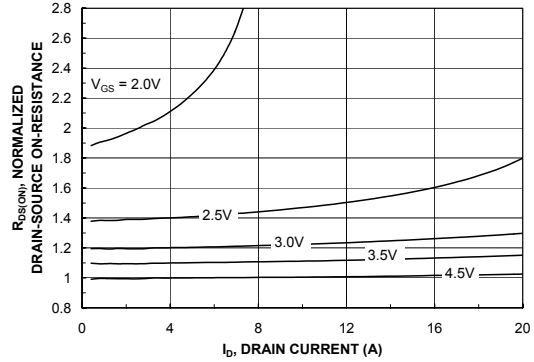


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

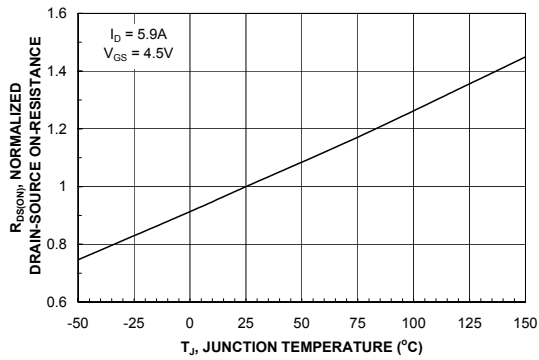


Figure 13. On-Resistance Variation with Temperature.

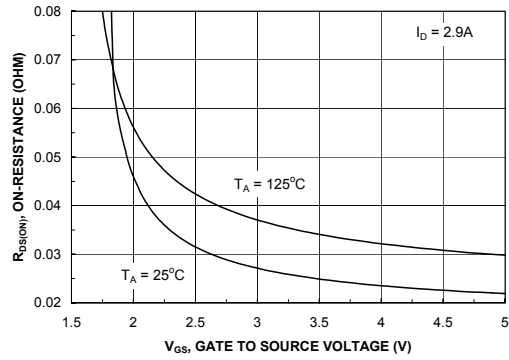


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

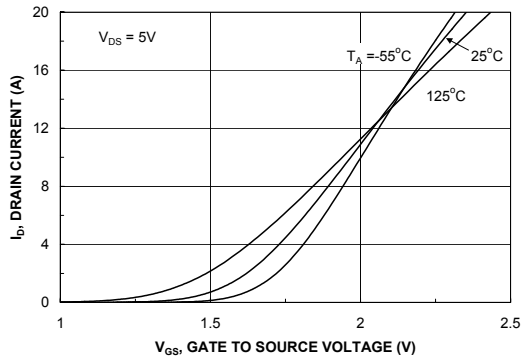


Figure 15. Transfer Characteristics.

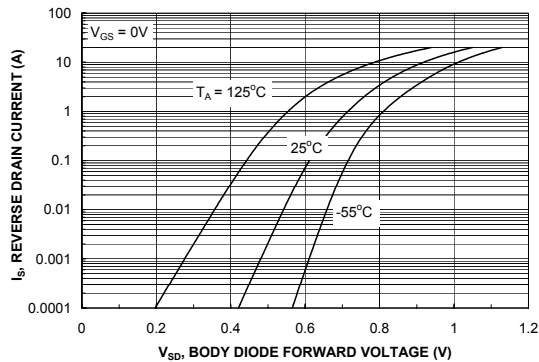
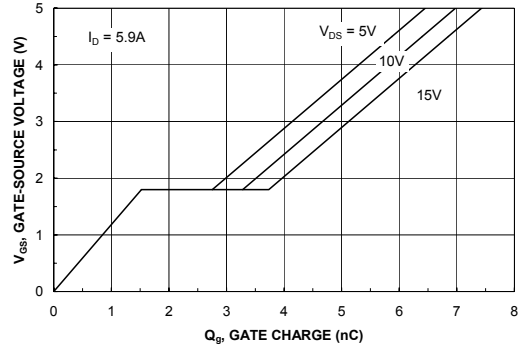
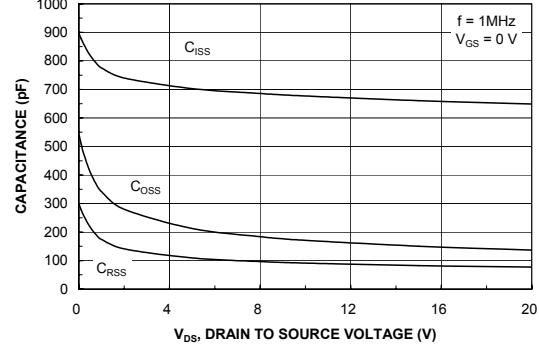


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

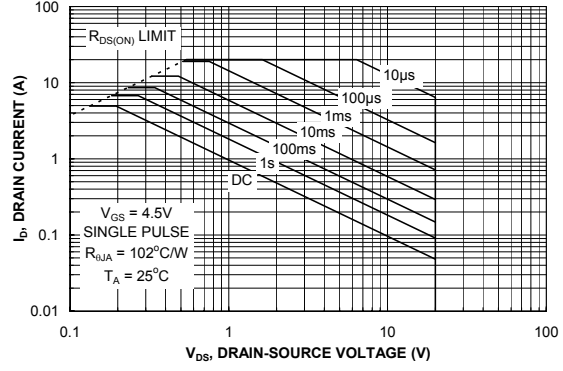
**Typical Characteristics : Q2**



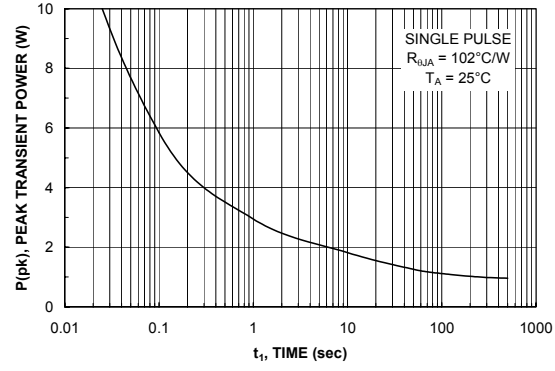
**Figure 17. Gate Charge Characteristics.**



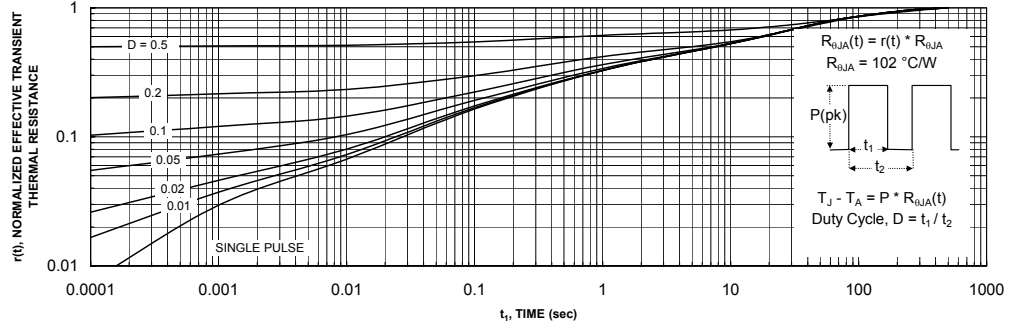
**Figure 18. Capacitance Characteristics.**



**Figure 19. Maximum Safe Operating Area.**



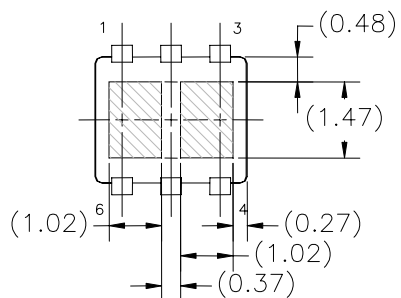
**Figure 20. Single Pulse Maximum Power Dissipation.**



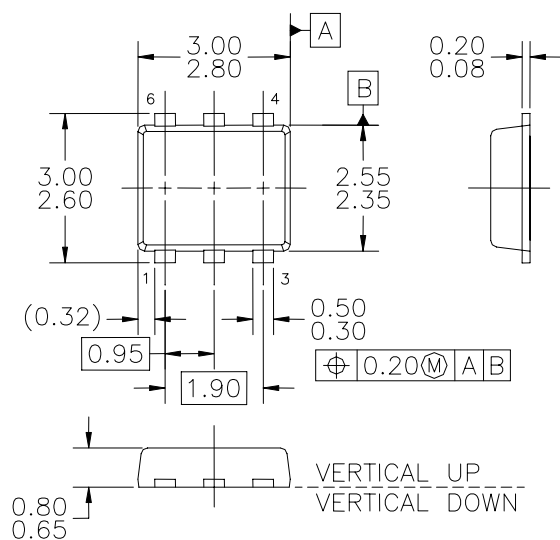
**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

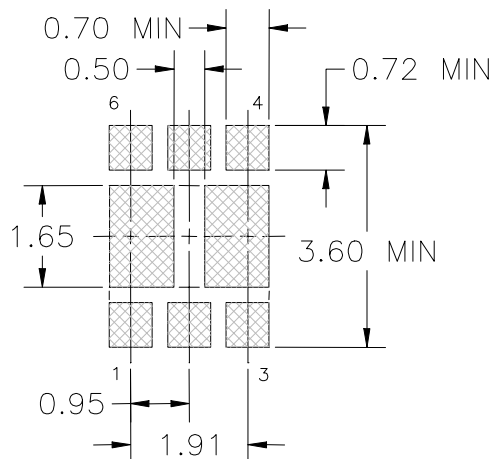
**Dimensional Outline and Pad Layout**



**Bottom View**



**Top View**



**Recommended Landing Pattern  
For Standard Dual Configuration**

NOTES: UNLESS OTHERWISE SPECIFIED

ALL DIMENSIONS ARE IN MILLIMETERS.



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EcoSPARK™	HiSeC™	MSXPro™	RapidConfigure™	UHC™
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EnSigna™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	VCX™
FACT™	ISOPLANAR™	OPTOLOGIC®	SMART START™	
Across the board. Around the world.™	OPTOPLANAR™	SPM™		
The Power Franchise™	PACMAN™	Stealth™		
Programmable Active Droop™	POP™	SuperSOT™-3		

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## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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