

July 2000 PRELIMINARY

# FDC645N

## N-Channel PowerTrench® MOSFET

#### **General Description**

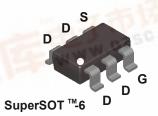
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low R<sub>DS(ON)</sub> and fast switching speed.

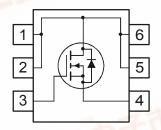
#### **Applications**

DC/DC converter

#### **Features**

- 5.5 A, 30 V.  $R_{DS(ON)} = 30 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$  $R_{DS(ON)} = 26 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
- High performance trench technology for extremely low R<sub>DS(ON)</sub>
- Low gate charge (13 nC typical)
- High power and current handling capability





Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	990	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	E8///(2/ #	30	V
V <sub>GSS</sub>	Gate-Source Voltage	A. A.	±12	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	5.5	А
	- Pulsed		20	
P <sub>D</sub>	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	- 50
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temp	erature Range	-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

Package Marking and Ordering Information

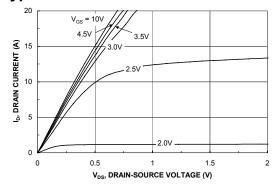
_	Device Marking	Device	Reel Size	Tape width	Quantity
_	.645	FDC645N	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics	1		I	I	I
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		22		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSSF</sub>	Gate–Body Leakage, Forward	V <sub>GS</sub> = 12 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -12 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	8.0	1.4	2	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		- 4		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	Static Drain–Source $V_{GS} = 4.5 \text{ V}, I_D = 5.5 \text{ A}$ $V_{GS} = 10 \text{ V}, I_D = 6.2 \text{ A}$				
I <sub>D(on)</sub>	On-State Drain Current	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 5 V	20			Α
<b>g</b> FS	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5.5 A		33		S
Dynamic	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 15 \text{ V},  V_{GS} = 0 \text{ V},$		1460		pF
Coss	Output Capacitance	f = 1.0 MHz		227		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	7		96		pF
Switchir	g Characteristics (Note 2)			•	•	•
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DS} = 15 \text{ V},  I_D = 1 \text{ A},$		8	16	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 6 \Omega$		9	18	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			35	56	ns
t <sub>f</sub>	Turn-Off Fall Time			7	14	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 15 \text{ V}, I_{D} = 6.2 \text{ A},$		13	21	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 4.5 V		3.6		nC
Q <sub>gd</sub>	Gate-Drain Charge	1		3.6		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings	•	•	•	•
l <sub>s</sub>	Maximum Continuous Drain–Source				1.3	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A (Note 2)		0.7	1.2	V

#### Notes:

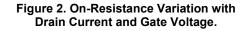
- R<sub>0JA</sub> is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.
  - a. 78°C/W when mounted on a 1in² pad of 2oz copper on FR-4 board.
  - b. 156°C/W when mounted on a minimum pad.
- 2. Pulse Test: Pulse Width  $\leq 300~\mu s,~Duty~Cycle \leq 2.0\%$

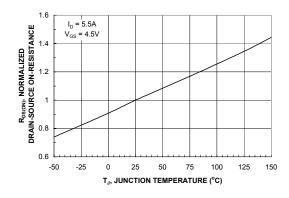
### **Typical Characteristics**



Resease NORMALIZED OR-RESISTANCE ON-RESISTANCE ON-RESISTAN

Figure 1. On-Region Characteristics.





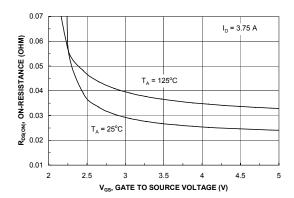
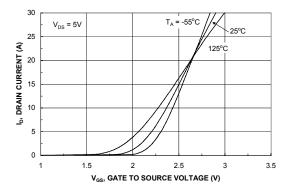


Figure 3. On-Resistance Variation withTemperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



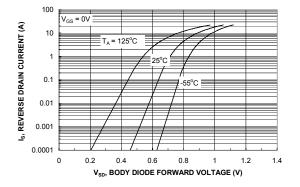
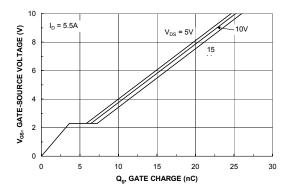


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



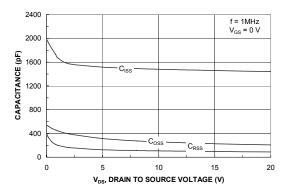


Figure 7. Gate Charge Characteristics.

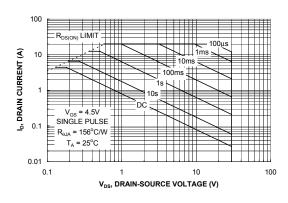


Figure 8. Capacitance Characteristics.

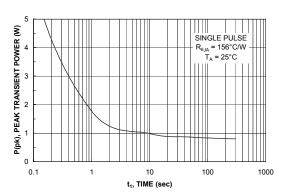


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

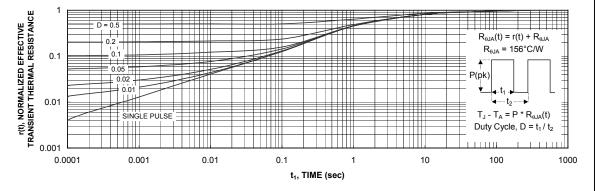
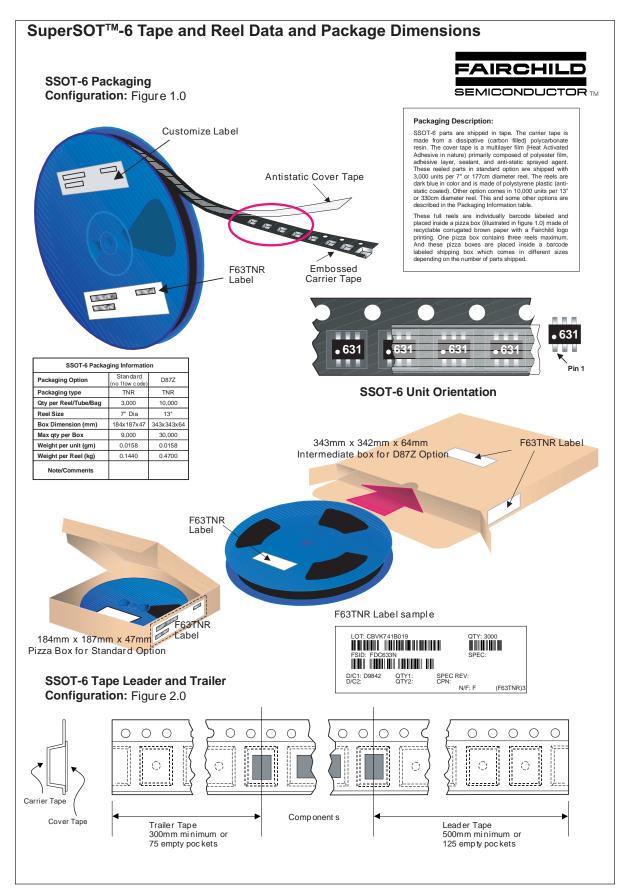


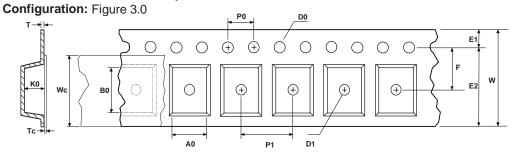
Figure 11. Transient Thermal Response Curve.

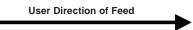
Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.



# SuperSOT<sup>™</sup>-6 Tape and Reel Data and Package Dimensions, continued

#### **SSOT-6 Embossed Carrier Tape**



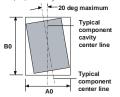


Dimensions are in millimeter														
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SSOT-6 (8mm)	3.23 +/-0.10	3.18 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



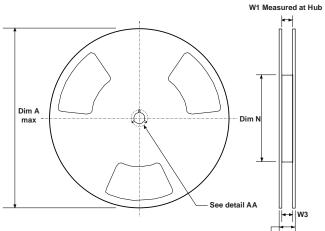
Sketch B (Top View)
Component Rotation



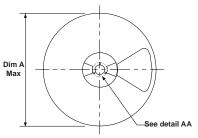
Sketch C (Top View)

Component lateral movement

# SSOT-6 Reel Configuration: Figure 4.0





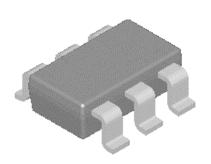


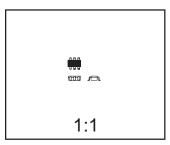
# 7" Diameter Option B Min Dim D DETAIL AA

	Dimensions are in inches and millimeters								
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

# SuperSOT<sup>™</sup>-6 Tape and Reel Data and Package Dimensions, continued

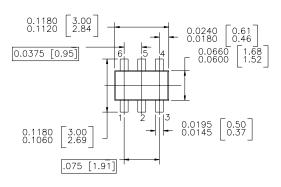
# SuperSOT -6 (FS PKG Code 31, 33)

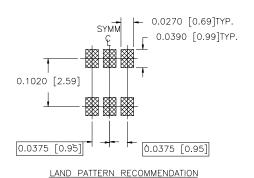




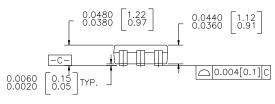
Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

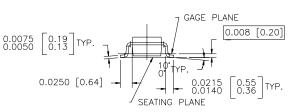
Part Weight per unit (gram): 0.0158





CONTROLLING DIMENSION IS INCH VALUES IN [ ] ARE MILLIMETERS





NOTES: UNLESS OTHERWISE SPECIFIED

1.0 STANDARD LEAD FINISH: 150 MICROINCHES 93.81 MICROMETERS) MINIMUM TIN / LEAD (SOLDER) ON COPPER.

2.0 NO JEDEC REGISTRATION AS OF JULY 1996

SUPER SOT 6 LEADS

#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

FACT Quiet Series<sup>TM</sup> QS<sup>TM</sup>
FAST $^{\otimes}$  Quiet Series<sup>TM</sup>
FASTr<sup>TM</sup> SuperSOT<sup>TM</sup>-3

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS. NOR THE RIGHTS OF OTHERS.

SuperSOT™-6

#### LIFE SUPPORT POLICY

**GTO™** 

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

SuperSOT™-8

SyncFET™

TinyLogic<sup>™</sup>

UHC™ VCX™

#### PRODUCT STATUS DEFINITIONS

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.