FAIRCHILD SEMICONDUCTOR™

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PRELIMINARY

FDD5202P

P-Channel, Logic Level, MOSFET

General Description

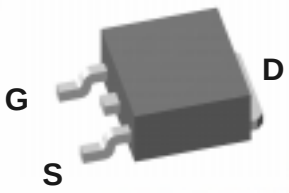
This P-Channel Logic level MOSFET is produced using Fairchild Semiconductor's advanced process that has been especially tailored to minimize the on state resistance and yet maintain low gate charge for superior switching performance.

Features

- -8 A, -60 V. $R_{DS(on)}$ = 0.3 Ω @ V_{GS} = -10 V
  $R_{DS(on)}$ = 0.5 Ω @ V_{GS} = -4.5 V.
- Low gate charge (15.5nC typical).
- Fast switching speed.

Applications

- DC/DC converter
- Motor drives
- L.D.O.



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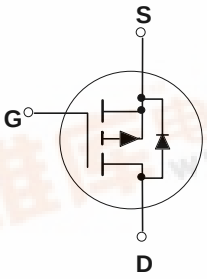

Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		-60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1)	-8	A
		(Note 1a)	-2.3	
	- Pulsed		-15	
P_D	Maximum Power Dissipation @ T_C = 25°C	(Note 1)	39	W
	T_A = 25°C	(Note 1a)	2.8	
	T_A = 25°C	(Note 1b)	1.3	
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction-to- Case	(Note 1)	3.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to- Ambient	(Note 1b)	96	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDD5202P	FDD5202P	13”	16mm	2500

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		-60		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48 V, V_{GS} = 0 V			-1	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-2	-2.3	-4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C		3.2		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.3 A V_{GS} = -10 V, I_D = -2.3 A,T_J=125°C V_{GS} = -4.5 V, I_D = -1.8 A		0.205 0.340 0.313	0.300 0.510 0.500	Ω
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-10			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -2.3 A		3		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -30 V, V_{GS} = 0 V, f = 1.0 MHz		560		pF
C_{oss}	Output Capacitance			130		pF
C_{rss}	Reverse Transfer Capacitance			35		pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -30 V, I_D = -1 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		8	15	ns
t_r	Turn-On Rise Time			20	40	ns
$t_{d(off)}$	Turn-Off Delay Time			20	40	ns
t_f	Turn-Off Fall Time			5	20	ns
Q_g	Total Gate Charge	V_{DS} = -30 V, I_D = -2.3 A, V_{GS} = -10 V		15.5	22	nC
Q_{gs}	Gate-Source Charge			2.4		nC
Q_{gd}	Gate-Drain Charge			4.7		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.2 A (Note 2)		-1	-1.3	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the drain tab. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

a) $R_{\theta JA}$= 45°C/W when mounted on a 1in² pad of 2oz copper.

b) $R_{\theta JA}$= 96°C/W when mounted on a 0.076 in² pad of 2oz copper.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

Typical Characteristics

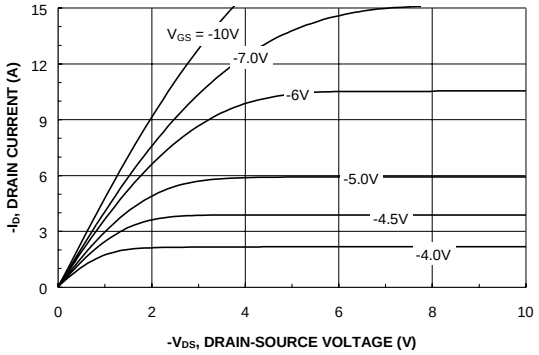

Figure 1. On-Region Characteristics.

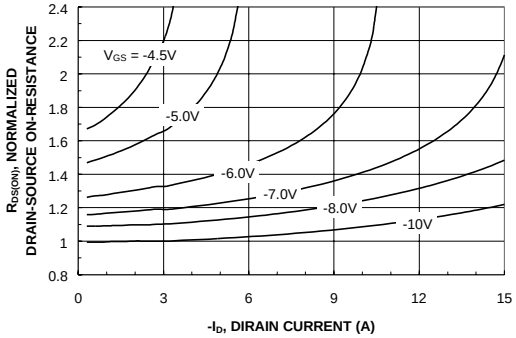

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

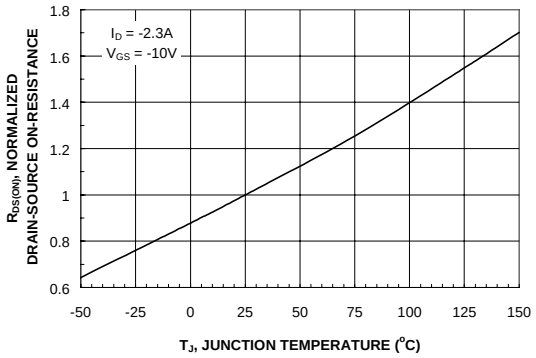

Figure 3. On-Resistance Variation with Temperature.

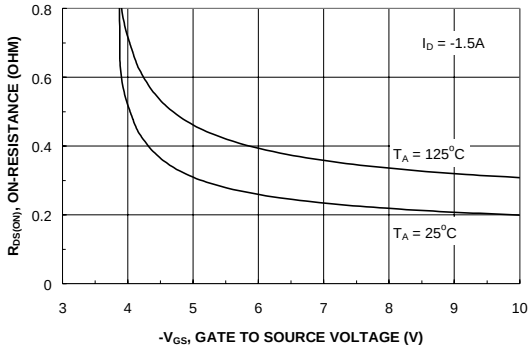

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

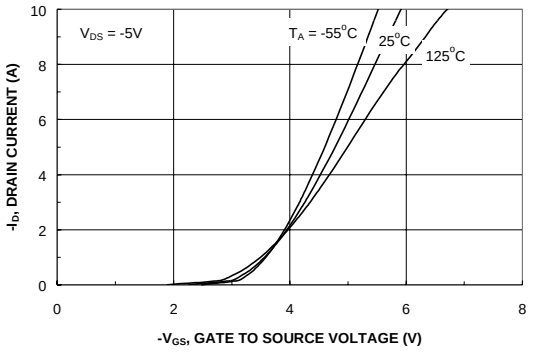

Figure 5. Transfer Characteristics.

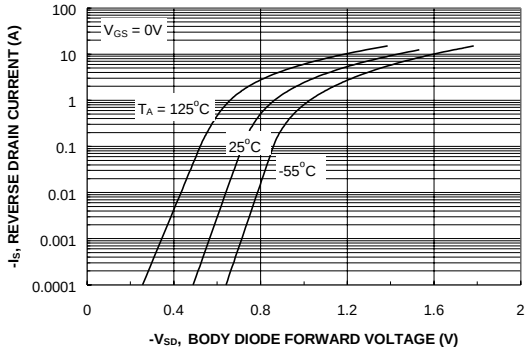

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

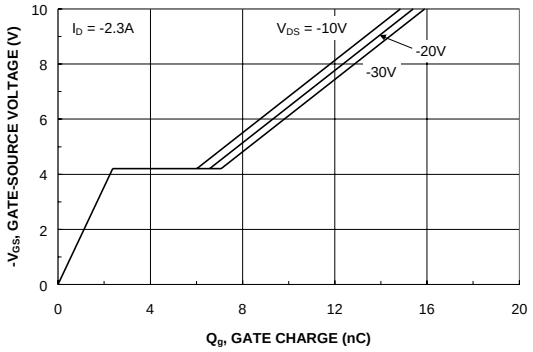

Figure 7. Gate-Charge Characteristics.

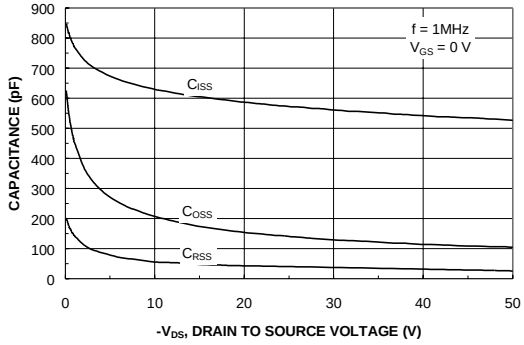

Figure 8. Capacitance Characteristics.

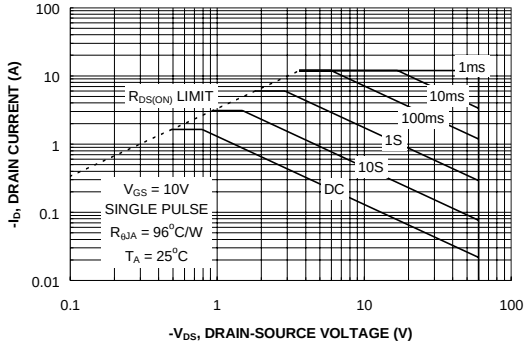

Figure 9. Maximum Safe Operating Area.

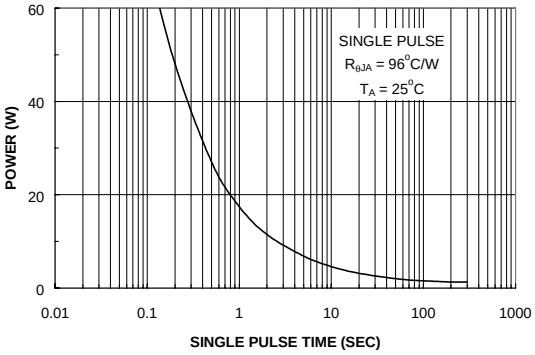

Figure 10. Single Pulse Maximum Power Dissipation.

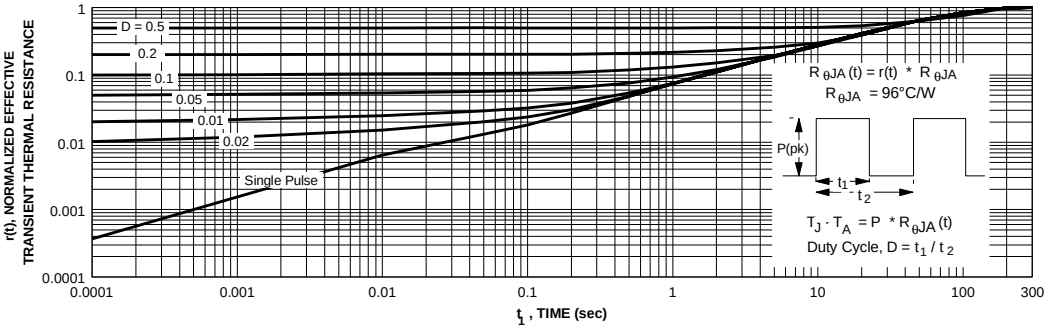

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient themal response will change depending on the circuit board design.

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