

August 2001

FDFS2P102A

Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

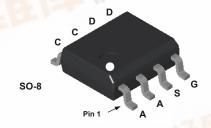
General Description

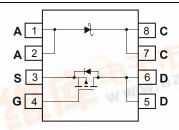
The FDFS2P102A combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in an SO-8 package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low onstate resistance. The independently connected Schottky diode allows its use in a variety of DC/DC converter topologies.

Features

- -3.3 A, -20V $R_{DS(ON)} = 125 \text{ m}\Omega$ @ $V_{GS} = -10 \text{ V}$ $R_{DS(ON)} = 200 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$
- V_F < 0.39 V @ 1 A (T_J = 125°C)
 V_F < 0.47 V @ 1 A
 V_F < 0.58 V @ 2 A
- Schottky and MOSFET incorporated into single power surface mount SO-8 package
- Electrically independent Schottky and MOSFET pinout for design flexibility





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DSS}	MOSFET Drain-Source Voltage		-20	V
V _{GSS}	MOSFET Gate-Source Voltage		±20	V
I _D	Drain Current - Continuous	(Note 1a)	-3.3	Α
	- Pulsed		-10	
P _D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
	-7 FW	(Note 1c)	0.9	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C
V_{RRM}	Schottky Repetitive Peak Reverse Voltage	Э	20	V
lo	Schottky Average Forward Current	(Note 1a)	1	Α

Package Marking and Ordering Information

Н	Device Marking	Device	Reel Size	Tape width	Quantity
	FDFS2P102A	FDFS2P102A	13"	12mm	2500 units

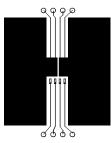
Symbol	Parameter	Test Co	onditions	Min	Тур	Max	Units
Off Char	acteristics				I	ı	I
BV _{DSS}		$V_{GS} = 0 \text{ V}, I_{D} = -2$	250 μΑ	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature	I _D = –250 μA,Ref			-23		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, \text{ V}$	_{GS} = 0 V			-1	μΑ
I _{GSSF}	Gate–Body Leakage, Forward	V_{GS} = 20 V , V	/ _{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, \text{ V}$	_{DS} = 0 V			-100	nA
On Char	acteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = -$	-250 μΑ	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient		eferenced to 25°C		4.4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10 \text{ V},$ $V_{GS} = -4.5 \text{ V},$ $V_{GS} = -10 \text{ V}, I_D = -10 \text{ V},$			96 152 137	125 200 190	mΩ
I _{D(on)}	On-State Drain Current	$V_{GS} = -10 \text{ V}, V_{D}$	_S = -5 V	-10			Α
g FS	Forward Transconductance	$V_{DS} = -5V$, $I_{D} = -3.3$ A			4.6		S
Dvnamic	Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -10 V, V _{GS} = 0 V, f = 1.0 MHz			182		pF
Coss	Output Capacitance				60		pF
C _{rss}	Reverse Transfer Capacitance				24		pF
Switchin	g Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	$V_{DD} = -10 \text{ V}, \qquad I_{D} = -1 \text{ A}, \\ V_{GS} = -10 \text{ V}, \qquad R_{GEN} = 6 \Omega$			5	10	ns
t _r	Turn-On Rise Time				14	52	ns
t _{d(off)}	Turn-Off Delay Time				11	20	ns
t _f	Turn-Off Fall Time				2	4	ns
Q _g	Total Gate Charge	$V_{DS} = -10 \text{ V},$	$I_D = -3.3 \text{ A},$		2.1	3.0	nC
Q_{gs}	Gate–Source Charge	$V_{GS} = -5 V$			1.0		nC
Q_{gd}	Gate-Drain Charge	7			0.6		nC
Drain-So	ource Diode Characteristics a	nd Maximum	Ratings				
Is	Maximum Continuous Drain-Source [-1.3	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S	= -1.3 A (Note 2)		-0.8	-1.2	V
Schottky	Diode Characteristics						
I _R	Reverse Leakage	V _R = 20 V	T _J = 25°C			50	μΑ
.,			T _J = 125°C			18	mA
V_{F}	Forward Voltage	I _F = 1 A	T _J = 25°C			0.47	V
		I _F = 2 A	$T_J = 125^{\circ}C$ $T_J = 25^{\circ}C$			0.39	
		' Z \\	$T_J = 25^{\circ}C$ $T_J = 125^{\circ}C$			0.53	

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



125°C/W when mounted on a 0.02 in² pad of 2 oz copper



135°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%

Typical Characteristics

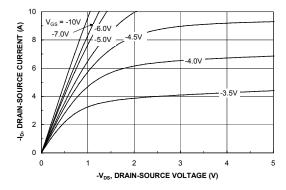


Figure 1. On-Region Characteristics.

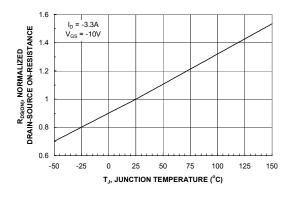


Figure 3. On-Resistance Variation with Temperature.

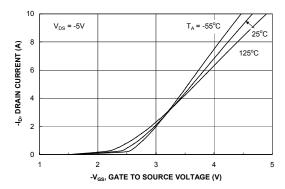


Figure 5. Transfer Characteristics.

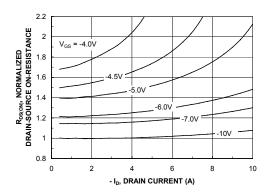


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

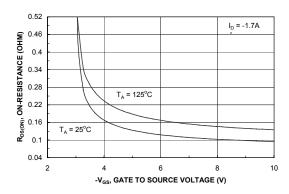


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

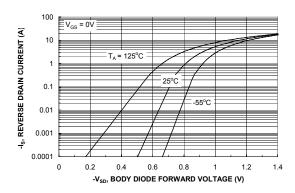
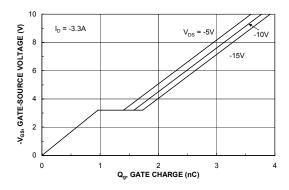


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



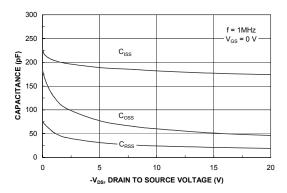


Figure 7. Gate Charge Characteristics.

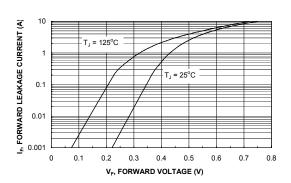


Figure 8. Capacitance Characteristics.

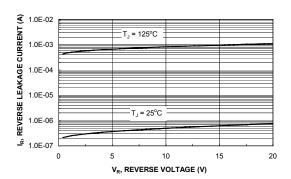


Figure 9. Schottky Diode Forward Voltage.



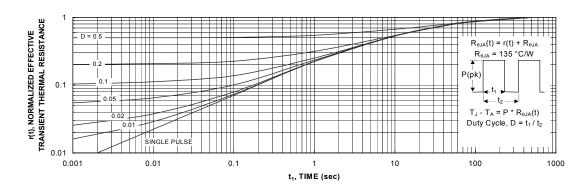


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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