

FAIRCHILD
SEMICONDUCTOR®

February 2003

FDH038AN08A1
N-Channel PowerTrench® MOSFET
75V, 80A, 3.8mΩ

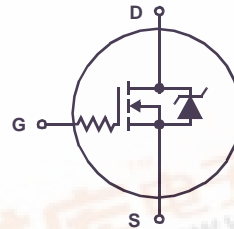
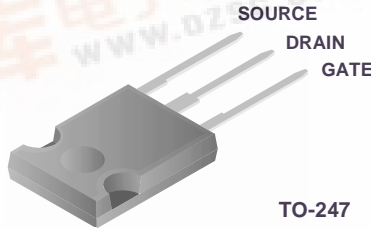
Features

- $r_{DS(ON)} = 3.5m\Omega$ (Typ.), $V_{GS} = 10V$, $I_D = 80A$
- $Q_g(tot) = 125nC$ (Typ.), $V_{GS} = 10V$
- Internal Gate Resistor, $R_g = 20\Omega$ (Typ.)
- Low Miller Charge
- Low Q_{RR} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- Qualified to AEC Q101

Applications

- 42V Automotive Load Control
- Starter / Alternator Systems
- Electronic Power Steering Systems
- Electronic Valve Train Systems
- DC-DC converters and Off-line UPS
- Distributed Power Architectures and VRMs
- Primary Switch for 24V and 48V systems

Formerly developmental type 82690



MOSFET Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	75	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current		
	Continuous ($T_C < 158^\circ C$, $V_{GS} = 10V$)	80	A
	Continuous ($T_A = 25^\circ C$, $V_{GS} = 10V$, with $R_{\theta JA} = 30^\circ C/W$)	22	A
	Pulsed	Figure 4	A
E_{AS}	Single Pulse Avalanche Energy (Note 1)	1.17	J
P_D	Power dissipation	450	W
	Derate above $25^\circ C$	3.0	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ C$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance Junction to Case TO-247	0.33	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-247	30	$^\circ C/W$

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild Semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.



Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDH038AN08A1	FDH038AN08A1	TO-247	Tube	N/A	30 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	75	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$ $V_{GS} = 0\text{V}$ $T_C = 150^\circ\text{C}$	-	-	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	-	4	V
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 80\text{A}, V_{GS} = 10\text{V}$	-	0.0035	0.0038	Ω
		$I_D = 40\text{A}, V_{GS} = 6\text{V}$	-	0.0047	0.0071	
		$I_D = 80\text{A}, V_{GS} = 10\text{V},$ $T_J = 175^\circ\text{C}$	-	0.0074	0.008	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	8665	-	pF
C_{OSS}	Output Capacitance		-	1320	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	340	-	pF
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V to } 10\text{V}$	-	125	160	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0\text{V to } 2\text{V}$	-	17	22	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 40\text{V}$ $I_D = 80\text{A}$ $I_g = 1.0\text{mA}$	-	57	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau		-	42	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	30	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 40\text{V}, I_D = 80\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 2.4\Omega$	-	-	345	ns
$t_{d(ON)}$	Turn-On Delay Time		-	88	-	ns
t_r	Rise Time		-	141	-	ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	232	-	ns
t_f	Fall Time		-	126	-	ns
t_{OFF}	Turn-Off Time		-	-	530	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 80\text{A}$	-	-	1.25	V
		$I_{SD} = 40\text{A}$	-	-	1.0	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 75\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	50	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 75\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	65	nC

Notes:

1: Starting $T_J = 25^\circ\text{C}$, $L = 0.65\text{mH}$, $I_{AS} = 60\text{A}$.

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

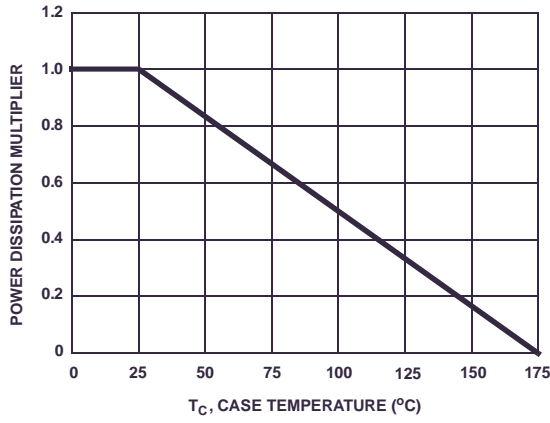


Figure 1. Normalized Power Dissipation vs Ambient Temperature

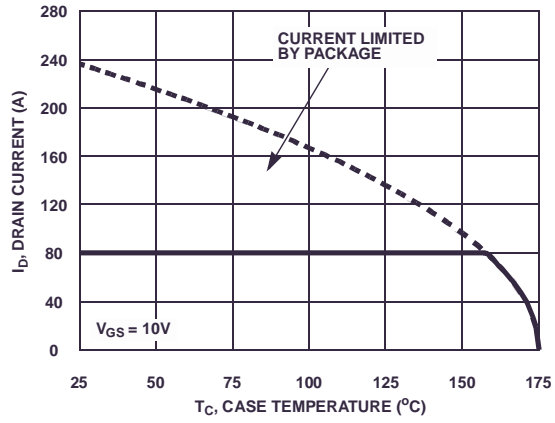


Figure 2. Maximum Continuous Drain Current vs Case Temperature

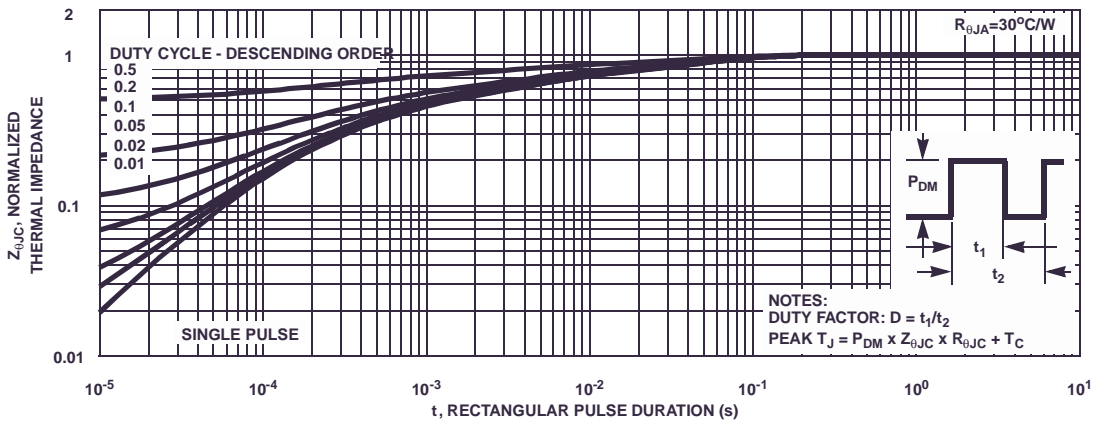


Figure 3. Normalized Maximum Transient Thermal Impedance

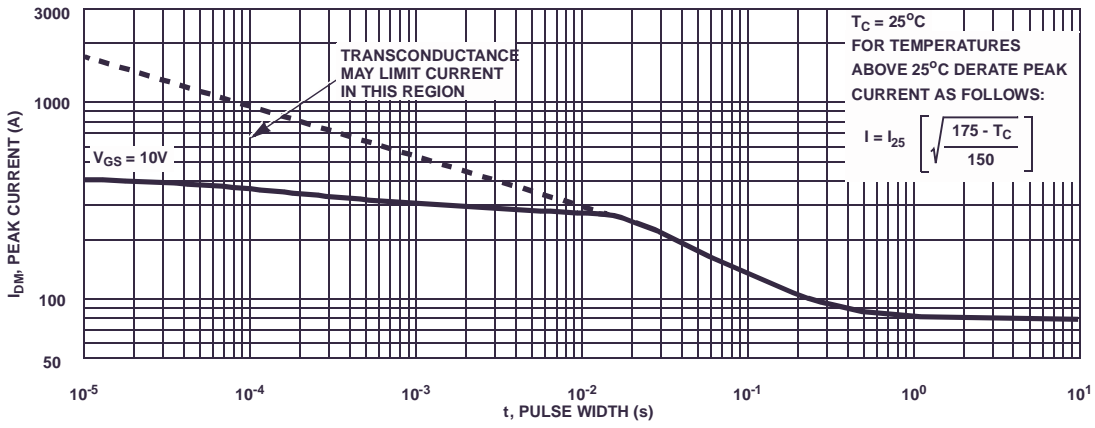


Figure 4. Peak Current Capability

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

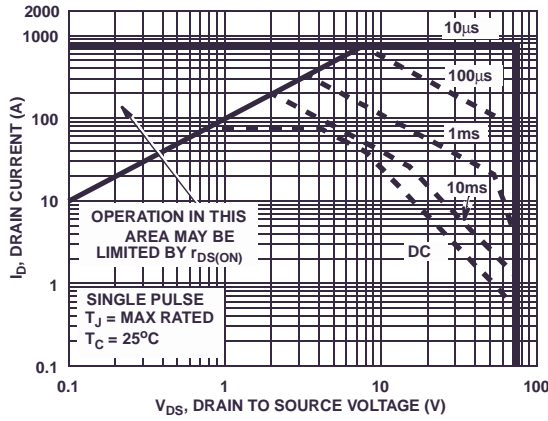
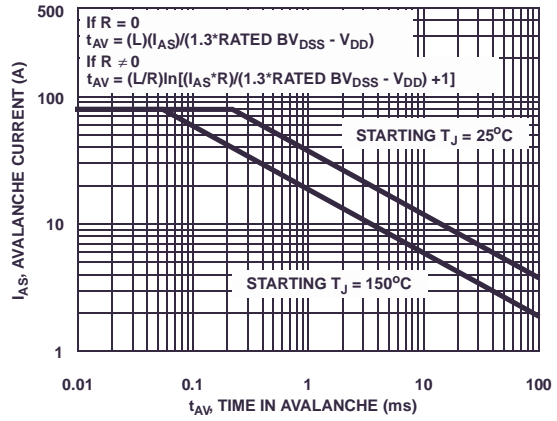


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515
Figure 6. Unclamped Inductive Switching Capability

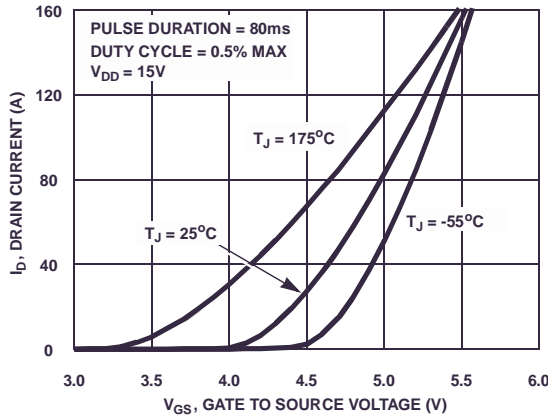


Figure 7. Transfer Characteristics

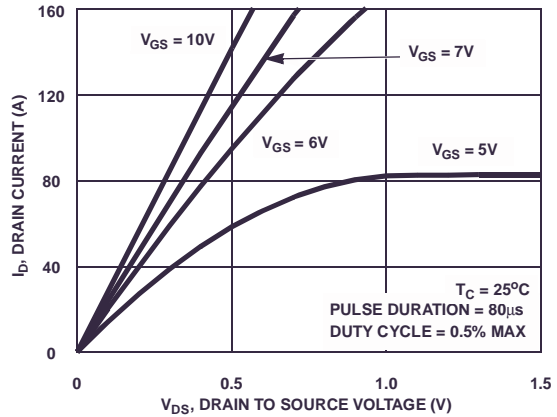


Figure 8. Saturation Characteristics

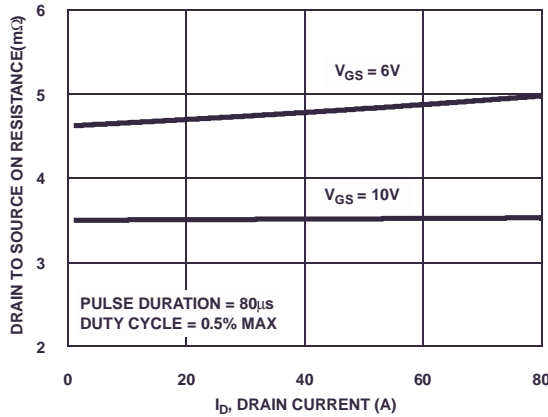


Figure 9. Drain to Source On Resistance vs Drain Current

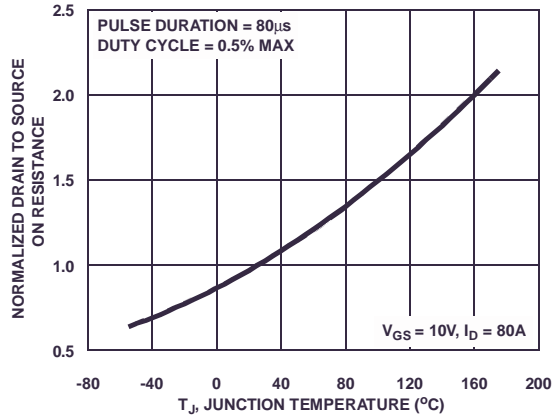


Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature

Typical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

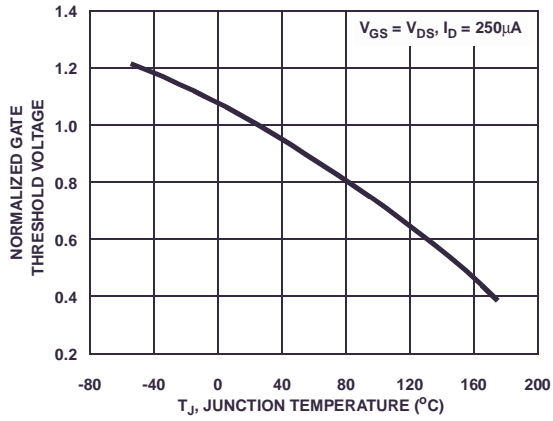


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

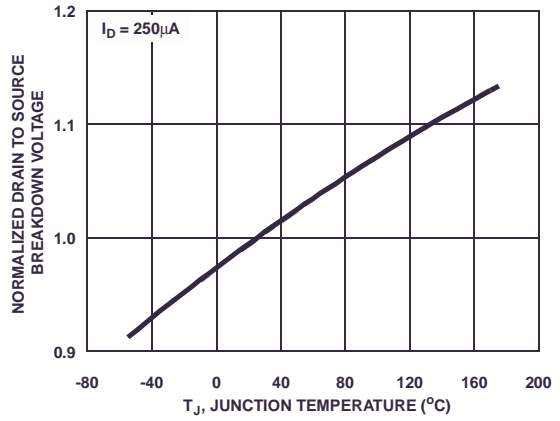


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

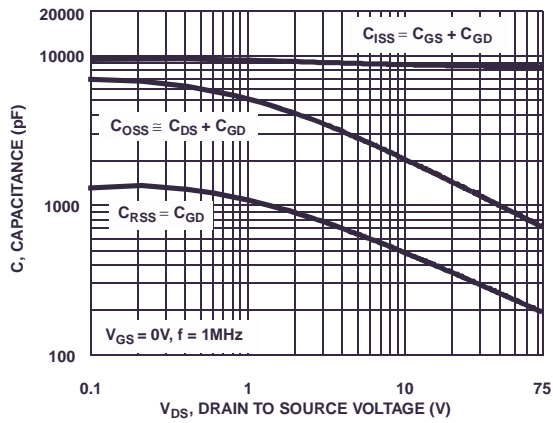


Figure 13. Capacitance vs Drain to Source Voltage

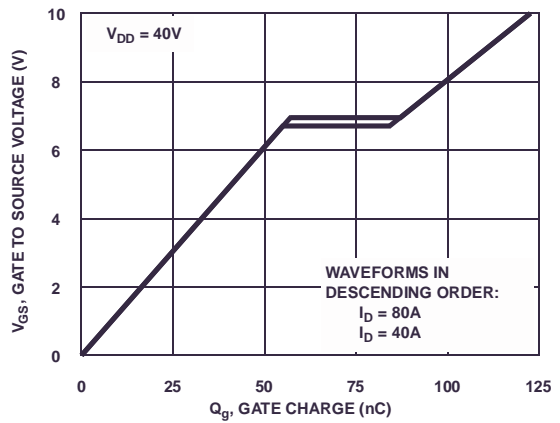


Figure 14. Gate Charge Waveforms for Constant Gate Currents

Test Circuits and Waveforms

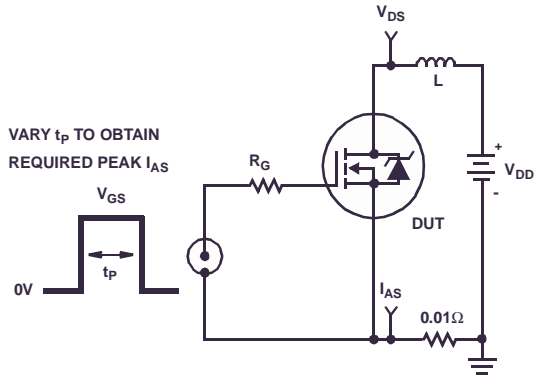


Figure 15. Unclamped Energy Test Circuit

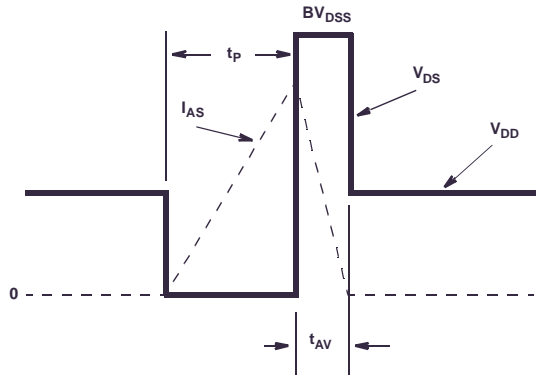


Figure 16. Unclamped Energy Waveforms

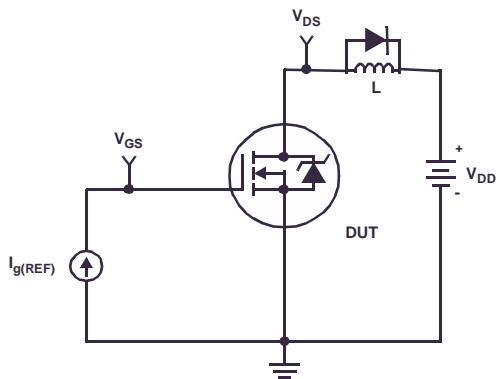


Figure 17. Gate Charge Test Circuit

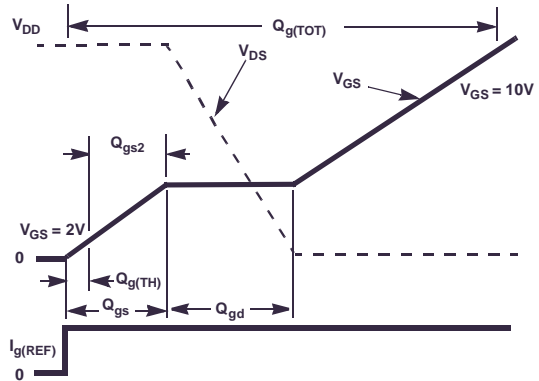


Figure 18. Gate Charge Waveforms

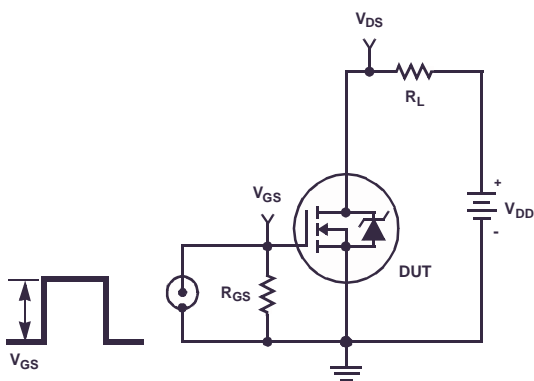


Figure 19. Switching Time Test Circuit

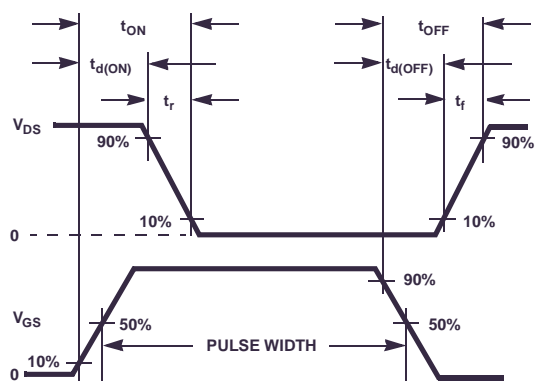


Figure 20. Switching Time Waveforms

PSPICE Electrical Model

.SUBCKT FDH038AN08A1 2 1 3 ; rev January 2003

CA 12 8 1.0e-9

Cb 15 14 3.1e-9

Cin 6 8 8.22e-9

Dbody 7 5 DbodyMOD

Dbreak 5 11 DbreakMOD

Dplcap 10 5 DplcapMOD

Ebreak 11 7 17 18 84.9

Eds 14 8 5 8 1

Egs 13 8 6 8 1

Esg 6 10 6 8 1

Evtbres 6 21 19 8 1

Evttemp 20 6 18 22 1

It 8 17 1

Lgate 1 9 4.81e-9

Ldrain 2 5 1.0e-9

Lsource 3 7 4.63e-9

RLgate 1 9 48.1

RLdrain 2 5 10

RLsource 3 7 46.3

Mmed 16 6 8 8 MmedMOD

Mstro 16 6 8 8 MstroMOD

Mweak 16 21 8 8 MweakMOD

Rbreak 17 18 RbreakMOD 1

Rdrain 50 16 RdrainMOD 2.0e-4

Rgate 9 20 20

Rslc1 5 51 RslcMOD 1.0e-6

Rslc2 5 50 1e3

Rsource 8 7 RsourceMOD 2.6e-3

Rvthres 22 8 RvthresMOD 1

Rvtemp 18 19 RvtempMOD 1

S1a 6 12 13 8 S1AMOD

S1b 13 12 13 8 S1BMOD

S2a 6 15 14 13 S2AMOD

S2b 13 15 14 13 S2BMOD

Vbat 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51))/(1e-6*300),10))}}

.MODEL DbodyMOD D (IS=2.4E-11 N=1.02 RS=1.65e-3 TRS1=3.2e-3 TRS2=2.0e-7

+ CJO=6.0e-9 M=5.6e-1 TT=2.38e-8 XTI=3.9)

.MODEL DbreakMOD D (RS=1.5e-1 TRS1=1.0e-3 TRS2=-8.9e-6)

.MODEL DplcapMOD D (CJO=1.5e-9 IS=1.0e-30 N=10 M=0.47)

.MODEL MmedMOD NMOS (VTO=3.2 KP=1.5 IS=1.0e-30 N=10 TOX=1 L=1u W=1u RG=20)

.MODEL MstroMOD NMOS (VTO=3.95 KP=235 IS=1.0e-30 N=10 TOX=1 L=1u W=1u)

.MODEL MweakMOD NMOS (VTO=2.73 KP=0.02 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=200 RS=.01)

.MODEL RbreakMOD RES (TC1=1.05e-3 TC2=-9.0e-7)

.MODEL RdrainMOD RES (TC1=1.8e-2 TC2=2.2e-4)

.MODEL RslcMOD RES (TC1=2.0e-3 TC2=1.0e-5)

.MODEL RsourceMOD RES (TC1=5.0e-3 TC2=1.0e-6)

.MODEL RvthresMOD RES (TC1=-4.2e-3 TC2=-1.8e-5)

.MODEL RvtempMOD RES (TC1=-4.5e-3 TC2=2.0e-6)

.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-4 VOFF=-1.5)

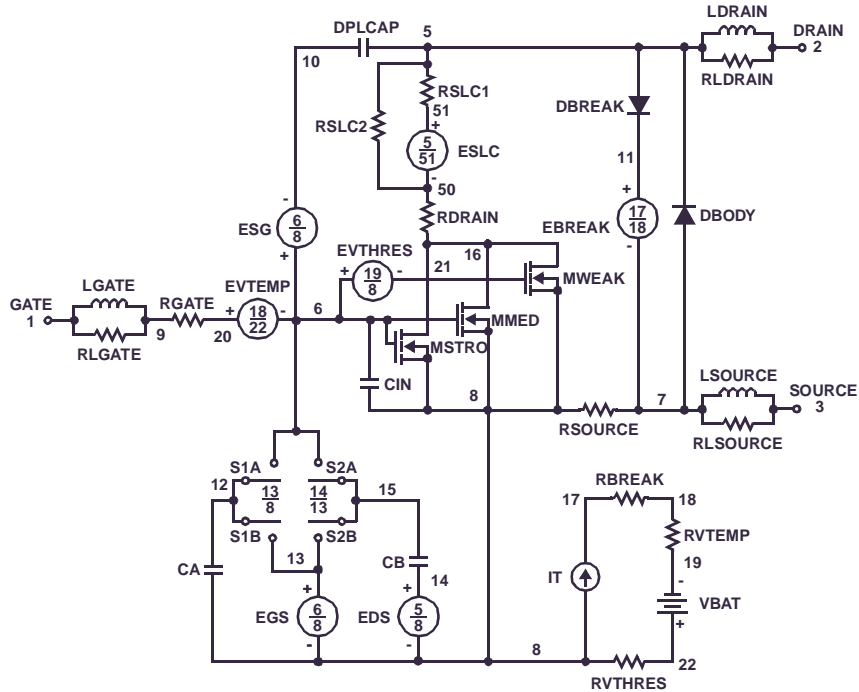
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-1.5 VOFF=-4)

.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=-0.5 VOFF=0.5)

.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VON=0.5 VOFF=-0.5)

.ENDS

Note: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. FrankWheatley.



SABER Electrical Model

REV January 2003

template FDH038AN08A1 n2,n1,n3

electrical n2,n1,n3

{

var i iscl

dp..model dbodymod = (isl=2.4e-11,nl=1.02,rs=1.65e-3,trs1=3.2e-3,trs2=2.0e-7,cjo=6.0e-9,m=5.6e-1,tt=2.38e-8,xti=3.9)

dp..model dbreakmod = (rs=1.5e-1,trs1=1.0e-3,trs2=-8.9e-6)

dp..model dplcapmod = (cjo=1.5e-9,isl=10e-30,nl=10,m=0.47)

m..model mmedmod = (type=_n,vto=3.2,kp=1.5,isl=1e-30,tox=1)

m..model mstrongmod = (type=_n,vto=3.95,kp=235,isl=1.0e-30,tox=1)

m..model mweakmod = (type=_n,vto=2.73,kp=0.02,isl=1.0e-30,tox=1,rs=0.1)

sw_vcsp..model s1amod = (ron=1e-5,roff=0.1,von=-4,voff=-1.5)

sw_vcsp..model s1bmod = (ron=1e-5,roff=0.1,von=-1.5,voff=-4)

sw_vcsp..model s2amod = (ron=1e-5,roff=0.1,von=-0.5,voff=0.5)

sw_vcsp..model s2bmod = (ron=1e-5,roff=0.1,von=0.5,voff=-0.5)

c.ca n12 n8 = 1.0e-9

c.cb n15 n14 = 3.1e-9

c.cin n6 n8 = 8.22e-9

dp.dbody n7 n5 = model=dbodymod

dp.dbreak n5 n11 = model=dbreakmod

dp.dplcap n10 n5 = model=dplcapmod

spe.ebreak n11 n7 n17 n18 = 84.9

spe.eds n14 n8 n5 n8 = 1

spe.egs n13 n8 n6 n8 = 1

spe.esg n6 n10 n6 n8 = 1

spe.evthres n6 n21 n19 n8 = 1

spe.evtemp n20 n6 n18 n22 = 1

i.it n8 n17 = 1

l.lgate n1 n9 = 4.81e-9

l.ldrain n2 n5 = 1.0e-9

l.lsource n3 n7 = 4.63e-9

res.rlgate n1 n9 = 48.1

res.rldrain n2 n5 = 10

res.rlsource n3 n7 = 46.3

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u

m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18 = 1, tc1=1.05e-3,tc2=-9.0e-7

res.rdrain n50 n16 = 2.0e-4, tc1=1.8e-2,tc2=2.2e-4

res.rgate n9 n20 = 20

res.rslc1 n5 n51 = 1e-6, tc1=2.0e-3,tc2=1.0e-5

res.rslc2 n5 n50 = 1.0e3

res.rsource n8 n7 = 2.6e-3, tc1=5.0e-3,tc2=1.0e-6

res.rvthres n22 n8 = 1, tc1=-4.2e-3,tc2=-1.8e-5

res.rvtemp n18 n19 = 1, tc1=-4.5e-3,tc2=2.0e-6

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod

sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod

sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod

sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

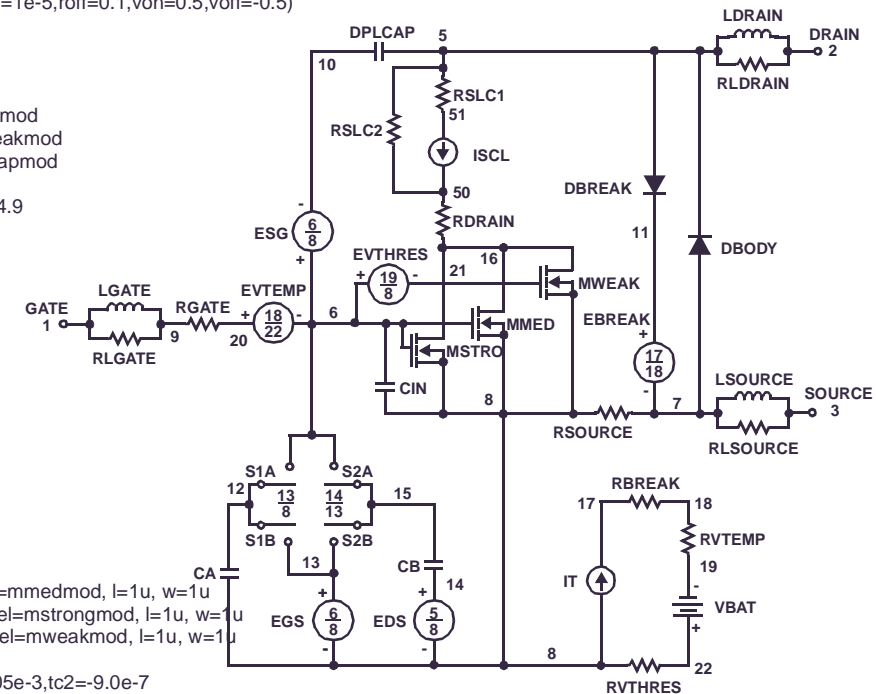
equations {

i (n51->n50) +=iscl

iscl: v(n51,n50) = ((v(n5,n51))/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/300))** 10)

}

}



SPICE Thermal Model

REV 23 January 2003

FDH038AN08A1T

CTHERM1 TH 6 5.5e-3
 CTHERM2 6 5 6.0e-3
 CTHERM3 5 4 7.4e-3
 CTHERM4 4 3 7.65e-3
 CTHERM5 3 2 5.85e-2
 CTHERM6 2 TL 6.0e-1

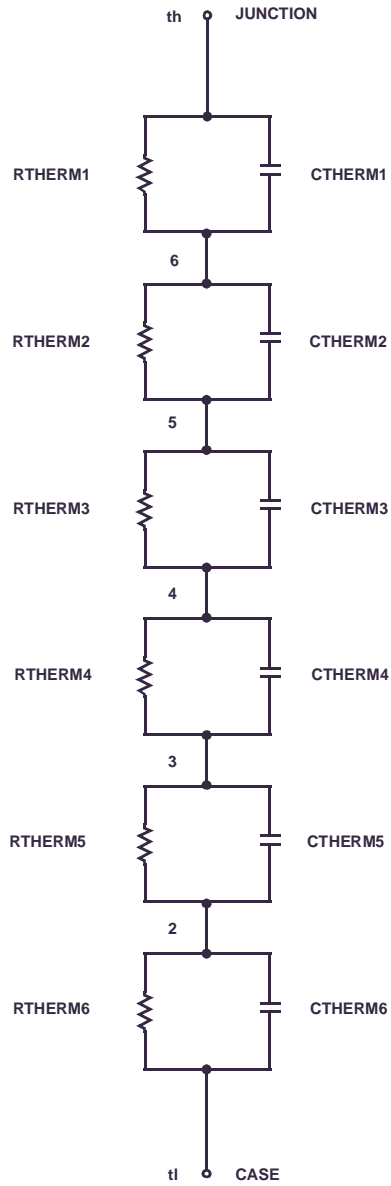
RTHERM1 TH 6 9.0e-3
 RTHERM2 6 5 2.08e-2
 RTHERM3 5 4 2.28e-2
 RTHERM4 4 3 7.0e-2
 RTHERM5 3 2 7.5e-2
 RTHERM6 2 TL 8.5e-2

SABER Thermal Model

SABER thermal model FDH038AN08A1T
 template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.ctherm1 th 6 =5.5e-3
    ctherm.ctherm2 6 5 =6.0e-3
    ctherm.ctherm3 5 4 =7.4e-3
    ctherm.ctherm4 4 3 =7.65e-3
    ctherm.ctherm5 3 2 =5.85e-2
    ctherm.ctherm6 2 tl =6.0e-1
```

```
rtherm.rtherm1 th 6 =9.0e-3
rtherm.rtherm2 6 5 =2.08e-2
rtherm.rtherm3 5 4 =2.28e-2
rtherm.rtherm4 4 3 =7.0e-2
rtherm.rtherm5 3 2 =7.5e-2
rtherm.rtherm6 2 tl =8.5e-2
}
```



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ActiveArray™	FACT Quiet Series™	ISOPLANAR™	POP™	Stealth™
Bottomless™	FAST®	LittleFET™	Power247™	SuperSOT™-3
CoolFET™	FASTr™	MicroFET™	PowerTrench®	SuperSOT™-6
CROSSVOLT™	FRFET™	MicroPak™	QFET™	SuperSOT™-8
DOME™	GlobalOptoisolator™	MICROWIRE™	QS™	SyncFET™
EcoSPARK™	GTO™	MSX™	QT Optoelectronics™	TinyLogic®
E ² CMOS™	HiSeC™	MSXPro™	Quiet Series™	TruTranslation™
EnSigna™	I ² C™	OCX™	RapidConfigure™	UHC™
Across the board. Around the world.™		OCXPro™	RapidConnect™	UltraFET®
The Power Franchise™		OPTOLOGIC®	SILENT SWITCHER®	VCX™
Programmable Active Droop™		OPTOPLANAR™	SMART START™	

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.