



## FDP55N06/FDPF55N06 60V N-Channel MOSFET

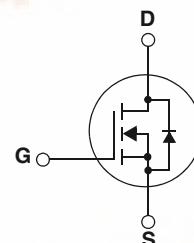
### Features

- 55A, 60V,  $R_{DS(on)} = 0.022 \Omega$  @  $V_{GS} = 10 V$
- Low gate charge ( typical 30 nC)
- Low Crss ( typical 60 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

**UniFET™**

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



### Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	FDP55N06	FDPF55N06	Units
$V_{DSS}$	Drain-Source Voltage	60		V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ C$ )	55	55 *	A
	- Continuous ( $T_C = 100^\circ C$ )	34.8	34.8 *	A
$I_{DM}$	Drain Current - Pulsed	(Note 1)	220	A
$V_{GSS}$	Gate-Source Voltage		$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	480	mJ
$I_{AR}$	Avalanche Current	(Note 1)	55	A
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	11.4	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ C$ )	114	48	W
	- Derate above $25^\circ C$	0.9	0.4	W/ $^\circ C$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ C$
$T_L$	Maximum lead temperature for soldering purposes, 1/8 $\nabla$ from case for 5 seconds		300	$^\circ C$

\* Drain current limited by maximum junction temperature

### Thermal Characteristics

Symbol	Parameter	FDP55N06	FDPF55N06	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.1	2.58	$^\circ C/W$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ C/W$



## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP55N06	FDP55N06	TO-220			50
FDPF55N06	FDPF55N06	TO-220F			50

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

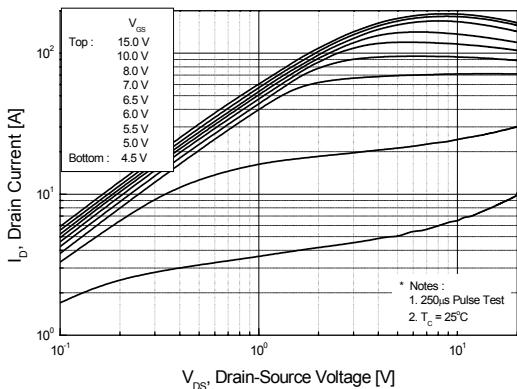
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	60	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.05	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 60 \text{ V}$ , $V_{GS} = 0 \text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 48 \text{ V}$ , $T_C = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20 \text{ V}$ , $V_{DS} = 0 \text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu\text{A}$	2.0	--	4.0	V
$R_{DS(\text{on})}$	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 27.5 \text{ A}$	--	0.018	0.022	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 25 \text{ V}$ , $I_D = 27.5 \text{ A}$ (Note 4)	--	33	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1.0 \text{ MHz}$	--	1160	1510	pF
$C_{oss}$	Output Capacitance		--	375	490	pF
$C_{rss}$	Reverse Transfer Capacitance		--	60	90	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}$ , $I_D = 55 \text{ A}$ , $R_G = 25 \Omega$	--	30	65	ns
$t_r$	Turn-On Rise Time		--	130	265	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	150	ns
$t_f$	Turn-Off Fall Time		--	95	195	ns
$Q_g$	Total Gate Charge	$V_{DS} = 48 \text{ V}$ , $I_D = 55 \text{ A}$ , $V_{GS} = 10 \text{ V}$	--	30	37	nC
$Q_{gs}$	Gate-Source Charge		--	6.5	--	nC
$Q_{gd}$	Gate-Drain Charge		--	7.5	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	55	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	220	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_S = 55 \text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$ , $I_S = 55 \text{ A}$ , $dI_F / dt = 100 \text{ A}/\mu\text{s}$	--	40	--	ns
$Q_{rr}$	Reverse Recovery Charge		(Note 4)	--	55	$\mu\text{C}$

### Notes:

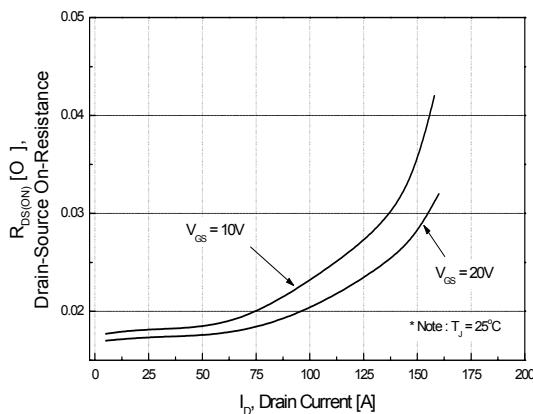
- Repetitive Rating : Pulse width limited by maximum junction temperature
- $L = 5.0\text{mH}$ ,  $I_{AS} = 55\text{A}$ ,  $V_{DD} = 50\text{V}$ ,  $R_G = 25 \Omega$ , Starting  $T_J = 25^\circ\text{C}$
- $I_{SD} \leq 55\text{A}$ ,  $di/dt \leq 200\text{A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
- Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
- Essentially independent of operating temperature

## Typical Performance Characteristics

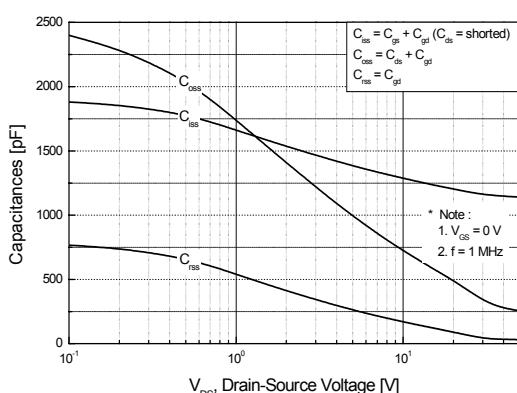
**Figure 1. On-Region Characteristics**



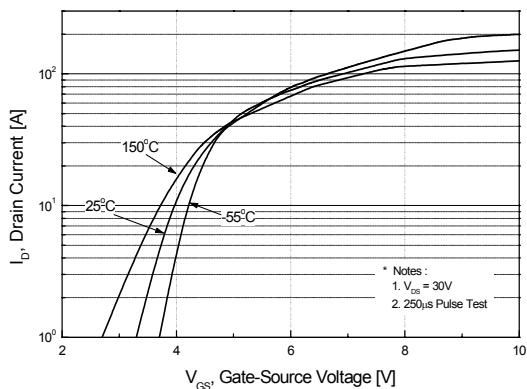
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



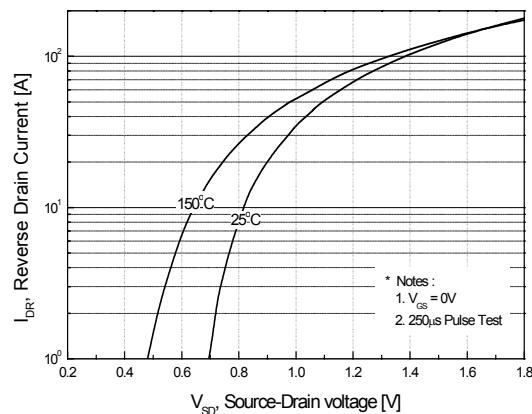
**Figure 5. Capacitance Characteristics**



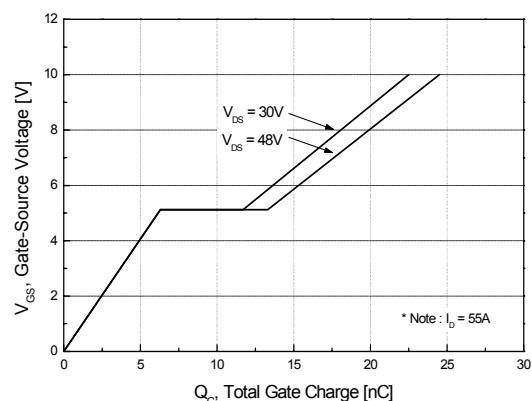
**Figure 2. Transfer Characteristics**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**

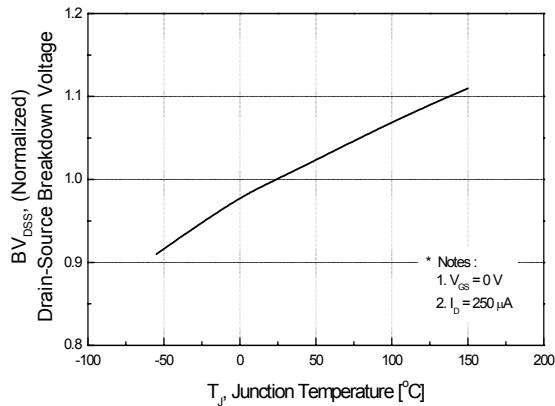


**Figure 6. Gate Charge Characteristics**

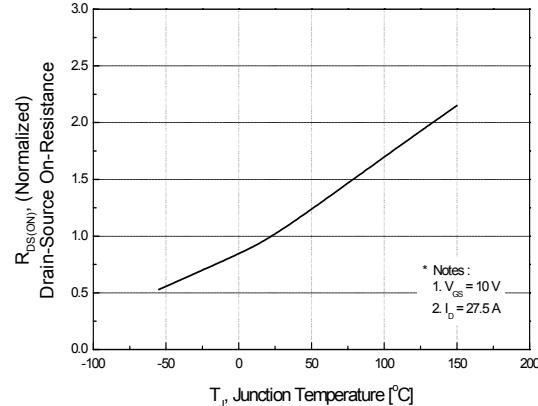


## Typical Performance Characteristics (Continued)

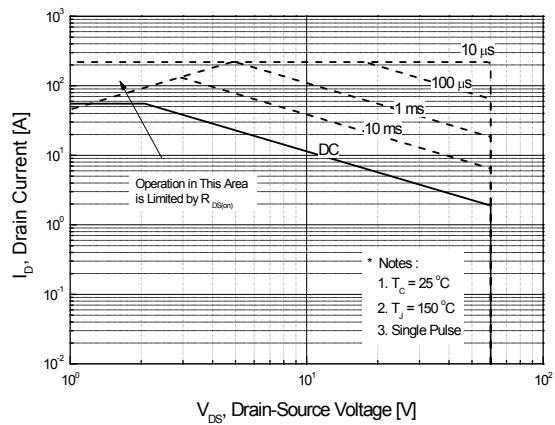
**Figure 7. Breakdown Voltage Variation vs. Temperature**



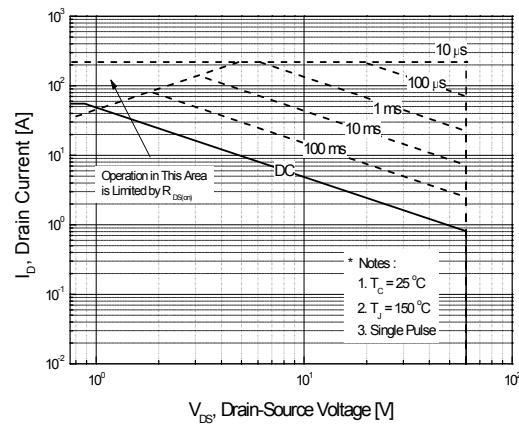
**Figure 8. On-Resistance Variation vs. Temperature**



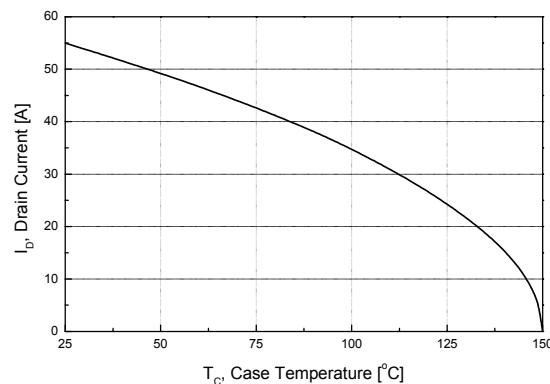
**Figure 9-1. Maximum Safe Operating Area for FDP55N06**



**Figure 9-2. Maximum Safe Operating Area for FDPF55N06**

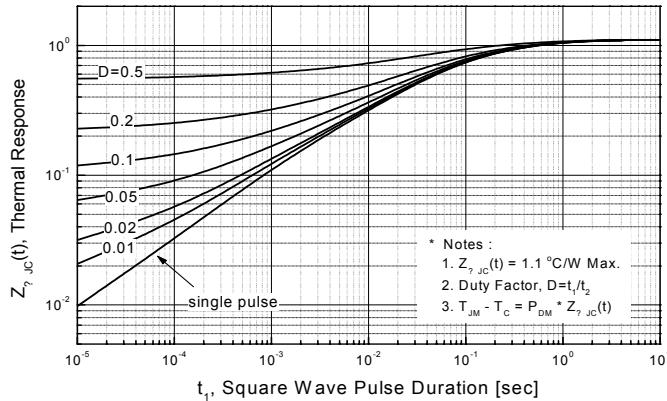


**Figure 10. Maximum Drain Current vs. Case Temperature**

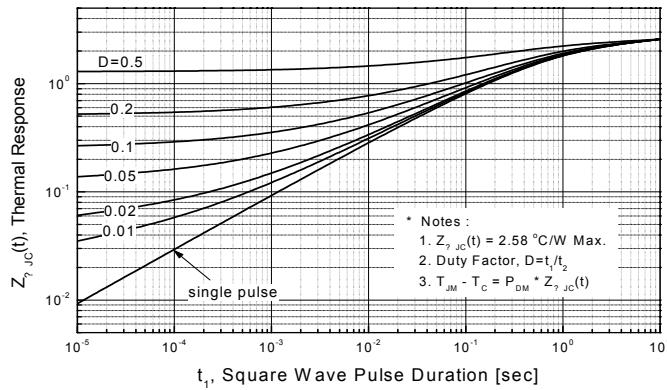


## Typical Performance Characteristics (Continued)

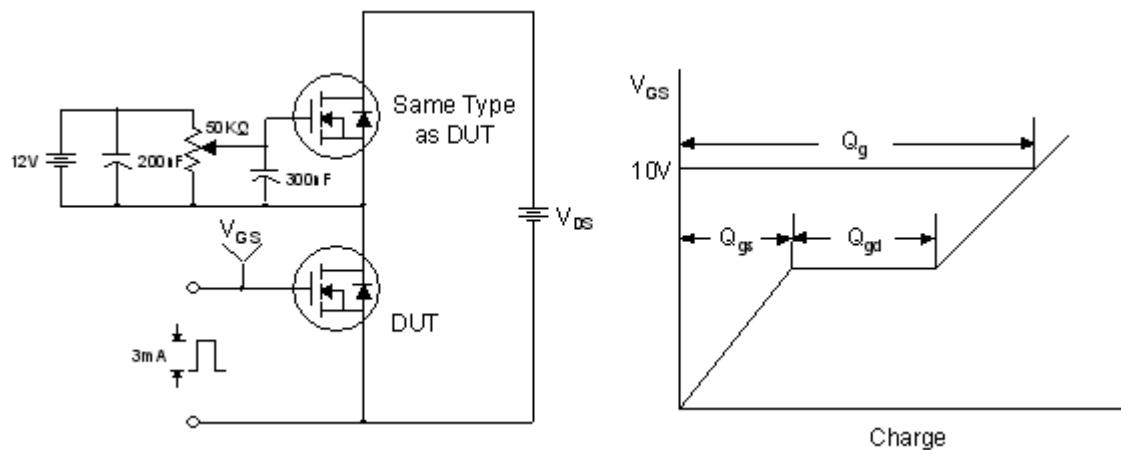
**Figure 11-1. Transient Thermal Response Curve for FDP55N06**



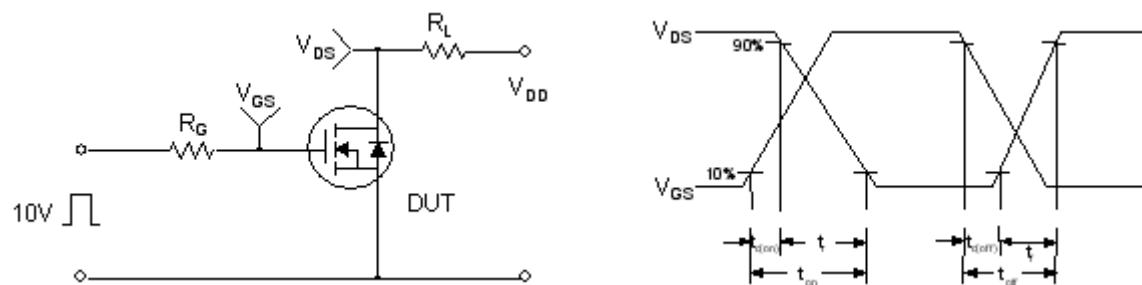
**Figure 11-2. Transient Thermal Response Curve for FDPF55N06**



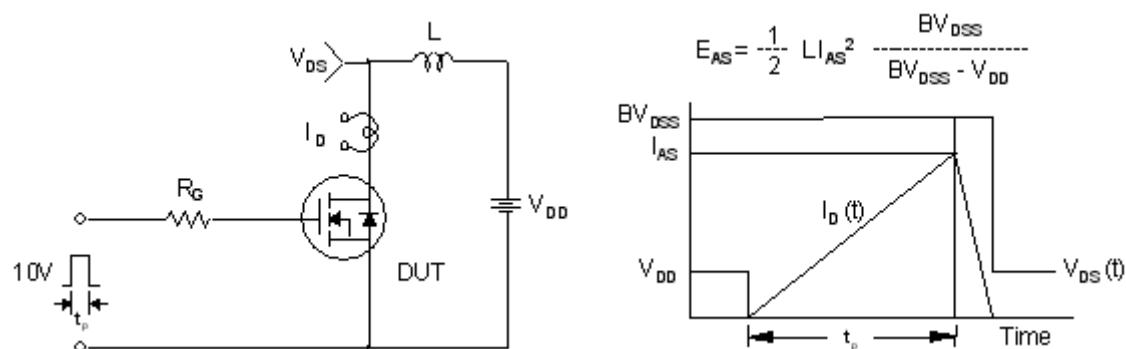
### Gate Charge Test Circuit & Waveform



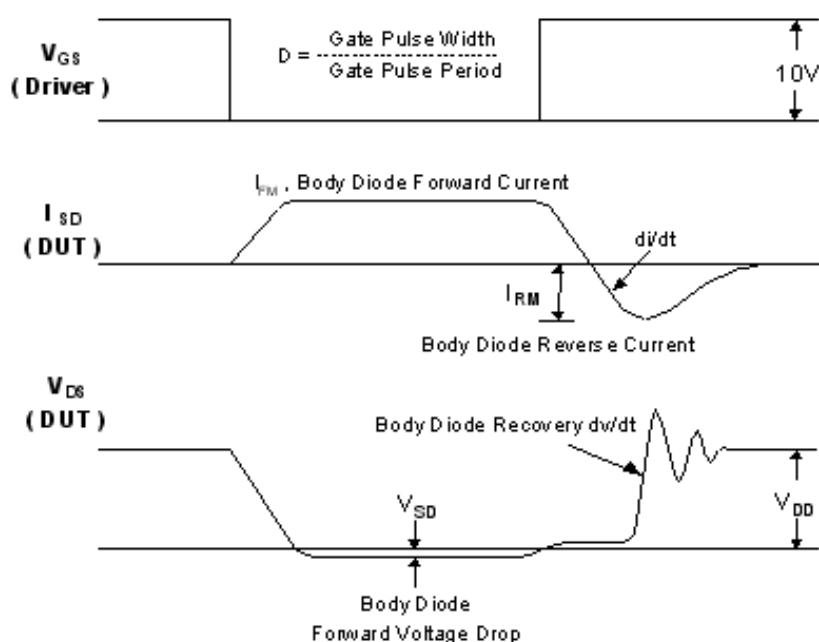
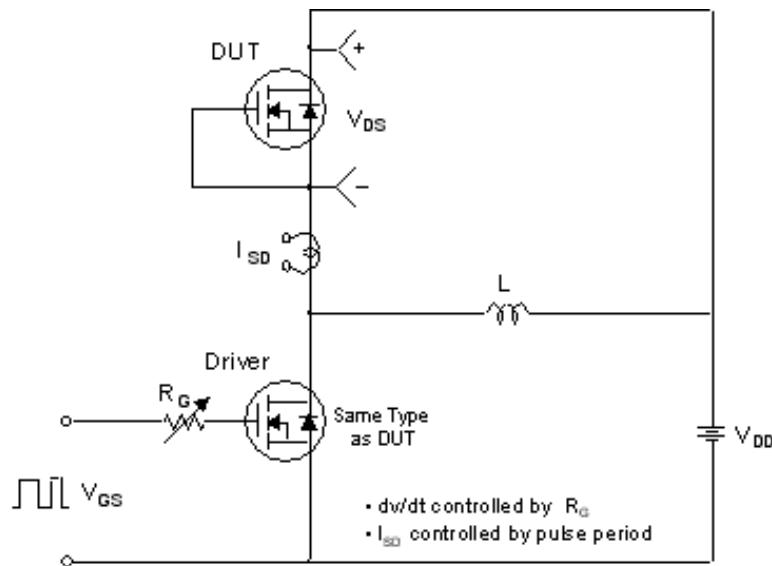
### Resistive Switching Test Circuit & Waveforms



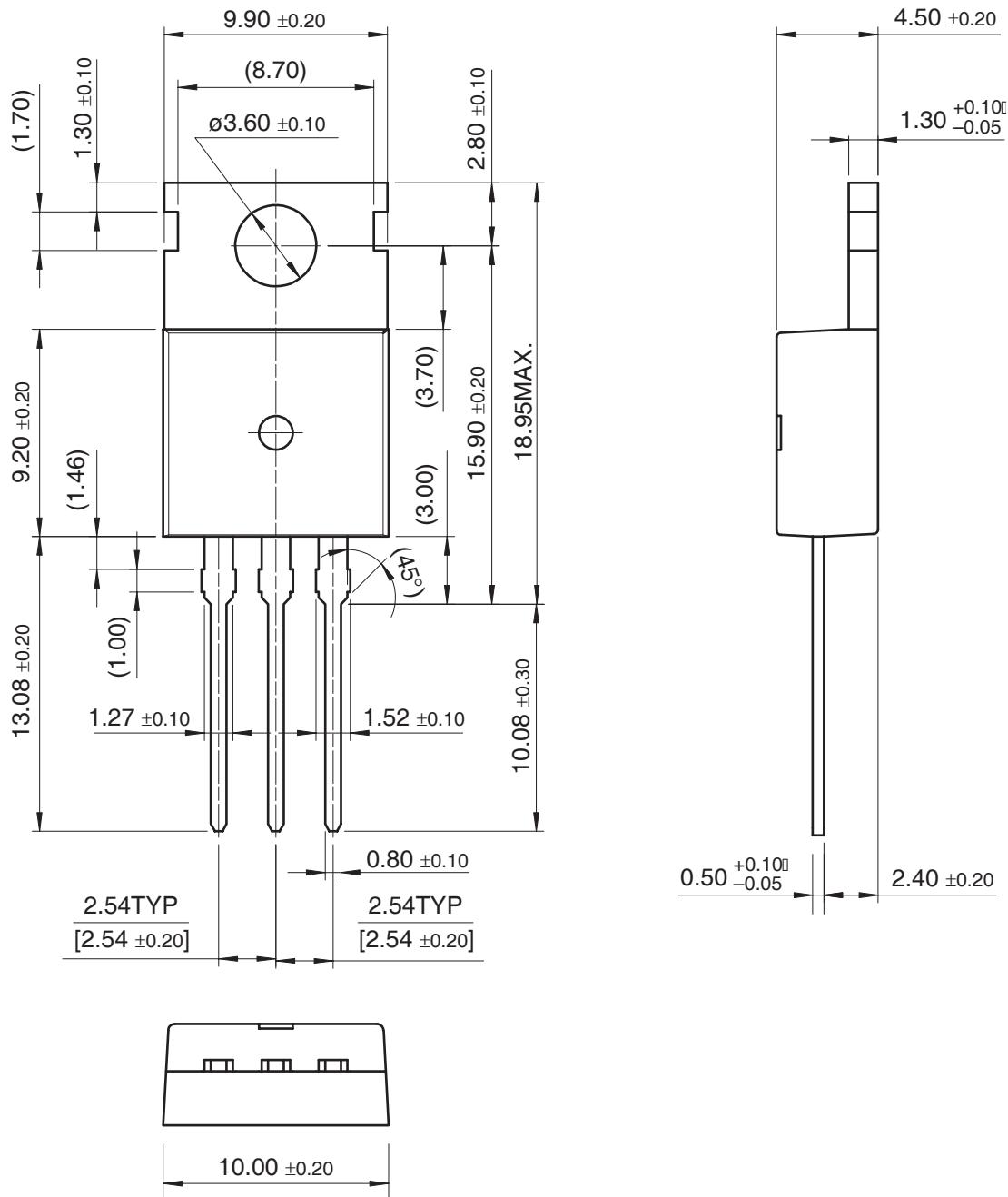
### Unclamped Inductive Switching Test Circuit & Waveforms



## Peak Diode Recovery dv/dt Test Circuit &amp; Waveforms

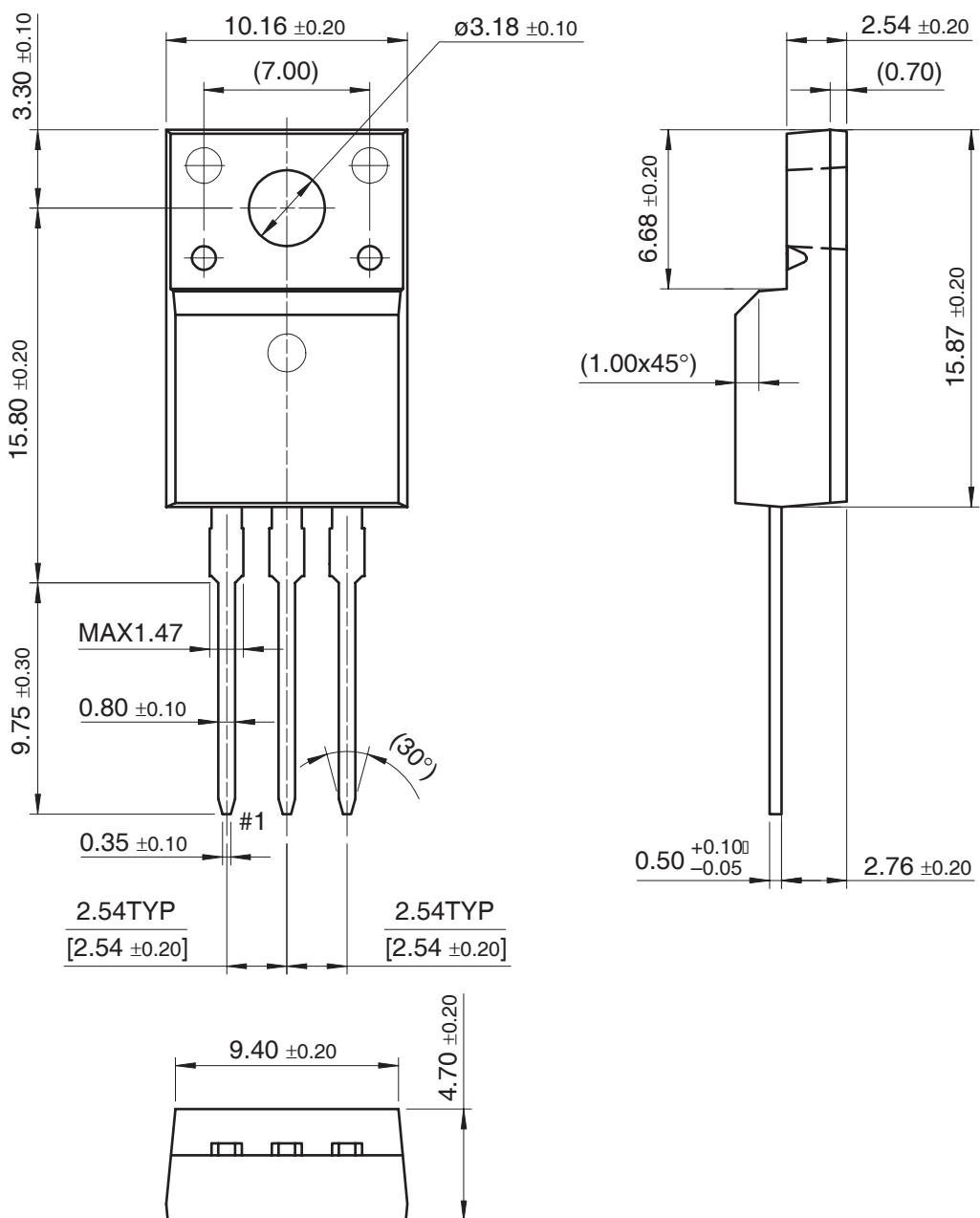


## TO-220



## Mechanical Dimensions

TO-220F



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E²CMOST™	j-Lo™	OCX™	µSerDes™	VCX™
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Programmable Active Droop™		Power247™	SupersOT™-3	
		PowerEdge™	SupersOT™-6	

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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