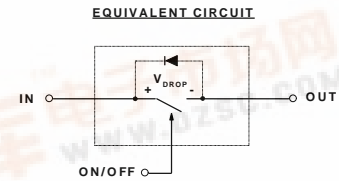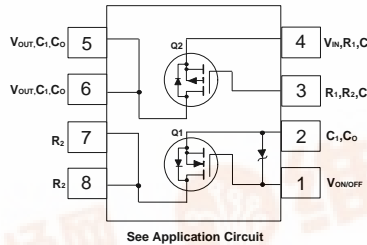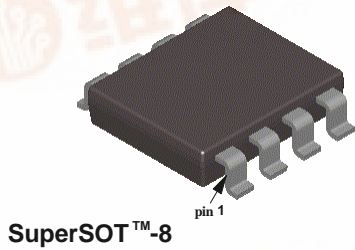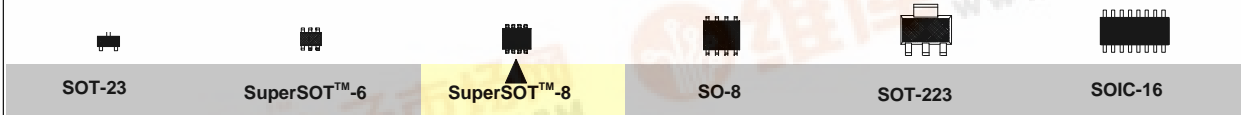**FAIRCHILD**
SEMICONDUCTOR ™

August 2000

FDR8321L
P-Channel MOSFET With Gate Driver For Load Switch Application

General Description

This device is designed for configuration as a load switch and is particularly suited for Power Management in portable battery powered electronic equipment. Designed to operate from 2.5V to 8V input and supply up to 2.9A. The device features a small N-Channel MOSFET (Q1) together with a large P-Channel power MOSFET (Q2) in a single SuperSOT™-8 package.

Features

- V_{DROP} = 0.2V @ V_{IN} = 5V, I_L = 2.9A. $R_{DS(ON)}$ = 0.070 Ω
  V_{DROP} = 0.2V @ V_{IN} = 2.5V, I_L = 2A. $R_{DS(ON)}$ = 0.105 Ω.

- $V_{ON/OFF}$ Zener protection for ESD ruggedness (>6KV Human Body Model).

- High density cell design for extremely low on-resistance.

| SOT-23 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16 |

SuperSOT™-8

pin 1

EQUIVALENT CIRCUIT

V_{OUT}, C_1, C_O	5	4	V_{IN}, R_1, C_i
V_{OUT}, C_1, C_O	6	3	R_1, R_2, C_1
R_2	7	2	C_1, C_O
R_2	8	1	$V_{ON/OFF}$

Q2   Q1

See Application Circuit

IN V_{DROP} OUT

ON/OFF

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		FDR8321L	Units
V_{IN}	Input Voltage Range		2.5 - 8	V
$V_{ON/OFF}$	On/Off Voltage Range		1.5 - 8	V
I_L	Load Current @ V_{DROP}= 0.2V - Continuous	(Note 1)	2.9	A
	- Pulsed		10	
P_D	Maximum Power Dissipation	(Note 2)	0.8	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 2)	156	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 2)	40	°C/W

## Electrical Characteristics   (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
I_{FL}	Forward Leakage Current	V_{IN} = 5 V, $V_{ON/OFF}$ = 0 V			1	µA
ON CHARACTERISTICS (Note 3)						
V_{DROP}	Conduction Voltage Drop	V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V, I_L = 2.9 A		0.185	0.2	V
		V_{IN} = 2.5 V, $V_{ON/OFF}$ = 3.3 V, I_L = 2 A		0.18	0.2	
$R_{DS(ON)}$	Q_2 - Static Drain-Source On-Resistance	V_{GS} = -5 V, I_D = -2.9 A		0.06	0.07	Ω
		V_{GS} = -2.5 V, I_D = -2 A		0.09	0.105	
I_L	Load Current	V_{DROP} = 0.2 V, V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V	2.9			A
		V_{DROP} = 0.2 V, V_{IN} = 2.5 V, $V_{ON/OFF}$ = 3.3 V	2			

Notes:

1. V_{IN}=5V, $V_{ON/OFF}$=8V, V_{DROP}=0.2V, T_A=25°C

2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ typical =156°C/W when mounted on a minimum 0.0025 in^2 pad on FR-4.

3. Pulse Test: Pulse Width $\leq$ 300µs, Duty Cycle $\leq$ 2.0%

FDR8321L Load Switch Application

APPLICATION CIRCUIT
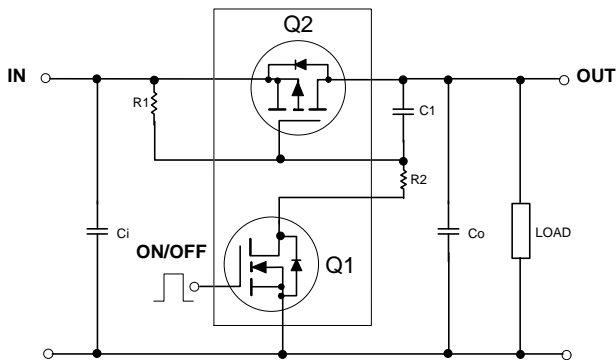
External Component Recommendation

First select R2, 100 - 1kΩ, for Slew Rate control.

C1 $\leq$ 1000pF can be added in addition to R2 for further In-rush current control.

Then select R1 such that R1/R2 ratio maintains between 10 - 100. R1 is required to turn Q2 off.

For SPICE simulation, users can download a "FDR8321L.MOD" Spice model from Fairchild Web Site at www.fairchildsemi.com

Typical Electrical Characteristics ($T_A = 25\ ^{\circ}C$ unless otherwise noted)
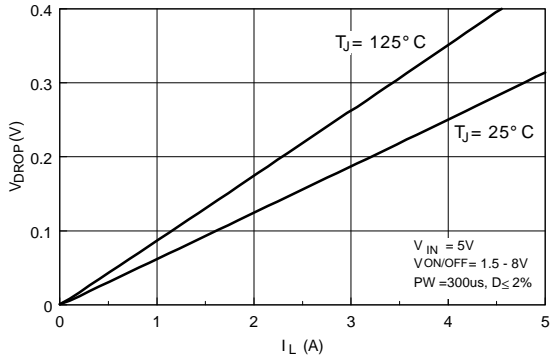
Figure 1. Conduction Voltage Drop versus
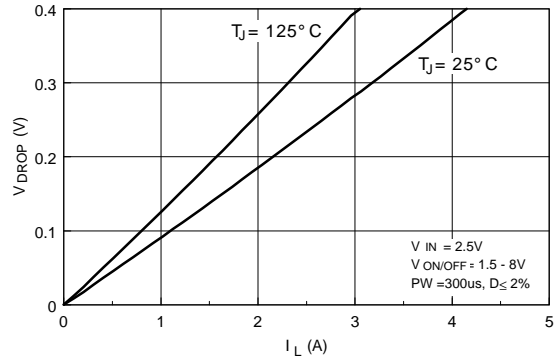Load Current at Input Voltage 5V.

Figure 2. Conduction Voltage Drop versus
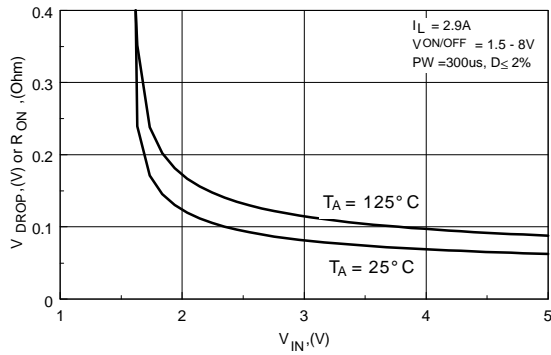Load Current at Input Voltage 2.5V.

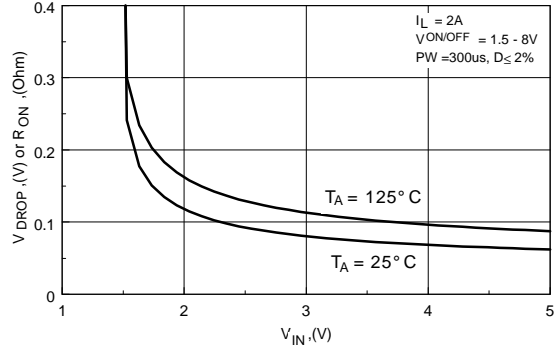**Figure 3.** Conduction Voltage Drop versus
input Voltage at Load Current 2.9A.

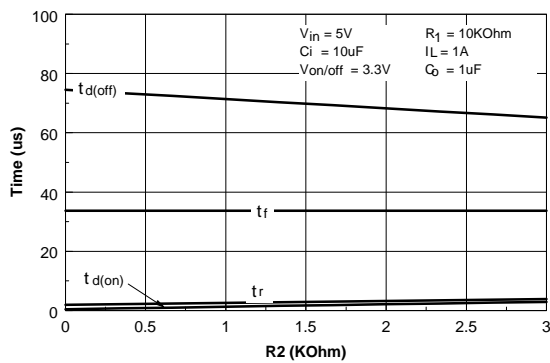**Figure 4.** Conduction Voltage Drop versus
Input Voltage at Load Current 2A.

Figure 5. Switching Variation with R_2
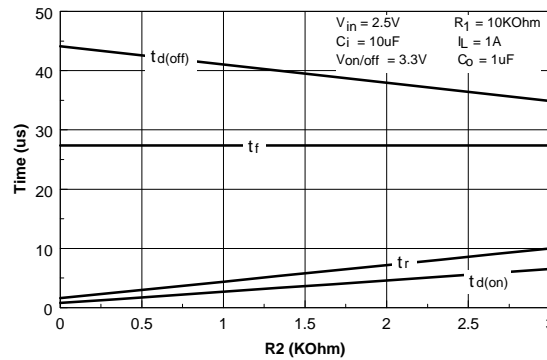at $V_{in} = 5V$ and $R_1 = 10K\Omega$.

Figure 6. Switching Variation with R_2
at $V_{in} = 2.5V$ and $R_1 = 10K\Omega$.

Typical Electrical Characteristics $(T_A = 25\ ^{\circ}C$ unless otherwise noted $)$

y-axis: r(t), NORMALIZED EFFECTIVE TRANSIENT THERMAL RESISTANCE

x-axis: t_1, TIME (sec)

D = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse

$R_{\theta JA}(t) = r(t)\ ^* R_{\theta JA}$

$R_{\theta JA} = 156\ ^{\circ}C/W$

P(pk)

t_1
t_2

$T_J - T_A = P\ ^* R_{\theta JA}(t)$
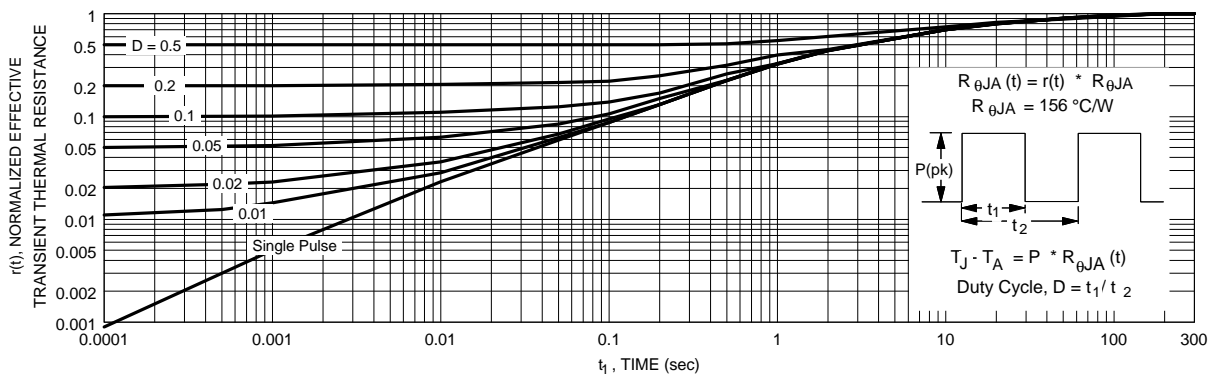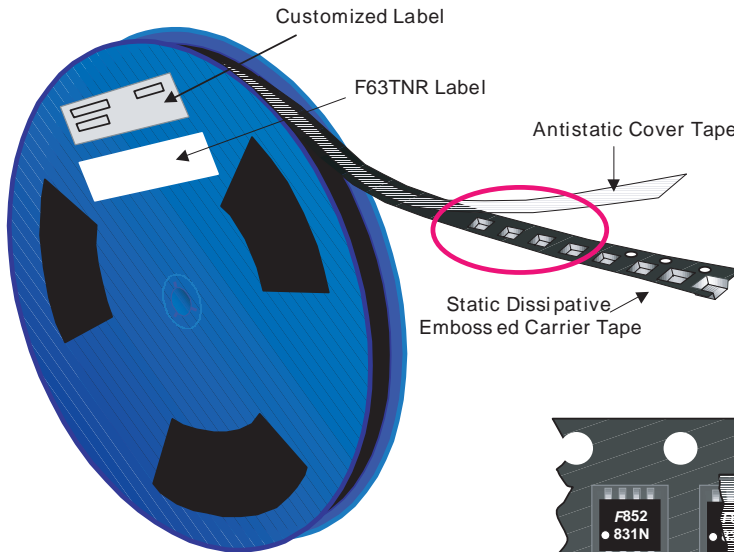
Duty Cycle, $D = t_1 / t_2$

Figure 7. Transient Thermal Response Curve.
Thermal characterization performed on the conditions described in Note 2.

# SuperSOT™-8 Tape and Reel Data and Package Dimensions

FAIRCHILD
SEMICONDUCTOR ™

SSOT-8 Packaging
Configuration: Figure 1.0

Customized Label

F63TNR Label

Antistatic Cover Tape

Static Dissipative Embossed Carrier Tape
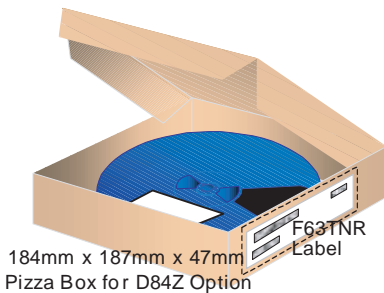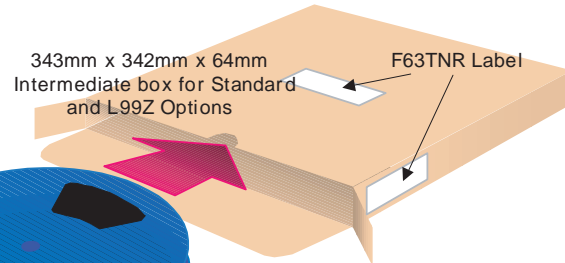
Packaging Description:

SSOT-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

*F*852
● 831N

Pin 1
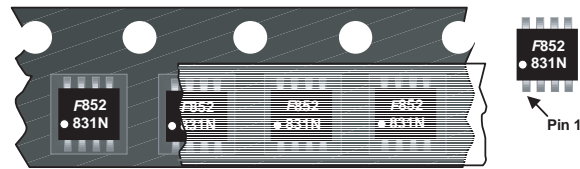
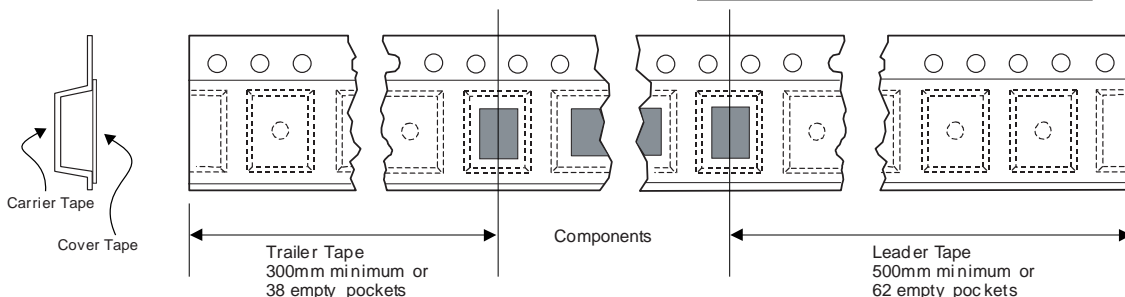### SSOT-8 Unit Orientation

SSOT-8 Packaging Information		
Packaging Option	Standard (no flow code)	D84Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	500
Reel Size	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	184x187x47
Max qty per Box	6,000	1,000
Weight per unit (gm)	0.0416	0.0416
Weight per Reel (kg)	0.5615	0.0980
Note/Comments		

343mm x 342mm x 64mm
Intermediate box for Standard and L99Z Options

F63TNR Label

F63TNR Label

184mm x 187mm x 47mm
Pizza Box for D84Z Option

F63TNR Label

F63TNR Label sample

LOT: CBVK741B019	QTY: 3000
FSID: FDR835N	SPEC:
D/C1: D9842 QTY1:	SPEC REV:
D/C2: QTY2:	CPN:
	N/F: F (F63TNR)3

SSOT-8 Tape Leader and Trailer
Configuration: Figure 2.0

Carrier Tape

Cover Tape

Components

Trailer Tape
300mm minimum or
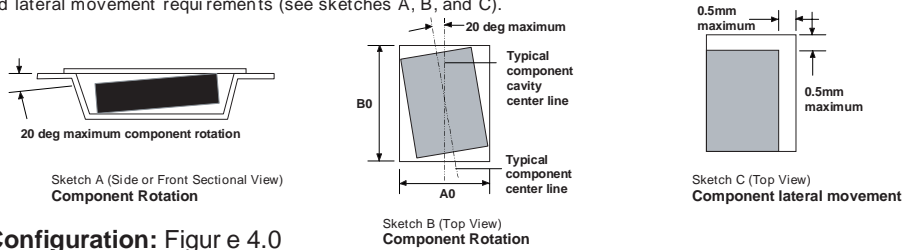38 empty pockets

Leader Tape
500mm minimum or
62 empty pockets

SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

SSOT-8 Embossed Carrier Tape
Configuration: Figure 3.0

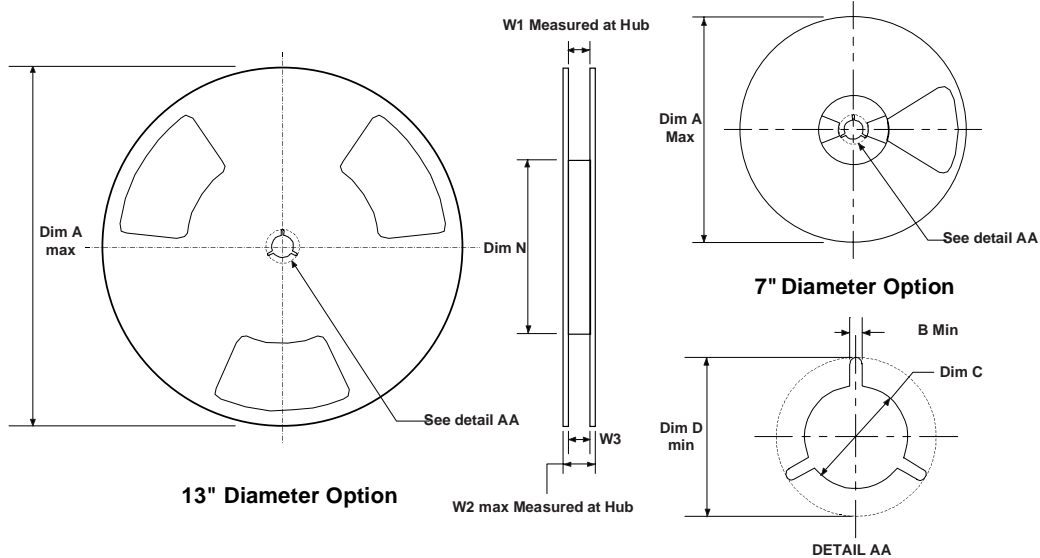**User Direction of Feed**
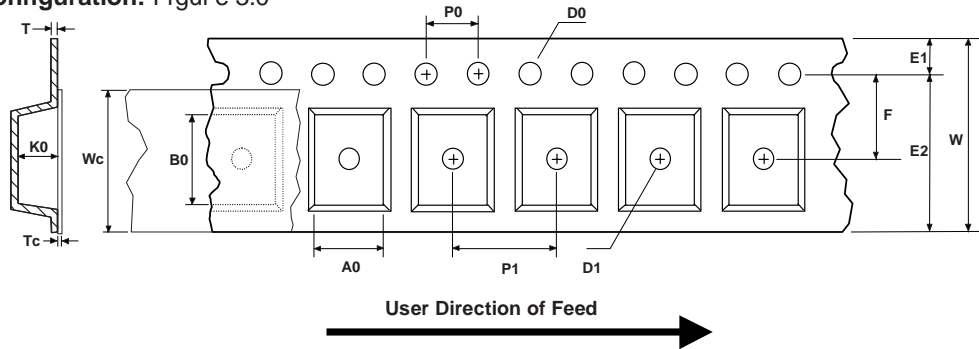
Dimensions are in millimeter													
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SSOT-8 (12mm)	4.47 +/-0.10	5.00 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.280 +/-0.150	9.5 +/-0.025	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).


Sketch A (Side or Front Sectional View)
Component Rotation

20 deg maximum component rotation

Sketch B (Top View)
Component Rotation

20 deg maximum

Typical component cavity center line

Typical component center line

Sketch C (Top View)
Component lateral movement

0.5mm maximum

0.5mm maximum

SSOT-8 Reel Configuration: Figure 4.0

13" Diameter Option

7" Diameter Option

W1 Measured at Hub

W2 max Measured at Hub

Dim N

W3

See detail AA

Dim A Max

See detail AA

B Min

Dim C

Dim D min

DETAIL AA

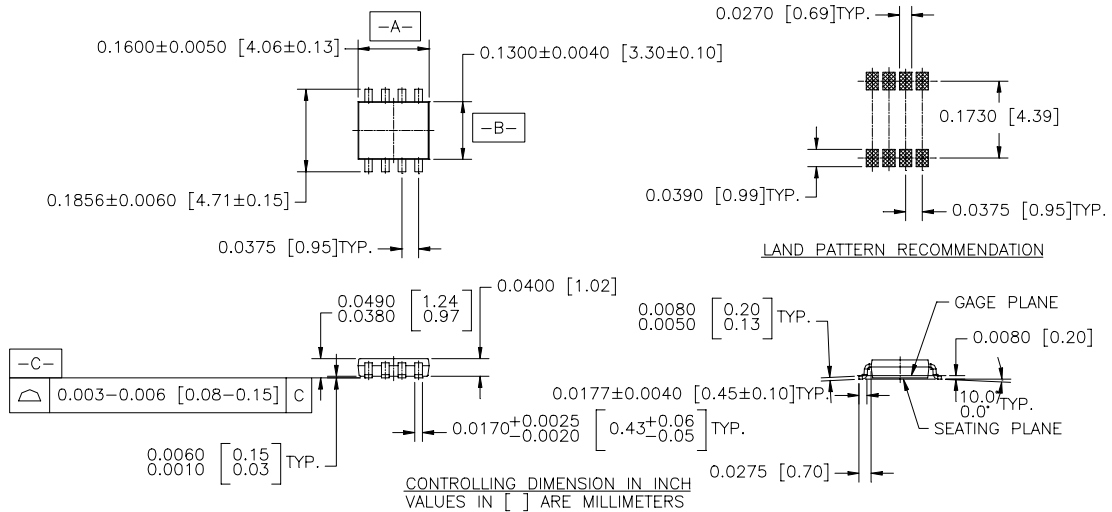| Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

SuperSOT™-8 (FS PKG Code 34, 35)

1 : 1
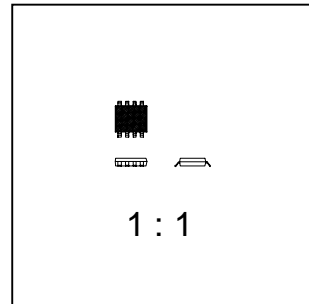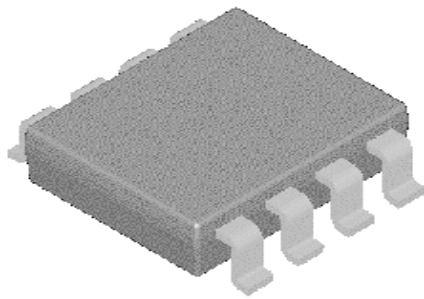
Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0416

0.1600±0.0050 [4.06±0.13]

−A−

0.1300±0.0040 [3.30±0.10]

−B−

0.1856±0.0060 [4.71±0.15]

0.0375 [0.95]TYP.

0.0270 [0.69]TYP.

0.1730 [4.39]

0.0390 [0.99]TYP.

0.0375 [0.95]TYP.

LAND PATTERN RECOMMENDATION

0.0490 [1.24]
0.0380 [0.97]

0.0400 [1.02]

−C−

△ 0.003−0.006 [0.08−0.15] C

0.0170 +0.0025 −0.0020 [0.43 +0.06 −0.05]TYP.

0.0060 [0.15]
0.0010 [0.03]TYP.

CONTROLLING DIMENSION IN INCH
VALUES IN [ ] ARE MILLIMETERS

0.0080 [0.20]
0.0050 [0.13]TYP.

0.0177±0.0040 [0.45±0.10]TYP.

GAGE PLANE

0.0080 [0.20]

10.0° TYP.
0.0°

SEATING PLANE

0.0275 [0.70]

SUPER SOT, 8 LEADS

NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH TI BE 200 MICROINCHES / 5.08 MICROMETERS
   MINIMUM TIN/LEAD (SOLDER) ON COPPER.

2. NO JEDEC REGISTRATION AS JAN. 1996

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CROSSVOLT™	HiSeC™	Quiet Series™	
DOME™	ISOPLANAR™	SuperSOT™-3	
E²CMOS™	MICROWIRE™	SuperSOT™-6	
EnSigna™	OPTOLOGIC™	SuperSOT™-8	
FACT™	OPTOPLANAR™	SyncFET™	
FACT Quiet Series™	POP™	TinyLogic™	
FAST®	PowerTrench®	UHC™	

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Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. F1