



May 2003

FDS3170N7

100V N-Channel PowerTrench[®] MOSFET

General Description

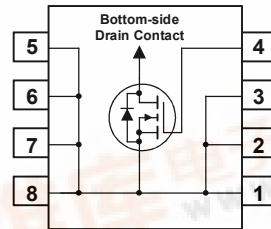
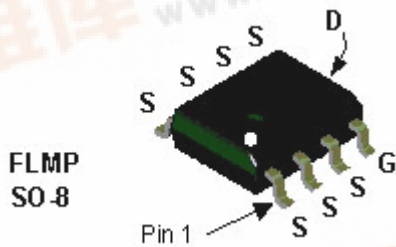
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for "low side" synchronous rectifier operation, providing an extremely low $R_{DS(ON)}$ in a small package.

Applications

- Synchronous rectifier
- DC/DC converter

Features

- 6.7 A, 100 V. $R_{DS(ON)} = 26 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 28 \text{ m}\Omega @ V_{GS} = 6.0 \text{ V}$
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability
- Fast switching, low gate charge
- FLMP SO-8 package: Enhanced thermal performance in industry-standard package size



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	100	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1a)	6.7	A
	– Pulsed	60	
P_D	Power Dissipation for Single Operation (Note 1a)	3.0	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	40	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	0.5	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS3170N7	FDS3170N7	13"	12mm	2500 units



Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche Ratings (Note 2)

W_{DSS}	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 50\text{ V}$, $I_D = 6.7\text{ A}$			360	mJ
I_{AR}	Drain-Source Avalanche Current				6.7	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		104		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2	2.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-6.9		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 6.7\text{ A}$ $V_{GS} = 6.0\text{ V}$, $I_D = 6.4\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 6.7\text{ A}$, $T_J = 125^\circ\text{C}$		21 22 40	26 28 52	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 6.7\text{ A}$		37		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		2714		pF
C_{oss}	Output Capacitance			171		pF
C_{rss}	Reverse Transfer Capacitance			82		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}$, $f = 1.0\text{ MHz}$		1.1		Ω

Switching Characteristics (Note 2)

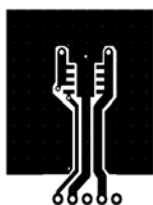
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$		14	26	ns
t_r	Turn-On Rise Time			10	18	ns
$t_{d(off)}$	Turn-Off Delay Time			49	80	ns
t_f	Turn-Off Fall Time			24	40	ns
Q_g	Total Gate Charge	$V_{DS} = 50\text{ V}$, $I_D = 6.7\text{ A}$, $V_{GS} = 10\text{ V}$		55	77	nC
Q_{gs}	Gate-Source Charge			12		nC
Q_{gd}	Gate-Drain Charge			14		nC

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current			2.5		A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.5\text{ A}$ (Note 2)		0.7	1.2	V
t_{RR}	Reverse Recovery Time	$I_F = 6.7\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 2)		47		ns
Q_{RR}	Reverse Recovery Charge			135		nC

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%, For Repetitive Avalanche T_J must be less than 150°C



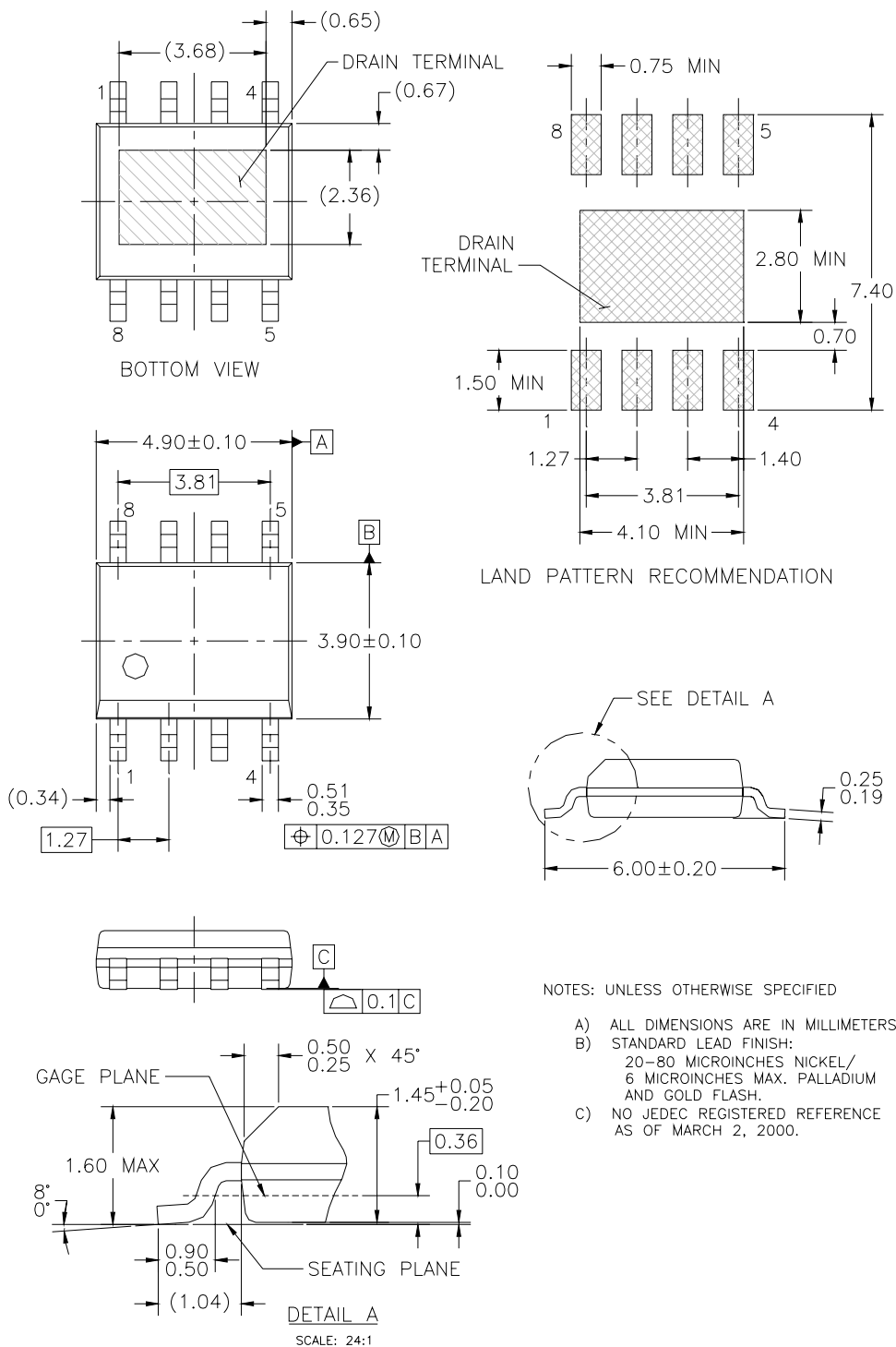
a) $40^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b) $85^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) STANDARD LEAD FINISH:
20-80 MICRONS NICKEL/
6 MICRONS MAX. PALLADIUM
AND GOLD FLASH.
- C) NO JEDEC REGISTERED REFERENCE
AS OF MARCH 2, 2000.

Typical Characteristics

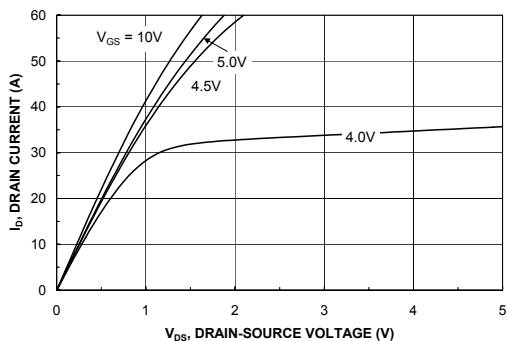


Figure 1. On-Region Characteristics.

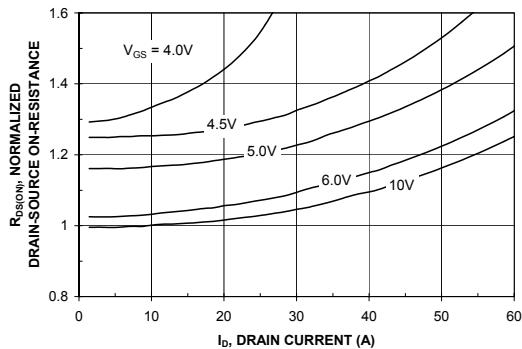


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

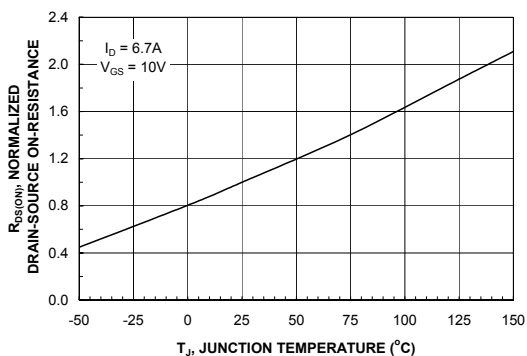


Figure 3. On-Resistance Variation with Temperature.

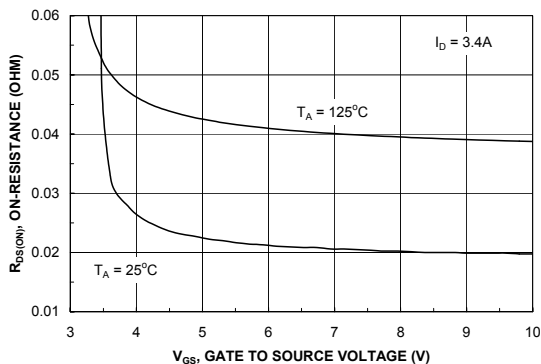


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

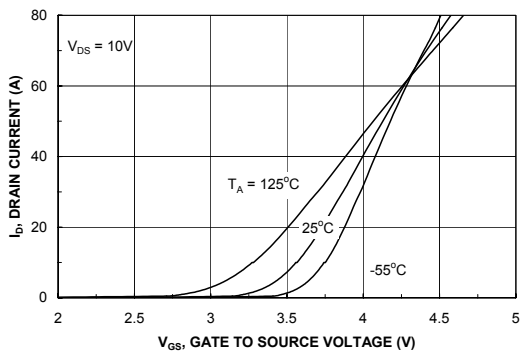


Figure 5. Transfer Characteristics.

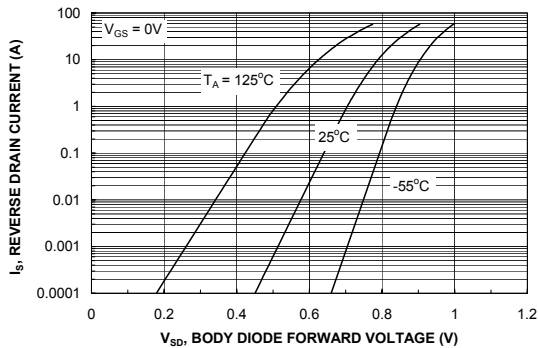


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

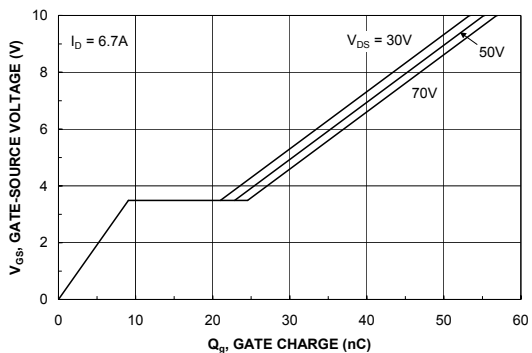


Figure 7. Gate Charge Characteristics.

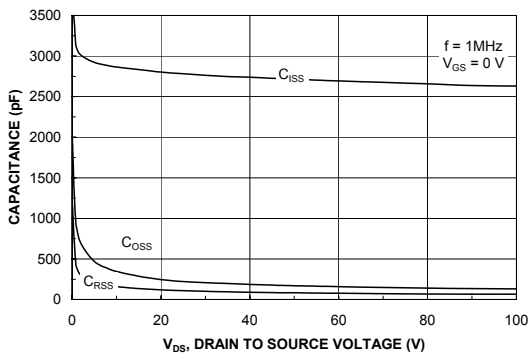


Figure 8. Capacitance Characteristics.

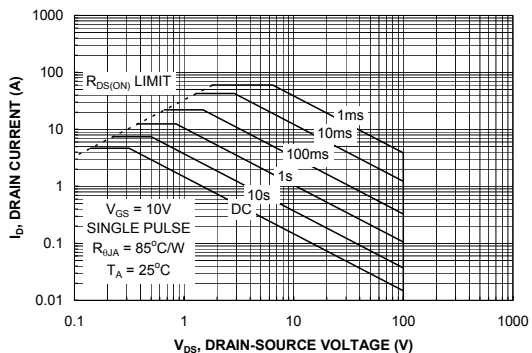


Figure 9. Maximum Safe Operating Area.

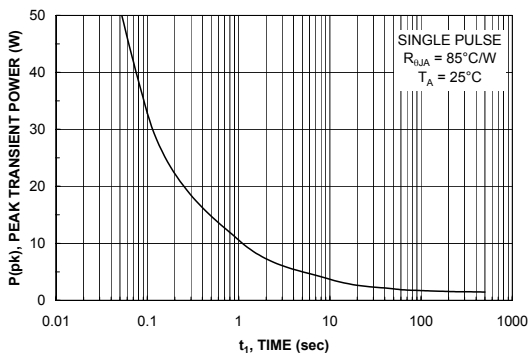


Figure 10. Single Pulse Maximum Power Dissipation.

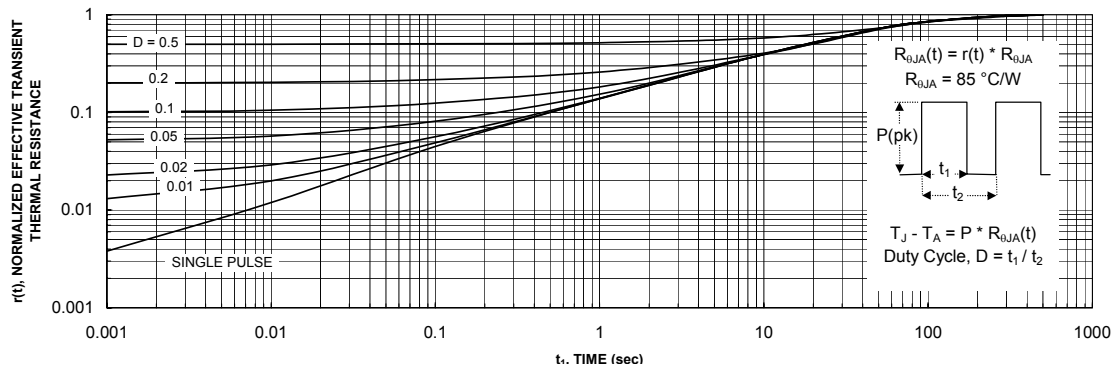


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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