**FAIRCHILD**
SEMICONDUCTOR®

May 2005

FDS6900AS

Dual N-Ch PowerTrench® SyncFET™

General Description

The FDS6900AS is designed to replace two single SO-8 MOSFETs and Schottky diode in synchronous DC:DC power supplies that provide various peripheral voltages for notebook computers and other battery powered electronic devices. FDS6900AS contains two unique 30V, N-channel, logic level, PowerTrench MOSFETs designed to maximize power conversion efficiency.

The high-side switch (Q1) is designed with specific emphasis on reducing switching losses while the low-side switch (Q2) is optimized to reduce conduction losses. Q2 also includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology.

Features

- **Q2**: Optimized to minimize conduction losses
  Includes SyncFET Schottky body diode

  8.2A, 30V $R_{DS(on)} = 22m\Omega$ @ $V_{GS} = 10V$

            $R_{DS(on)} = 28m\Omega$ @ $V_{GS} = 4.5V$

- **Q1**: Optimized for low switching losses
  Low Gate Charge (11nC typical)

  6.9A, 30V $R_{DS(on)} = 27m\Omega$ @ $V_{GS} = 10V$

            $R_{DS(on)} = 34m\Omega$ @ $V_{GS} = 4.5V$

- 100% R_G (Gate Resistance) Tested

SO-8

Pin 1

Dual N-Channel SyncFet
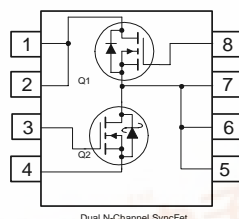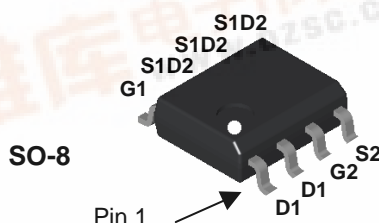
Absolute Maximum Ratings $T_A = 25°C$ unless otherwise noted

Symbol	Parameter		Q2	Q1	Units
V_{DSS}	Drain-Source Voltage		30	30	V
V_{GSS}	Gate-Source Voltage		±20	±20	V
I_D	Drain Current - Continuous	(Note 1a)	8.2	6.9	A
	- Pulsed		30	20	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6900AS	FDS6900AS	13"	12mm	2500 units
FDS6900AS	FDS6900AS_NL (Note 4)	13"	12mm	2500 units

FDS6900AS Rev B(X)

Electrical Characteristics

$T_A = 25°C$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 1$ mA $V_{GS} = 0$ V, $I_D = 250$ uA	Q2 Q1	30 30			V
$\dfrac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10$ mA, Referenced to 25°C $I_D = 250$ μA, Referenced to 25°C	Q2 Q1		27 22		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24$ V, $V_{GS} = 0$ V	Q2 Q1			500 1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = \pm20$ V, $V_{DS} = 0$ V	Q2 Q1			±100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 1$ mA $V_{DS} = V_{GS}$, $I_D = 250$ μA	Q2 Q1	1 1	1.9 1.9	3 3	V
$\dfrac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 10$ mA, Referenced to 25°C $I_D = 250$ uA, Referenced to 25°C	Q2 Q1		−3.2 −4.2		mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 8.2$ A $V_{GS} = 10$ V, $I_D = 8.2$ A, $T_J = 125°C$ $V_{GS} = 4.5$ V, $I_D = 7.6$ A	Q2		17 23 21	22 36 28	mΩ
		$V_{GS} = 10$ V, $I_D = 6.9$ A $V_{GS} = 10$ V, $I_D = 6.9$ A, $T_J = 125°C$ $V_{GS} = 4.5$ V, $I_D = 6.2$ A	Q1		22 30 27	27 38 34	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10$ V, $V_{DS} = 5$ V	Q2 Q1	30 20			A
g_{FS}	Forward Transconductance	$V_{DS} = 5$ V, $I_D = 8.2$ A $V_{DS} = 5$ V, $I_D = 6.9$ A	Q2 Q1		25 21		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	$V_{DS} = 15$ V, $V_{GS} = 0$ V, f = 1.0 MHz	Q2 Q1		570 600		pF
C_{oss}	Output Capacitance		Q2 Q1		180 150		pF
C_{rss}	Reverse Transfer Capacitance		Q2 Q1		70 70		pF
R_G	Gate Resistance		Q2 Q1		2.8 2.2	4.9 3.8	Ω
Switching Characteristics (Note 2)							
$t_{d(on)}$	Turn-On Delay Time		Q2 Q1		10 9	19 18	ns
t_r	Turn-On Rise Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 10$V, $R_{GEN} = 6$ Ω	Q2 Q1		5 4	10 8	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		26 23	42 32	ns
t_f	Turn-Off Fall Time		Q2 Q1		3 3	6 6	ns
$t_{d(on)}$	Turn-On Delay Time		Q2 Q1		11 10	20 19	ns
t_r	Turn-On Rise Time	$V_{DD} = 15$ V, $I_D = 1$ A, $V_{GS} = 4.5$ V, $R_{GEN} = 6$ Ω	Q2 Q1		15 9	27 18	ns
$t_{d(off)}$	Turn-Off Delay Time		Q2 Q1		16 14	29 25	ns
t_f	Turn-Off Fall Time		Q2 Q1		6 4	12 8	ns

Electrical Characteristics (continued) T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units

Switching Characteristics   (Note 2)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
$Q_{g(TOT)}$	Total Gate Charge at Vgs=10V	Q2: V_{DS} = 15 V, I_D = 8.2A	Q2 Q1		10 11	15 15	nC
Q_g	Total Gate Charge at Vgs=5V	Q1: V_{DS} = 15 V, I_D = 6.9A	Q2 Q1		5.8 6.1	8.2 8.5	nC
Q_{gs}	Gate–Source Charge		Q2 Q1		1.6 1.7		nC
Q_{gd}	Gate–Drain Charge		Q2 Q1		2.1 2.2		nC

Drain–Source Diode Characteristics and Maximum Ratings

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q2 Q1			2.3 1.3	A
T_{rr}	Reverse Recovery Time	I_F = 8.2 A,	Q2		15		ns
Q_{rr}	Reverse Recovery Charge	d_{iF}/d_t = 300 A/µs (Note 3)			6		nC
T_{rr}	Reverse Recovery Time	I_F = 6.9 A,	Q1		19		ns
Q_{rr}	Reverse Recovery Charge	d_{iF}/d_t = 100 A/µs (Note 3)			10		nC
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.3 A (Note 2) V_{GS} = 0 V, I_S = 5 A (Note 2) V_{GS} = 0 V, I_S = 1.3 A (Note 2)	Q2 Q2 Q1		0.6 0.7 0.7	0.7 1.0 1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
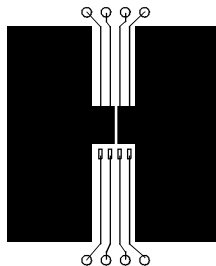
a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper
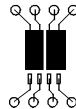
b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper
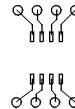
c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. See "SyncFET Schottky body diode characteristics" below.

4. FDS6900AS_NL is a lead free product. The FDS6900AS_NL marking will appear on the reel label.
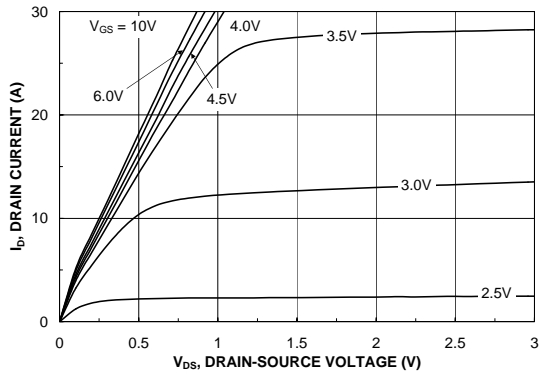
Typical Characteristics: Q2
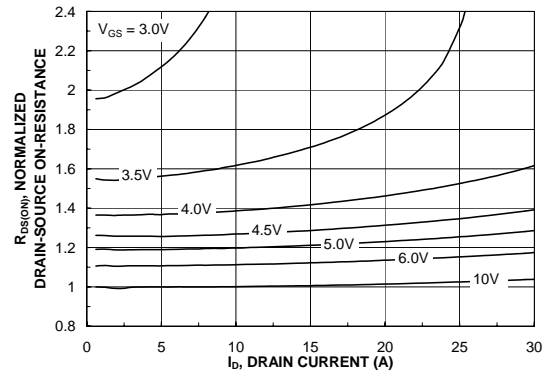
Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.
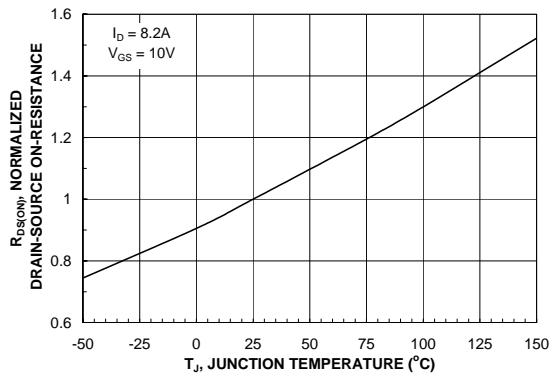
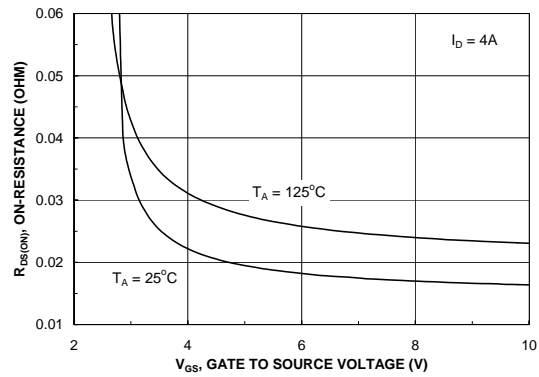**Figure 3. On-Resistance Variation with Temperature.**

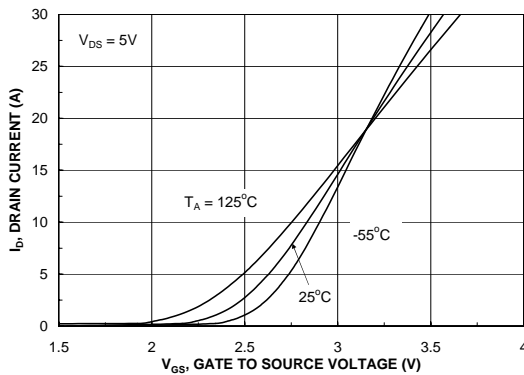**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**
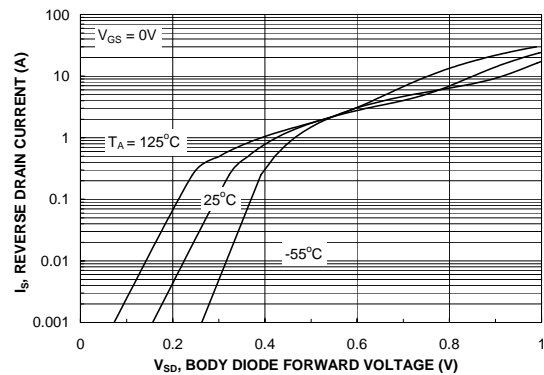
Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.
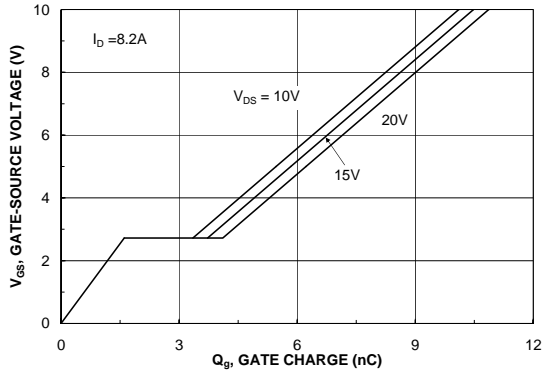
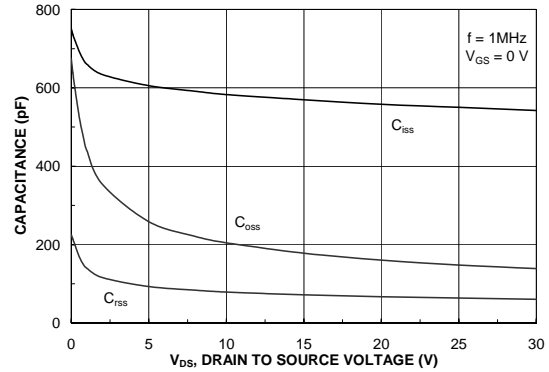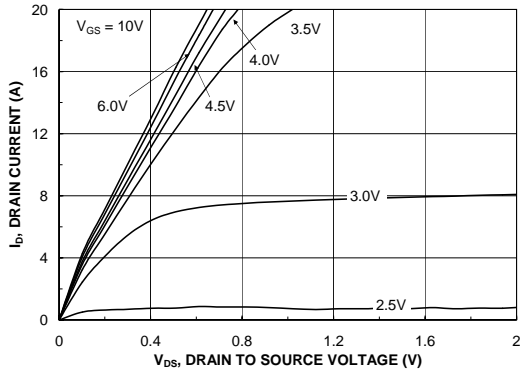## Typical Characteristics: Q2

Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.
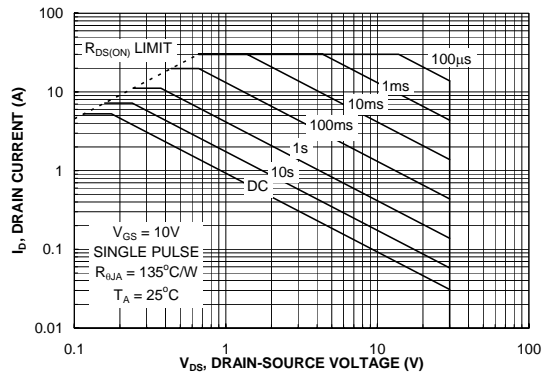
Figure 9. Maximum Safe Operating Area.
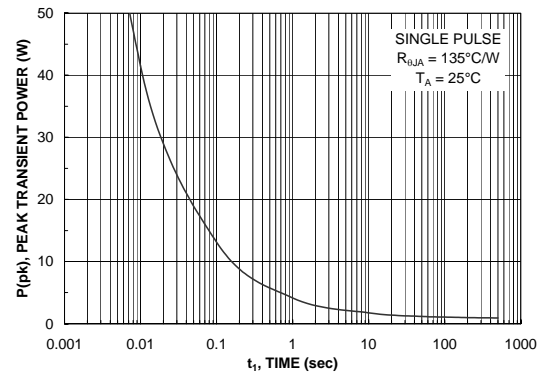
Figure 10. Single Pulse Maximum
Power Dissipation.
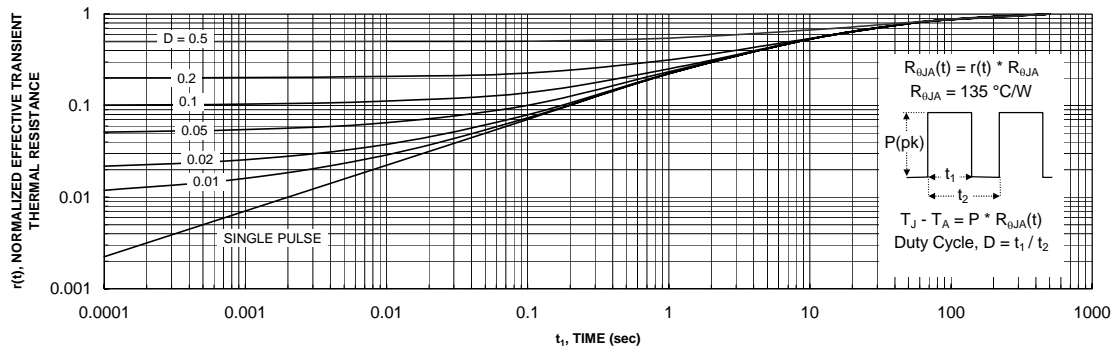
Figure 11. Transient Thermal Response Curve.

**Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.**

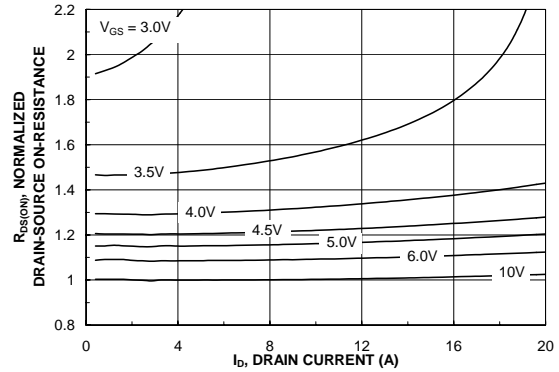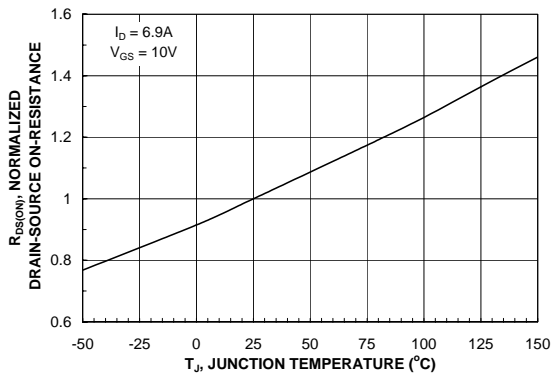## Typical Characteristics Q1

Figure 12. On-Region Characteristics.

Figure 13. On-Resistance Variation with Drain Current and Gate Voltage.

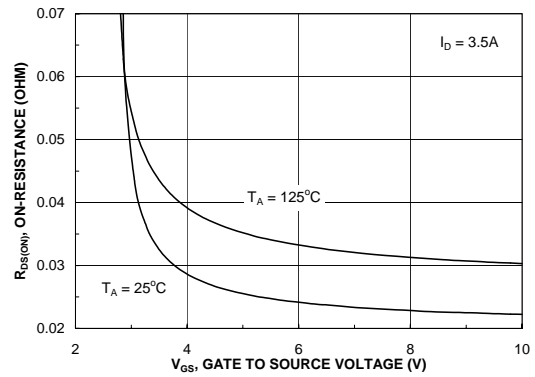Figure 14. On-Resistance Variation with Temperature.

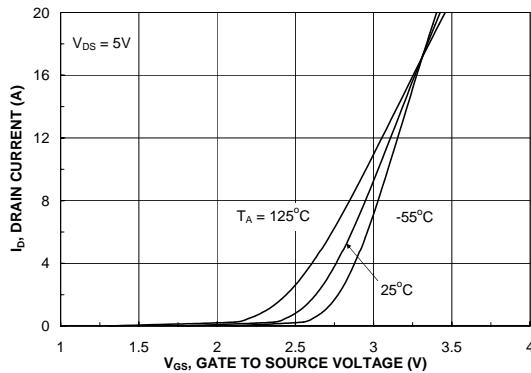Figure 15. On-Resistance Variation with Gate-to-Source Voltage.
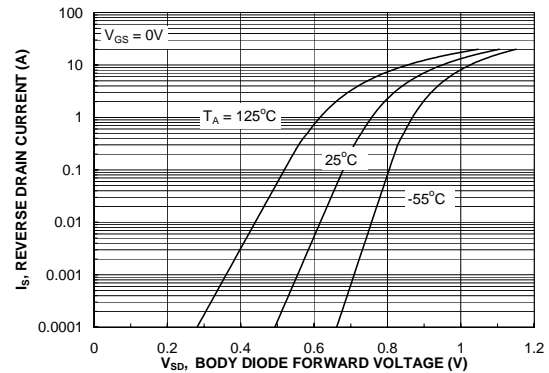
Figure 16. Transfer Characteristics.

Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature.
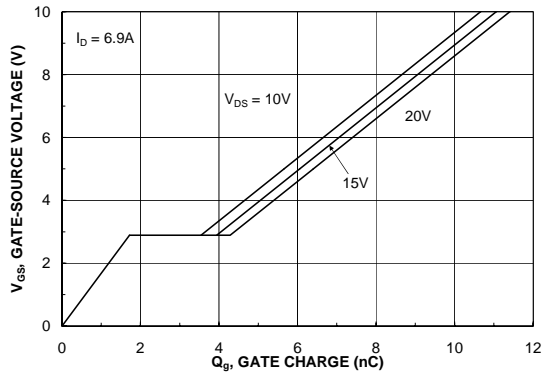
Typical Characteristics Q1
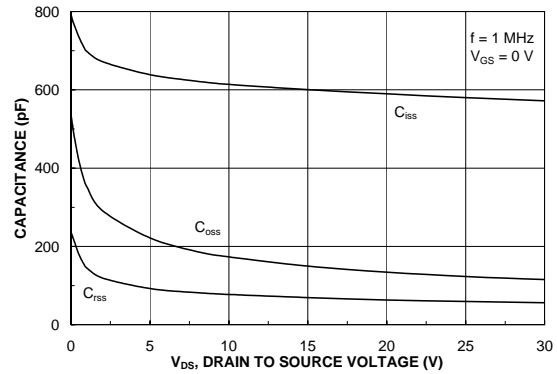

Figure 18. Gate Charge Characteristics.

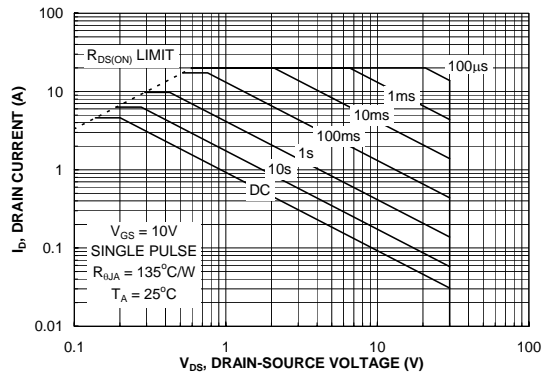Figure 19. Capacitance Characteristics.

Figure 20. Maximum Safe Operating Area.

Figure 21. Single Pulse Maximum
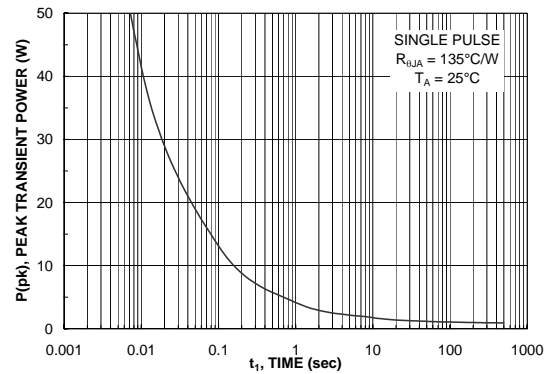Power Dissipation.

$$R_{\theta JA}(t) = r(t) * R_{\theta JA}$$
$$R_{\theta JA} = 135^\circ C/W$$

$$T_J - T_A = P * R_{\theta JA}(t)$$
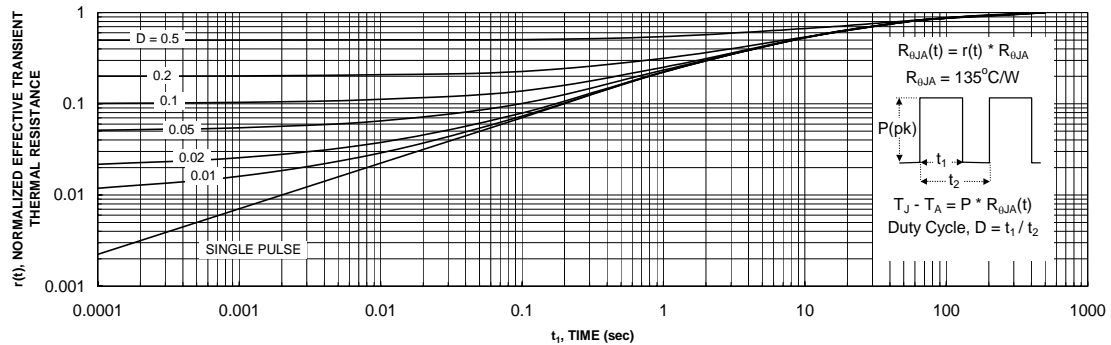Duty Cycle, $D = t_1 / t_2$

Figure 22. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics (continued)

SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. **Figure 23** shows the reverse recovery characteristic of the FDS6900AS.
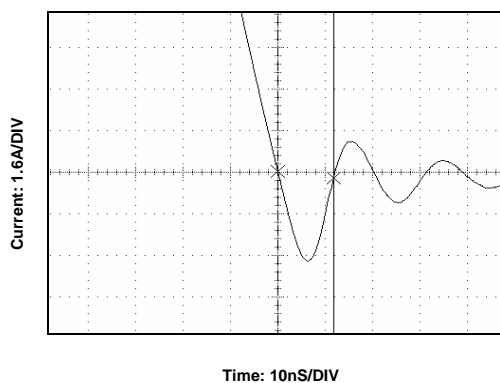

Current: 1.6A/DIV

Time: 10nS/DIV

Figure 23. FDS6900AS SyncFET body diode reverse recovery characteristic.

For comparison purposes, **Figure 24** shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDS6690).
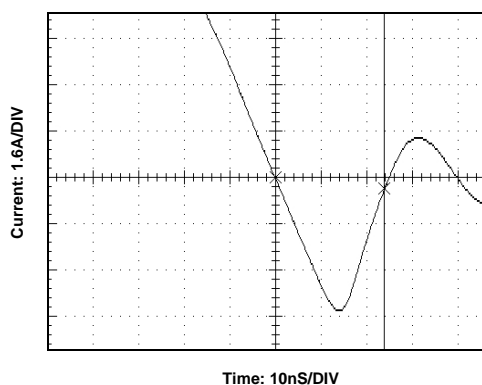

Current: 1.6A/DIV

Time: 10nS/DIV

Figure 24. Non-SyncFET (FDS6690) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.
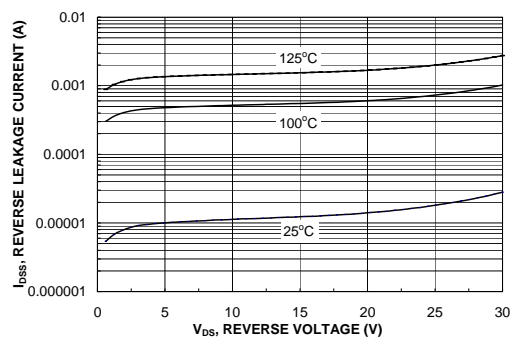

Figure 25. SyncFET body diode reverse leakage versus drain-source voltage and temperature

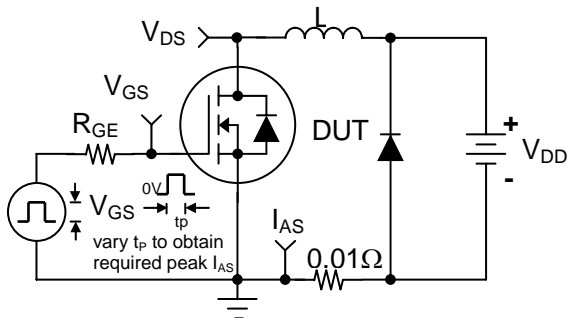## Typical Characteristics

Figure 26. Unclamped Inductive Load Test Circuit
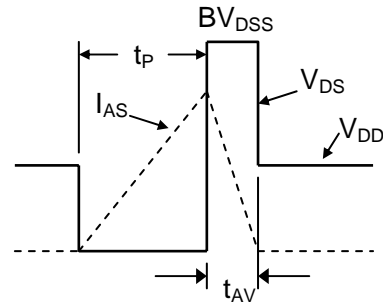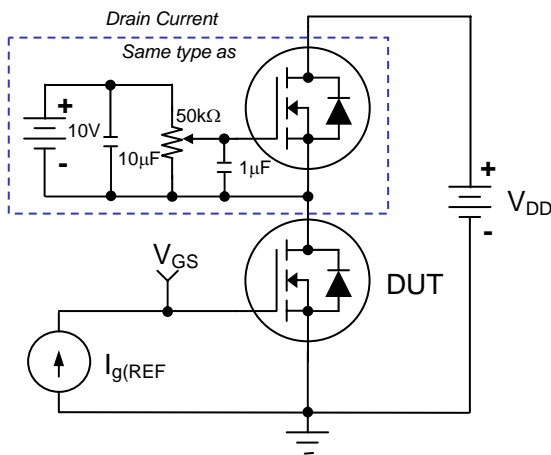

Figure 27. Unclamped Inductive Waveforms
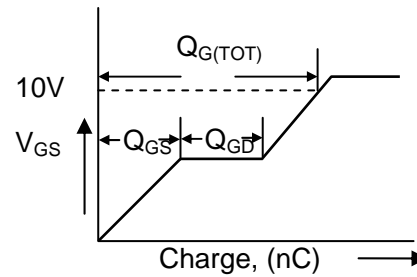

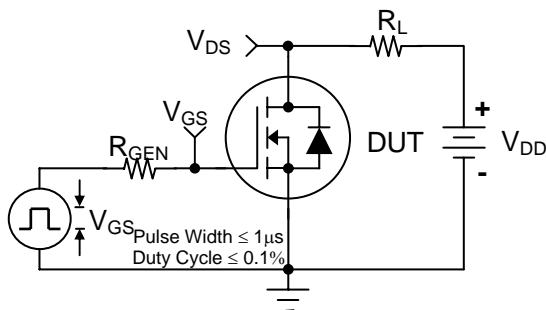Figure 28. Gate Charge Test Circuit

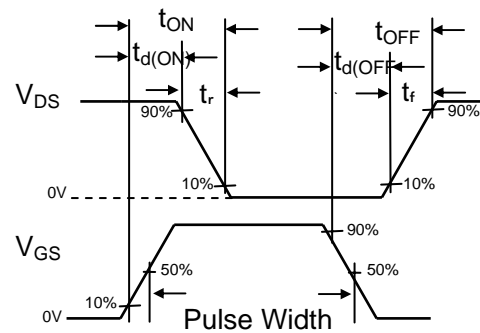Figure 29. Gate Charge Waveform

Figure 30. Switching Time Test Circuit

Figure 31. Switching Time Waveforms

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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