FAIRCHILD SEMICONDUCTOR TM

November 1999
ADVANCE INFORMATION

FDZ202P

P-Channel 2.5V Specified PowerTrench™ BGA MOSFET

General Description

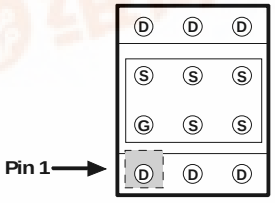
Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ202P minimizes both PCB space and $R_{DS(ON)}$. This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $R_{DS(ON)}$.

Applications

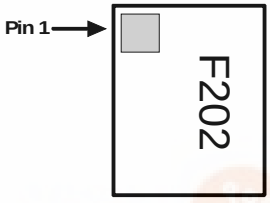
- Battery management
- Load switch
- Battery protection

Features

- –5.5 A, –20 V. $R_{DS(ON)}$ = 0.045 Ω @ V_{GS} = –4.5 V
  $R_{DS(ON)}$ = 0.075 Ω @ V_{GS} = –2.5 V.
- Occupies only 5 mm^2 of PCB area.
  Only 55% of the area of SSOT-6
- Ultra-thin package: less than 0.70 mm height when mounted to PCB
- Outstanding thermal transfer characteristics:
  4 times better than SSOT-6
- Ultra-low Q_g x $R_{DS(ON)}$ figure-of-merit.
- High power and current handling capability.



Bottom



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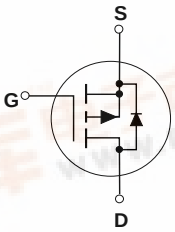


Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		–20	V
V_{GSS}	Gate-Source Voltage		±12	V
I_D	Drain Current – Continuous	(Note 1a)	–5.5	A
	– Pulsed		–20	
P_D	Power Dissipation (Steady State)	(Note 1a)	2.7	W
T_J, T_{stg}	Operating and Storage Junction Temperature Range		-55 to +175	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	55	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	8	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
F202	FDZ202P	TBD	TBD	TBD

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = –250 μA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = –250 μA, Referenced to 25°C		28		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = –16 V, V_{GS} = 0 V			–1	μA
I_{GSSF}	Gate–Body Leakage Current, Forward	V_{GS} = –12 V, V_{DS} = 0 V			–100	nA
I_{GSSR}	Gate–Body Leakage Current, Reverse	V_{GS} = 12 V V_{DS} = 0 V			100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = –250 μA	–0.4	–0.9	–1.5	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = –4.5 V, I_D = –5.5 A V_{GS} = –2.5 V, I_D = –4.0 A		0.036 0.060	0.045 0.075	Ω
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				–2.3	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = –2.3 A (Note 2)		–0.77	–1.2	V

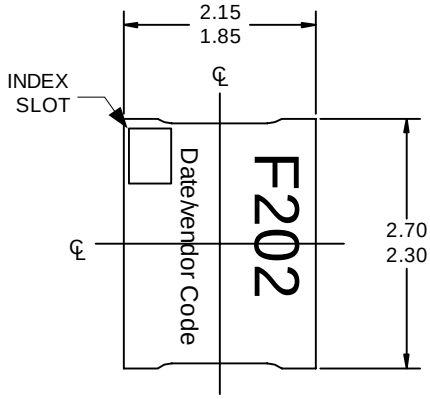
Notes:

1. $R_{\theta JA}$ is the a function of the junction-to-case ($R_{\theta JC}$), case-to-ambient ($R_{\theta CA}$) and the PC Board ($R_{\theta BA}$) thermal resistance where the case thermal reference is defined the top surface of the package. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ and $R_{\theta BA}$ are determined by the user's design.

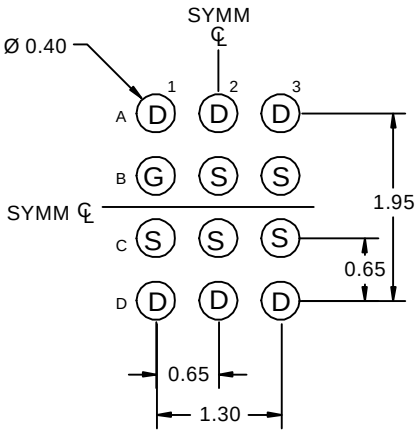
(a). $R_{\theta JA}$ = 55°C/W (steady-state) when mounted on 1 in^2 of 2 oz. copper.

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

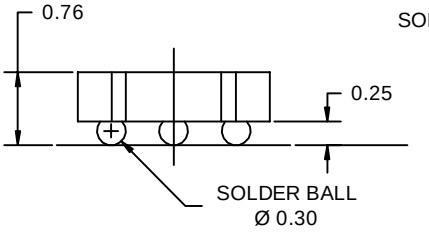
Dimensional Outline and Pad Layout



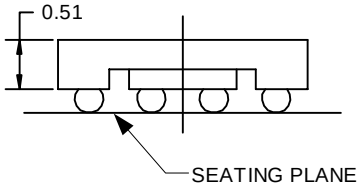
TOP VIEW



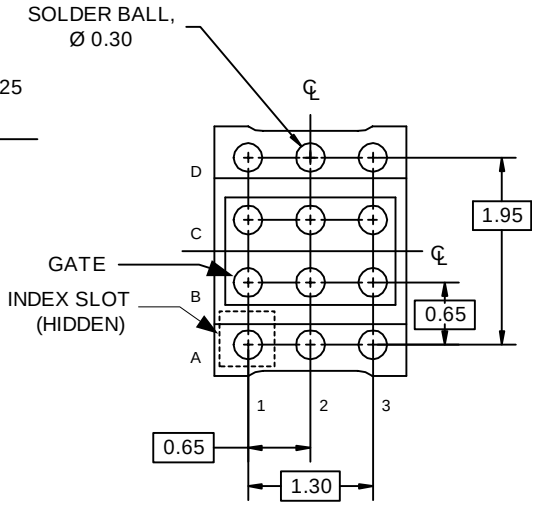
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
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