

November 1999 ADVANCE INFORMATION

FDZ2551N

Dual N-Channel 2.5V Specified PowerTrench™ BGA MOSFET

General Description

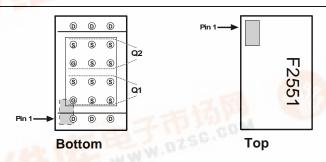
Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ2551N minimizes both PCB space and $R_{DS(ON)}$. This dual BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultralow profile packaging, low gate charge, and low $R_{DS(ON)}$.

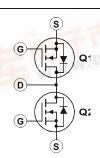
Applications

- · Battery management
- Load switch
- Battery protection

Features

- 9 A, 20 V. $R_{DS(ON)} = 0.018 \ \Omega \ @ \ V_{GS} = 4.5 \ V$ $R_{DS(ON)} = 0.030 \ \Omega \ @ \ V_{GS} = 2.5 \ V.$
- Occupies only 0.10 cm² of PCB area.
 1/3 the area of SO-8.
- Ultra-thin package: less than 0.70 mm height when mounted to PCB.
- Outstanding thermal transfer characteristics: significantly better than SO-8.
- Ultra-low $Q_g \times R_{DS(ON)}$ figure-of-merit.
- High power and current handling capability.





Absolute Maximum Ratings T_A=25°C unless otherwise noted

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Symbol	Parameter		Ratings		
V _{DSS}	Drain-Source Voltage		20	V	
V_{GSS}	Gate-Source Voltage		±12	V	
I _D	Drain Current - Continuous	(Note 1a)	9	Α	
	- Pulsed		20		
P _D	Power Dissipation (Steady State)	(Note 1a)	3	W	
T.I. T _{sta}	Operating and Storage Junction Temperature Range		-55 to +175	°C	

Thermal Characteristics

R _{0JA}	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
R _{eJC}	Thermal Resistance, Junction-to-Case	(Note 1)	8	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
F2551	FDZ2551N	TBD	TBD	TBD

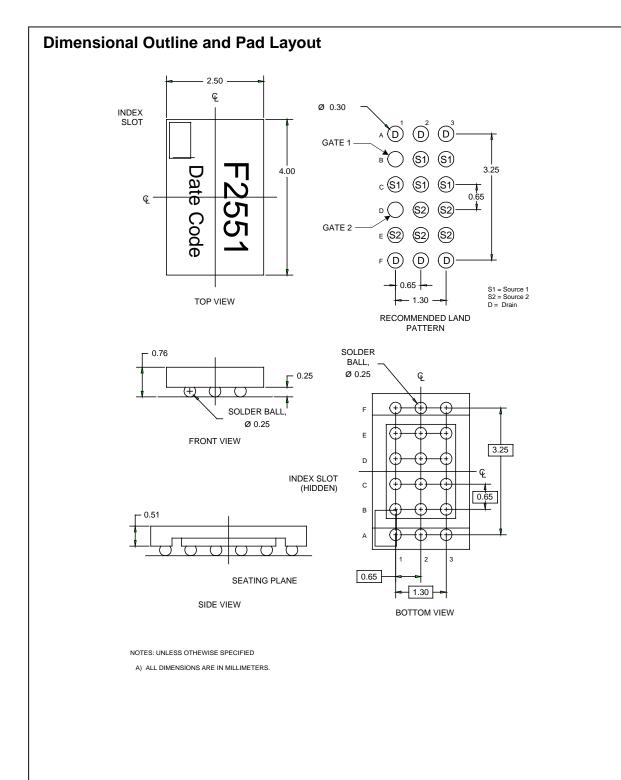
Electrical Characteristics T _A = 25°C unless otherwise noted						
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics		•			•
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	20			V
$\Delta BV_{DSS} \over \Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A,Referenced to 25°C		14		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			1	μΑ
I _{GSSF}	Gate–Body Leakage Current, Forward	$V_{GS} = 12 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage Current, Reverse	$V_{GS} = -12 \text{ V}$ $V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	0.4	0.9	1.5	V
R _{DS(on)}	Static Drain–Source On–Resistance	$ \begin{array}{cccccccccccccccccccccccccccccccccccc$			0.018 0.030	Ω
Drain-S	ource Diode Characteristics a	nd Maximum Ratings		•	•	
Is	Maximum Continuous Drain-Source	num Continuous Drain–Source Diode Forward Current 2.5 A			Α	
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.5 \text{ A} \text{(Note 2)}$		0.77	1.2	V

Notes

R_{eJA} is a function of the junction-to-case (R_{eJC}), case-to-ambient (R_{eCA}) and the PC Board (R_{eBA}) thermal resistance. For the purpose of determining R_{eJC} the case thermal reference is defined as the top surface of the package. R_{eJC} is guaranteed by design while R_{eCA} and R_{eBA} are determined by the user's design. Maximum current ratings assume single device operation.

⁽a). $\rm R_{\rm \theta JA} = 50^{\circ} C/W$ (steady-state) when mounted on 1 in 2 of 2 oz. copper.

^{2.} Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%





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