

4A, 100V, 0.60 Ohm, P-Channel Power MOSFET

This P-Channel enhancement mode silicon gate power field effect transistor is designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17501.

Ordering Information

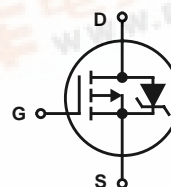
PART NUMBER	PACKAGE	BRAND
IRFF9120	TO-205AF	IRFF9120

NOTE: When ordering, use the entire part number.

Features

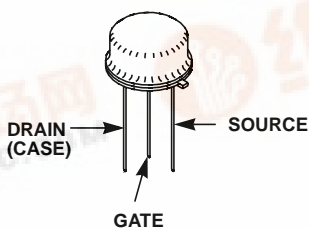
- 4A, 100V
- $r_{DS(ON)} = 0.60\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol



Packaging

JEDEC TO-205AF



IRFF9120

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

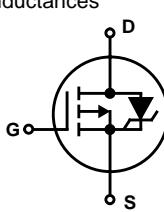
	IRFF9120	UNITS
Drain to Source Voltage (Note 1)	-100	V
Drain to Gate Voltage ($R_{GS} = 20\text{k}\Omega$) (Note 1)	-100	V
Continuous Drain Current, $T_C = 25^\circ\text{C}$	-4	A
Pulsed Drain Current (Note 3)	-16	A
Gate to Source Voltage	± 20	V
Maximum Power Dissipation, (Figure 14)	20	W
Linear Derating Factor (Figure 14)	0.16	$\text{W}/^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 4)	370	mJ
Operating and Storage Temperature	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. $T_J = 25^\circ\text{C}$ to 125°C .

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}$, $I_D = 250\mu\text{A}$	-100	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	-2.0	-	-4.0	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Max Rating}$, $V_{GS} = 0\text{V}$	-	-	-250	μA	
		$V_{DS} = \text{Max Rating} \times 0.8$, $V_{GS} = 0\text{V}$, $T_J = 125^\circ\text{C}$	-	-	-1000	μA	
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $V_{GS} = -10\text{V}$	-4	-	-	A	
Gate to Source Leakage Forward	I_{GSS}	$V_{GS} = -20\text{V}$	-	-	-100	nA	
Gate to Source Leakage Reverse	I_{GSS}	$V_{GS} = 20\text{V}$	-	-	100	nA	
Drain to Source On-State Resistance (Note 2)	$r_{DS(ON)}$	$V_{GS} = 10\text{V}$, $I_D = -2\text{A}$	-	0.5	0.6	Ω	
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}$, $I_D = 2\text{A}$	1.25	2	-	S	
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} \cong 0.5BV_{DSS}$, $I_D = 4\text{A}$, $R_G = 9.1\Omega$ (Figure 18) MOSFET Switching Times are Essentially Independent of Operating Temperature	-	25	50	ns	
Rise Time	t_r		-	50	100	ns	
Turn-Off Delay Time	$t_{D(OFF)}$		-	50	100	ns	
Fall Time	t_f		-	50	100	ns	
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{G(TOT)}$	$V_{GS} = 10\text{V}$, $I_D = 4\text{A}$, $V_{DS} = 0.8 \text{ Max } BV_{DSS}$ (See Figure 18 for Test Circuit) Gate Charge is Essentially Independent of Operating Temperature	-	16	22	nC	
Gate to Source Charge	Q_{GS}		-	9	-	nC	
Gate to Drain "Miller" Charge	Q_{GD}		-	7	-	nC	
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1.0\text{MHz}$, See Figure 10	-	300	-	pF	
Output Capacitance	C_{OSS}		-	200	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF	
Internal Drain Inductance	L_D	Measured from the Drain Lead, 5.0mm (0.2in) From Header to Center of Die	Modified MOSFET Symbol Showing the Internal Device Inductances 	-	5.0	-	nH
Internal Source Inductance	L_S	Measured from the Source Lead, 5.0mm (0.2in) from Header to Source Bonding Pad		-	15	-	nH
Junction to Case	$R_{\theta JC}$		-	-	6.25	$^\circ\text{C}/\text{W}$	
Junction to Ambient	$R_{\theta JA}$	Typical Socket Mount	-	-	175	$^\circ\text{C}/\text{W}$	

IRFF9120

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Rectifier	-	-	-4	A
Pulse Source Current (Note 3)	I_{SM}		-	-	-16	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^{\circ}\text{C}$, $I_{SD} = -4\text{A}$, $V_{GS} = 0\text{V}$	-	-	-1.5	V
Diode Reverse Recovery Time	t_{rr}	$T_J = 150^{\circ}\text{C}$, $I_{SD} = 4\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	230	-	ns
Reverse Recovery Charge	Q_{RR}	$T_J = 150^{\circ}\text{C}$, $I_{SD} = -4\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	1.3	-	μC

NOTES:

- Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty Cycle 2%.
- Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance Curve (Figure 3).
- $V_{DD} = 25\text{V}$, starting $T_J = 250^{\circ}\text{C}$, $L = 34.7\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 4.0\text{A}$. See Figures 15 and 16)

Typical Performance Curves

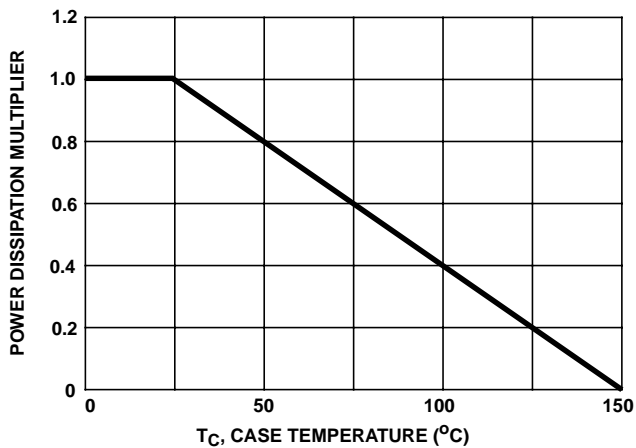


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

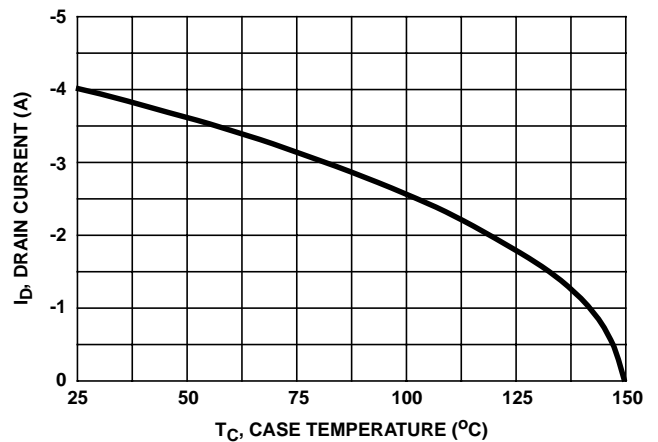


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

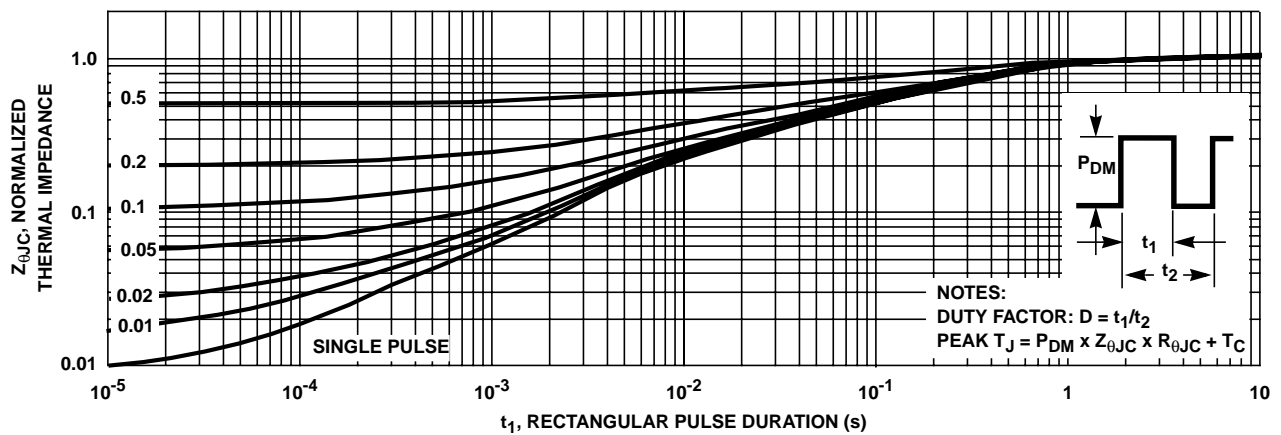


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

Typical Performance Curves (Continued)

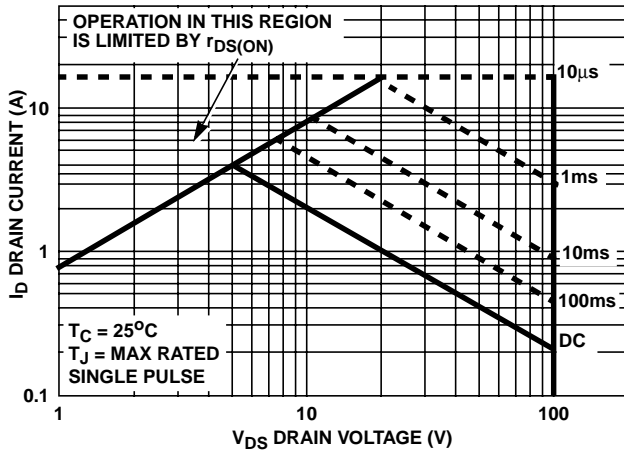


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

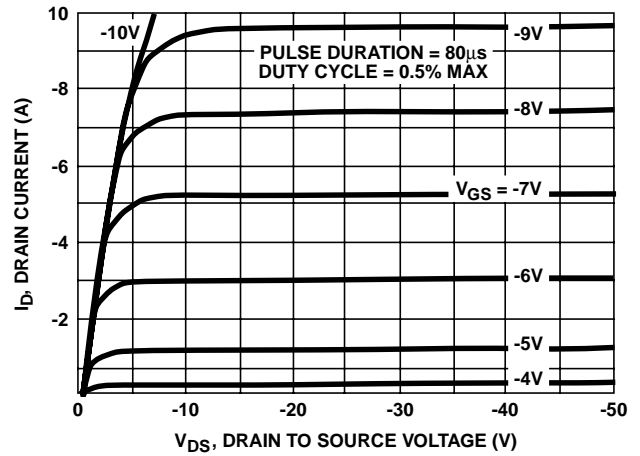


FIGURE 5. OUTPUT CHARACTERISTICS

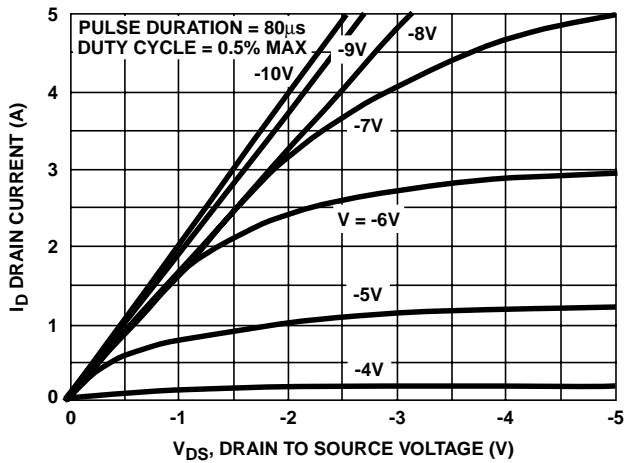


FIGURE 6. SATURATION CHARACTERISTICS

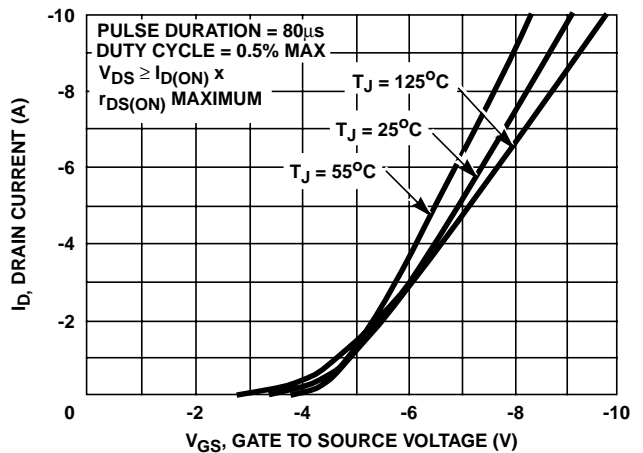


FIGURE 7. TRANSFER CHARACTERISTICS

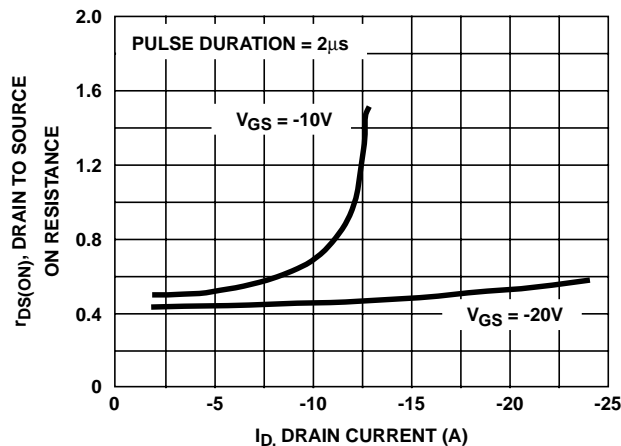


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

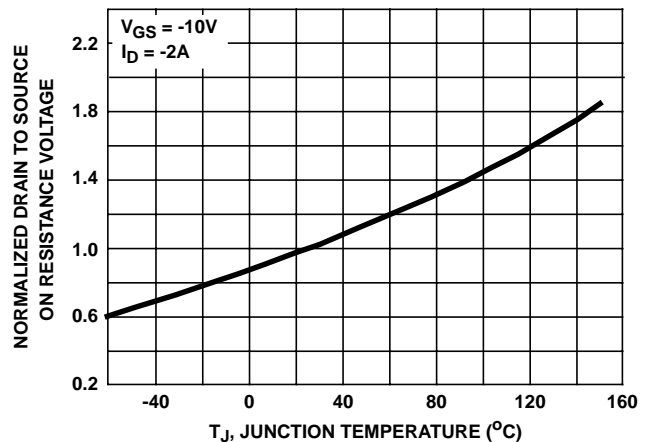


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

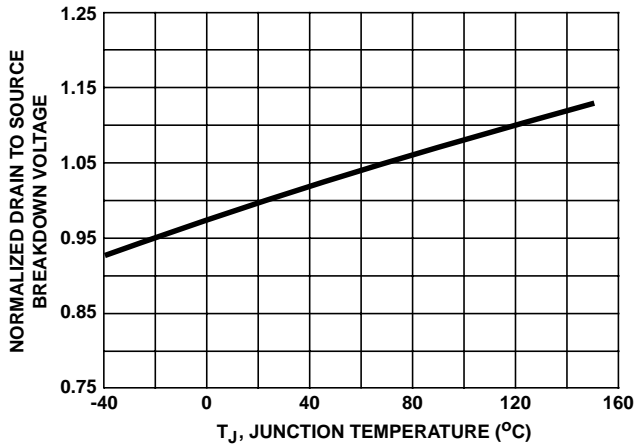


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

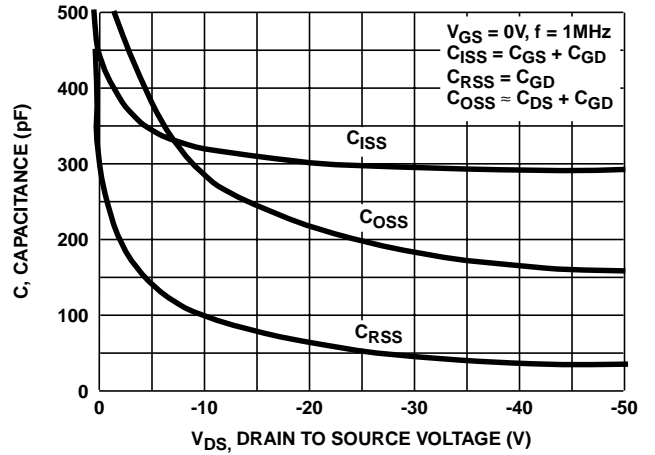


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

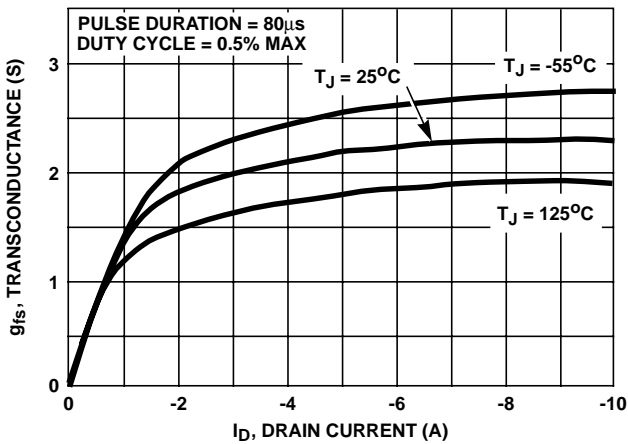


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

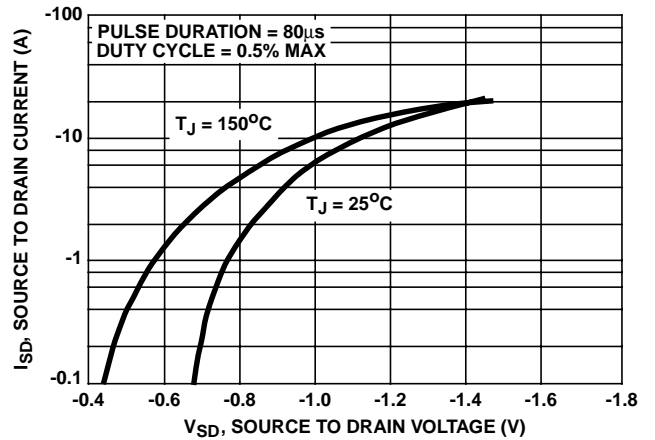


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

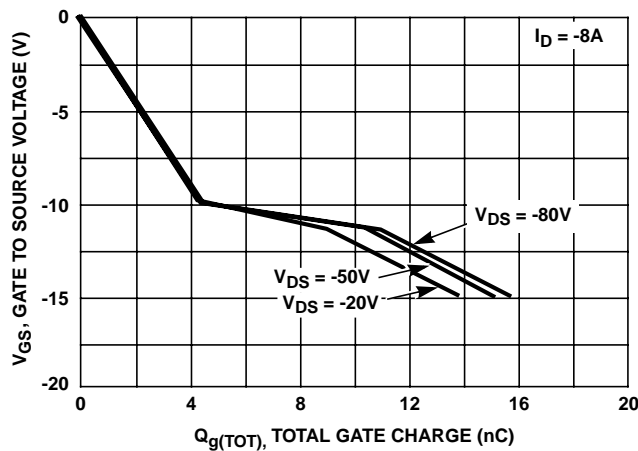


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

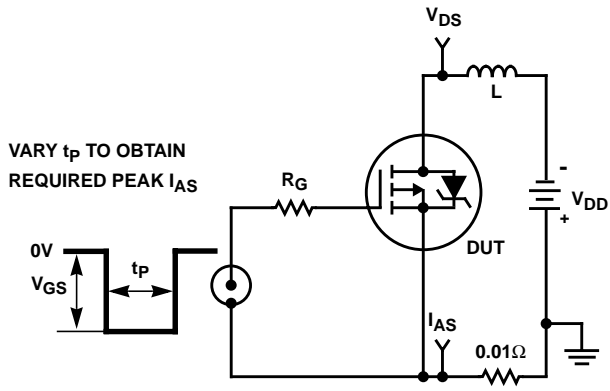


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

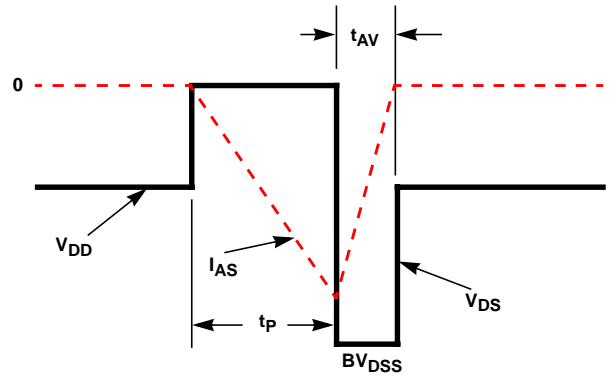


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

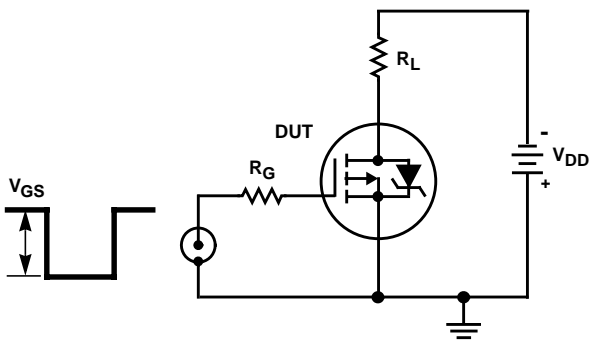


FIGURE 17. SWITCHING TIME TEST CIRCUIT

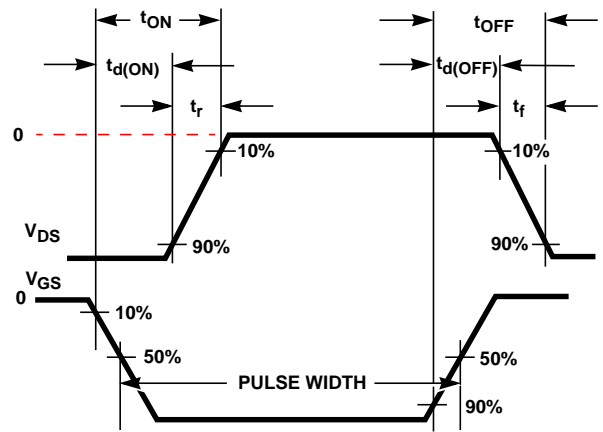


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

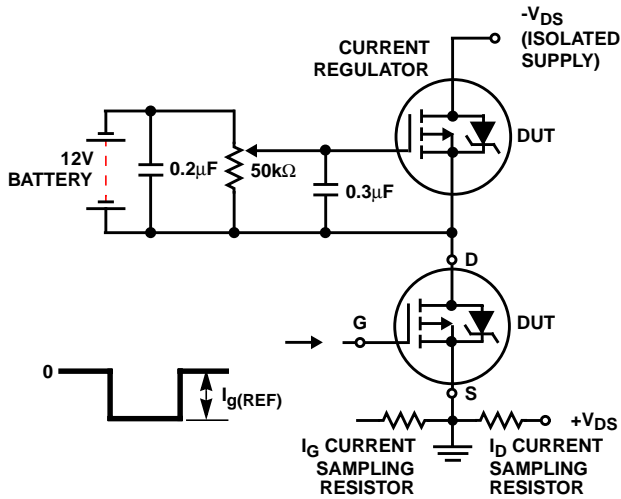


FIGURE 19. GATE CHARGE TEST CIRCUIT

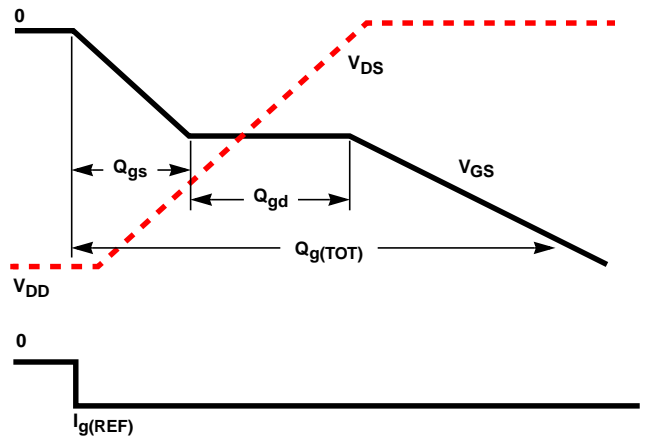


FIGURE 20. GATE CHARGE WAVEFORMS

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Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029