FAIRCHILD SEMICONDUCTOR®

August 2003

FGH40N6S2 / FGP40N6S2 / FGB40N6S2

600V, SMPS II Series N-Channel IGBT

General Description

The FGH40N6S2, FGP40N6S2 and the FGB40N6S2 are Low Gate Charge, Low Plateau Voltage SMPS II IGBTs combining the fast switching speed of the SMPS IGBTs along with lower gate charge, plateau voltage and avalanche capability (UIS). These LGC devices shorten delay times, and reduce the power requirement of the gate drive. These devices are ideally suited for high voltage switched mode power supply applications where low conduction loss, fast switching times and UIS capability are essential. SMPS II LGC devices have been specially designed for:

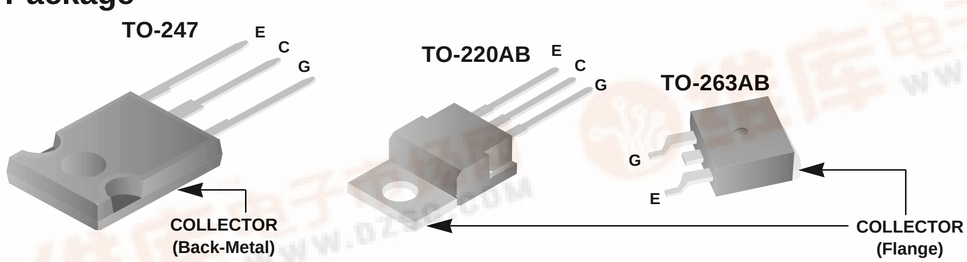
- Power Factor Correction (PFC) circuits
- Full bridge topologies
- Half bridge topologies
- Push-Pull circuits
- Uninterruptible power supplies
- Zero voltage and zero current switching circuits

IGBT (co-pack) formerly Developmental Type TA49438

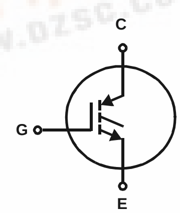
Features

- 100kHz Operation at 390V, 24A
- 200kHZ Operation at 390V, 18A
- 600V Switching SOA Capability
- Typical Fall Time. . . . . 85ns at TJ = 125°C
- Low Gate Charge . . . . 35nC at V_{GE} = 15V
- Low Plateau Voltage . . . . .6.5V Typical
- UIS Rated 260mJ
- Low Conduction Loss

Package



Symbol



Device Maximum Ratings T_C= 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
BV_{CES}	Collector to Emitter Breakdown Voltage	600	V
I_{C25}	Collector Current Continuous, T_C = 25°C	75	A
I_{C110}	Collector Current Continuous, T_C = 110°C	35	A
I_{CM}	Collector Current Pulsed (Note 1)	180	A
V_{GES}	Gate to Emitter Voltage Continuous	±20	V
V_{GEM}	Gate to Emitter Voltage Pulsed	±30	V
SSOA	Switching Safe Operating Area at T_J = 150°C, Figure 2	100A at 600V	
E_{AS}	Pulsed Avalanche Energy, I_{CE} = 30A, L = 1mH, V_{DD} = 50V	260	mJ
P_D	Power Dissipation Total T_C = 25°C	290	W
	Power Dissipation Derating T_C > 25°C	2.33	W/°C
T_J	Operating Junction Temperature Range	-55 to 150	°C
T_{STG}	Storage Junction Temperature Range	-55 to 150	°C

CAUTION: Stresses above those listed in "Device Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. Pulse width limited by maximum junction temperature.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
40N6S2	FGH40N6S2	TO-247	Tube	N/A	30
40N6S2	FGP40N6S2	TO-220AB	Tube	N/A	50
40N6S2	FGB40N6S2	TO-263AB	Tube	N/A	50
40N6S2	FGB40N6S2T	TO-263AB	330mm	24mm	800

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Off State Characteristics							
BV_{CES}	Collector to Emitter Breakdown Voltage	I_C = 250μA, V_{GE} = 0		600	-	-	V
BV_{ECS}	Emitter to Collector Breakdown Voltage	I_C = -10mA, V_{GE} = 0		20	-	-	V
I_{CES}	Collector to Emitter Leakage Current	V_{CE} = 600V	T_J = 25°C	-	-	250	μA
			T_J = 125°C	-	-	2.0	mA
I_{GES}	Gate to Emitter Leakage Current	V_{GE} = ± 20V		-	-	±250	nA
On State Characteristics							
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 20A, V_{GE} = 15V	T_J = 25°C	-	1.9	2.7	V
			T_J = 125°C	-	1.7	2.0	V
Dynamic Characteristics							
$Q_{G(ON)}$	Gate Charge	I_C = 20A, V_{CE} = 300V	V_{GE} = 15V	-	35	42	nC
			V_{GE} = 20V	-	45	55	nC
$V_{GE(TH)}$	Gate to Emitter Threshold Voltage	I_C = 250μA, V_{CE} = V_{GE}		3.5	4.3	5.0	V
V_{GEP}	Gate to Emitter Plateau Voltage	I_C = 20A, V_{CE} = 300V		-	6.5	8.0	V
Switching Characteristics							
SSOA	Switching SOA	T_J = 150°C, V_{GE} = 15V, R_G = 3Ω L = 100μH, V_{CE} = 600V		100	-	-	A
$t_{d(ON)I}$	Current Turn-On Delay Time	IGBT and Diode at T_J = 25°C, I_{CE} = 20A, V_{CE} = 390V, V_{GE} = 15V, R_G = 3Ω L = 200μH Test Circuit - Figure 26		-	8.0	-	ns
t_{rI}	Current Rise Time			-	10	-	ns
$t_{d(OFF)I}$	Current Turn-Off Delay Time			-	35	-	ns
t_{fI}	Current Fall Time			-	55	-	ns
E_{ON1}	Turn-On Energy (Note 2)			-	115	-	μJ
E_{ON2}	Turn-On Energy (Note 2)			-	200	-	μJ
E_{OFF}	Turn-Off Energy (Note 3)			-	195	260	μJ
$t_{d(ON)I}$	Current Turn-On Delay Time	IGBT and Diode at T_J = 125°C I_{CE} = 20A, V_{CE} = 390V, V_{GE} = 15V, R_G = 3Ω L = 200μH Test Circuit - Figure 26		-	14	-	ns
t_{rI}	Current Rise Time			-	18	-	ns
$t_{d(OFF)I}$	Current Turn-Off Delay Time			-	68	85	ns
t_{fI}	Current Fall Time			-	85	105	ns
E_{ON1}	Turn-On Energy (Note 2)			-	115	-	μJ
E_{ON2}	Turn-On Energy (Note 2)			-	380	450	μJ
E_{OFF}	Turn-Off Energy (Note 3)			-	375	600	μJ
Thermal Characteristics							
$R_{\theta JC}$	Thermal Resistance Junction-Case	TO-247		-	-	0.43	°C/W

NOTE:

2. Values for two Turn-On loss conditions are shown for the convenience of the circuit designer. E_{ON1} is the turn-on loss of the IGBT only. E_{ON2} is the turn-on loss when a typical diode is used in the test circuit and the diode is at the same T_J as the IGBT. The diode type is specified in figure 26.

3. Turn-Off Energy Loss (E_{OFF}) is defined as the integral of the instantaneous power loss starting at the trailing edge of the input pulse and ending at the point where the collector current equals zero (I_{CE} = 0A). All devices were tested per JEDEC Standard No. 24-1 Method for Measurement of Power Device Turn-Off Switching Loss. This test method produces the true total Turn-Off Energy Loss.

Typical Performance Curves T_J = 25°C unless otherwise noted

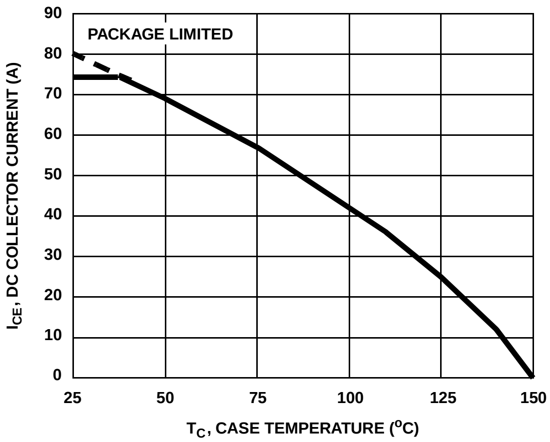


Figure 1. DC Collector Current vs Case Temperature

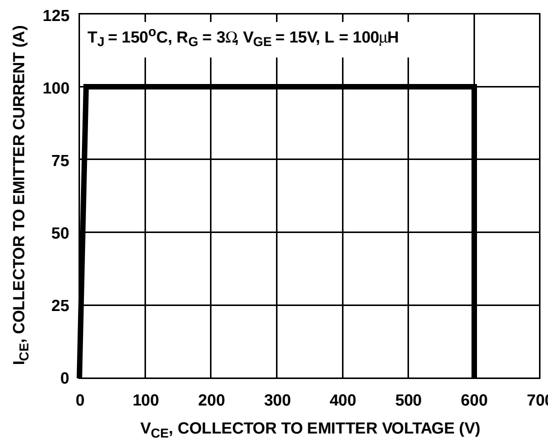


Figure 2. Minimum Switching Safe Operating Area

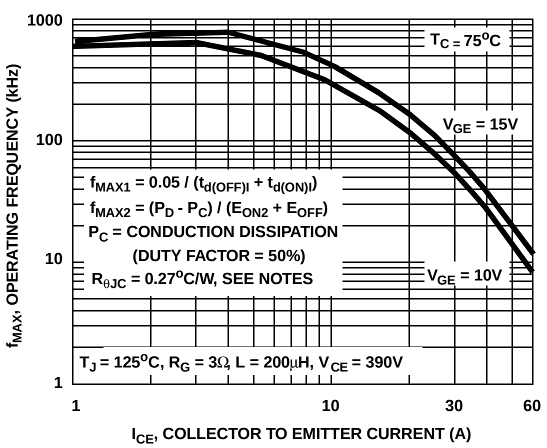


Figure 3. Operating Frequency vs Collector to Emitter Current

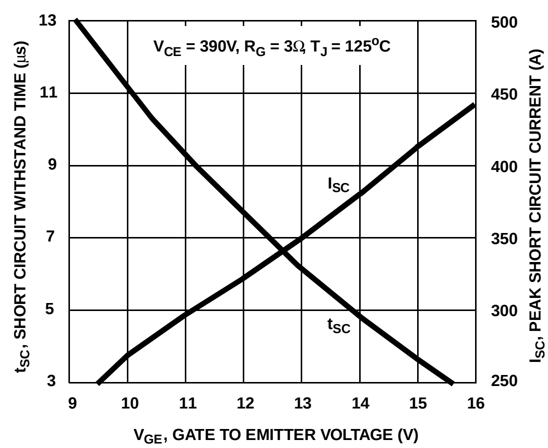


Figure 4. Short Circuit Withstand Time

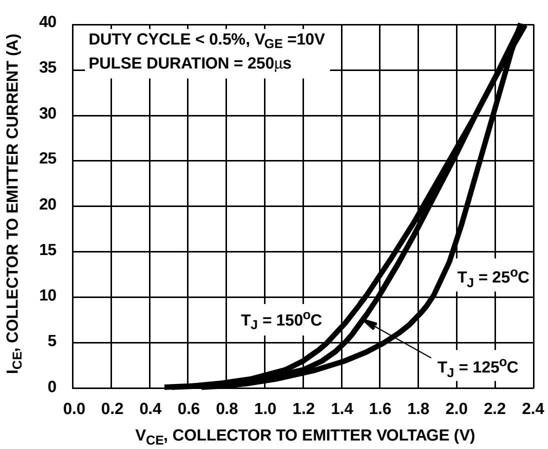


Figure 5. Collector to Emitter On-State Voltage

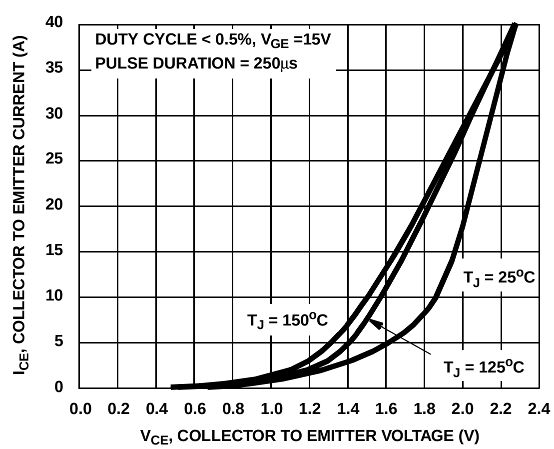


Figure 6. Collector to Emitter On-State Voltage

Typical Performance Curves T_J = 25°C unless otherwise noted

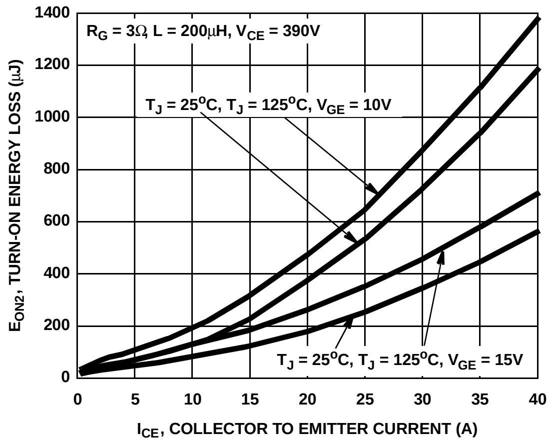


Figure 7. Turn-On Energy Loss vs Collector to Emitter Current

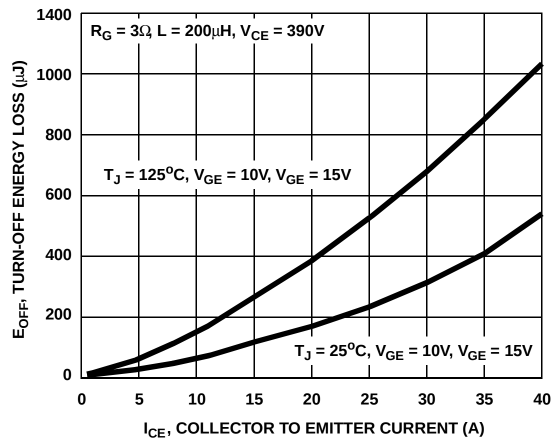


Figure 8. Turn-Off Energy Loss vs Collector to Emitter Current

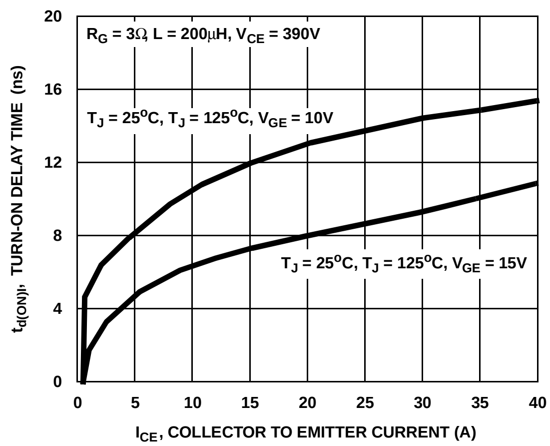


Figure 9. Turn-On Delay Time vs Collector to Emitter Current

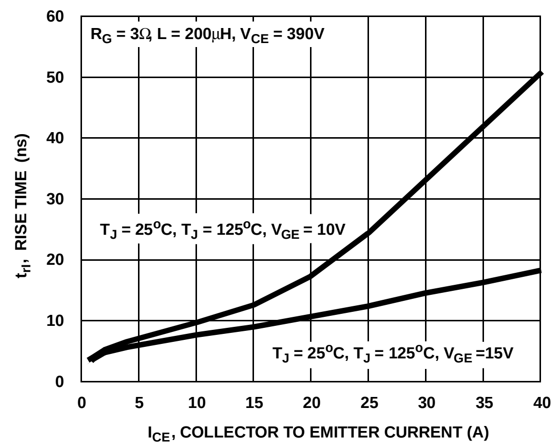


Figure 10. Turn-On Rise Time vs Collector to Emitter Current

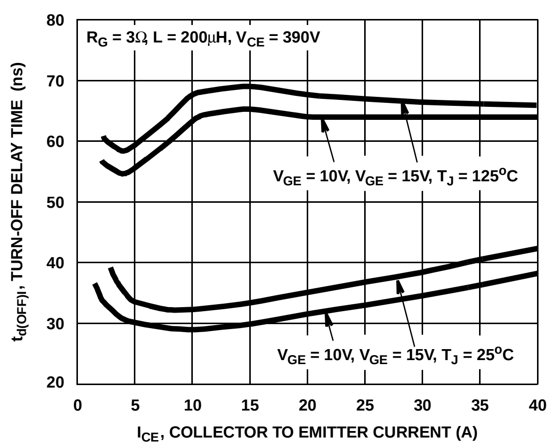


Figure 11. Turn-Off Delay Time vs Collector to Emitter Current

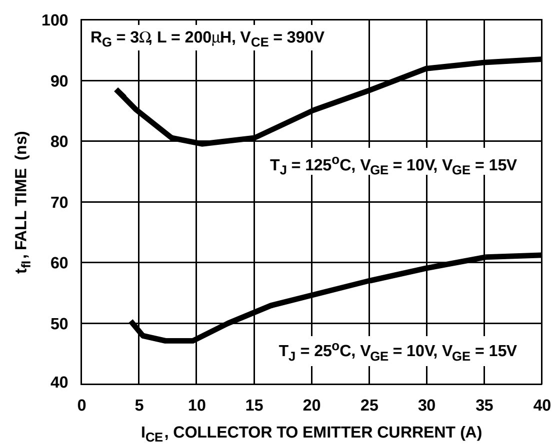


Figure 12. Fall Time vs Collector to Emitter Current

Typical Performance Curves T_J = 25°C unless otherwise noted

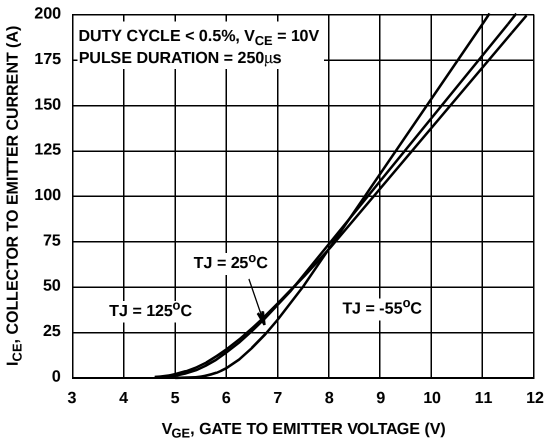


Figure 13. Transfer Characteristic

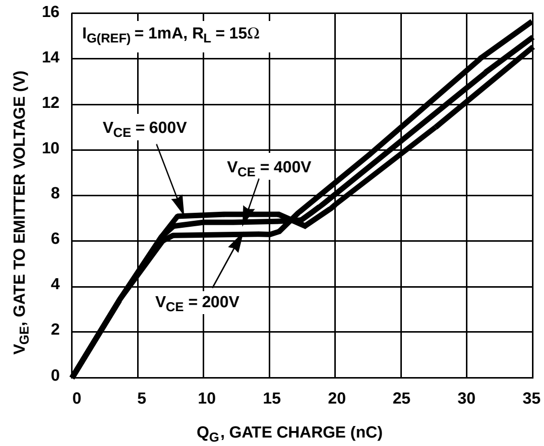


Figure 14. Gate Charge

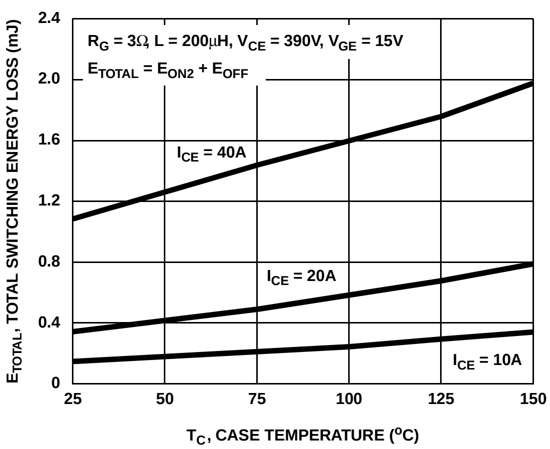


Figure 15. Total Switching Loss vs Case Temperature

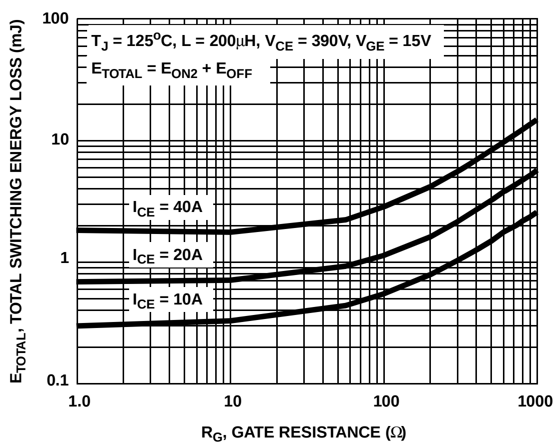


Figure 16. Total Switching Loss vs Gate Resistance

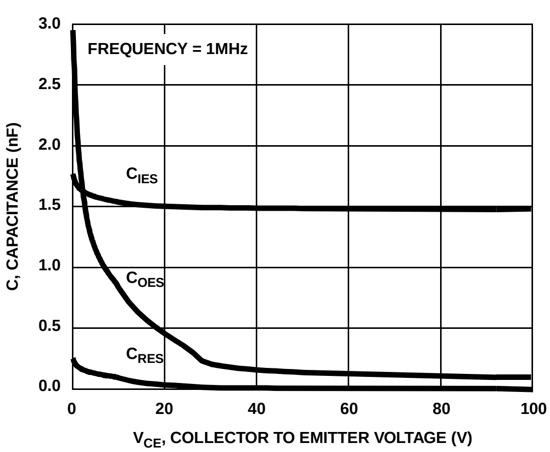


Figure 17. Capacitance vs Collector to Emitter Voltage

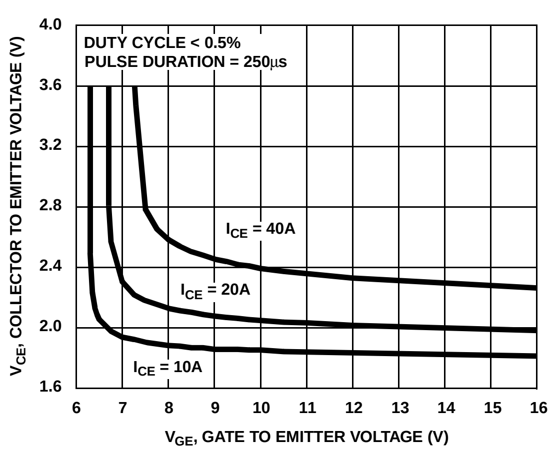


Figure 18. Collector to Emitter On-State Voltage vs Gate to Emitter Voltage

Typical Performance Curves T_J = 25°C unless otherwise noted

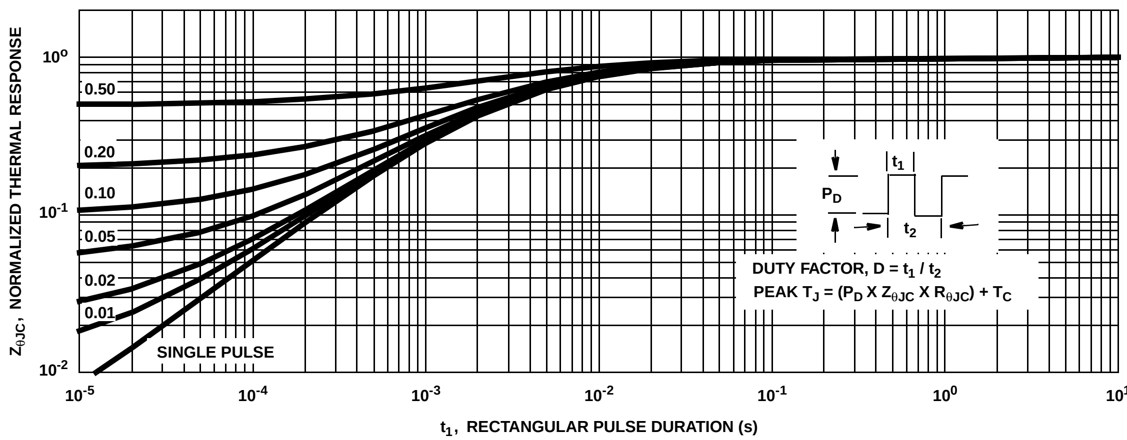


Figure 19. IGBT Normalized Transient Thermal Impedance, Junction to Case

Test Circuit and Waveforms

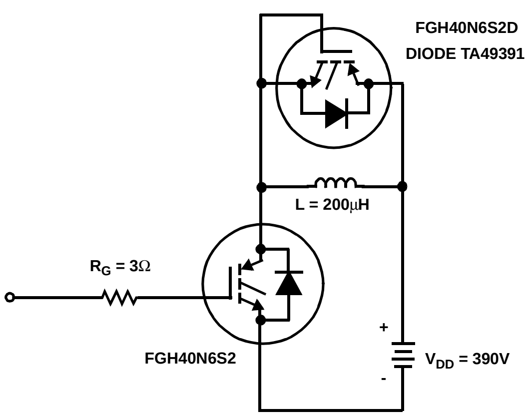


Figure 20. Inductive Switching Test Circuit

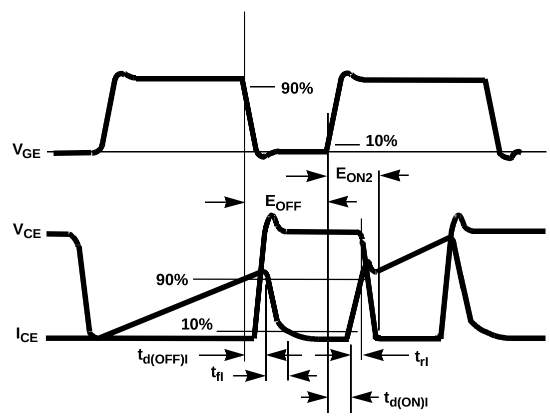


Figure 21. Switching Test Waveforms

Handling Precautions for IGBTs

Insulated Gate Bipolar Transistors are susceptible to gate-insulation damage by the electrostatic discharge of energy through the devices. When handling these devices, care should be exercised to assure that the static charge built in the handler's body capacitance is not discharged through the device. With proper handling and application procedures, however, IGBTs are currently being extensively used in production by numerous equipment manufacturers in military, industrial and consumer applications, with virtually no damage problems due to electrostatic discharge. IGBTs can be handled safely if the following basic precautions are taken:

1. Prior to assembly into a circuit, all leads should be kept shorted together either by the use of metal shorting springs or by the insertion into conductive material such as "ECCOSORBD™ LD26" or equivalent.
2. When devices are removed by hand from their carriers, the hand being used should be grounded by any suitable means - for example, with a metallic wristband.
3. Tips of soldering irons should be grounded.
4. Devices should never be inserted into or removed from circuits with power on.
5. **Gate Voltage Rating** - Never exceed the gate-voltage rating of V_{GEM}. Exceeding the rated V_{GE} can result in permanent damage to the oxide layer in the gate region.
6. **Gate Termination** - The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the device due to voltage buildup on the input capacitor due to leakage currents or pickup.
7. **Gate Protection** - These devices do not have an internal monolithic Zener diode from gate to emitter. If gate protection is required an external Zener is recommended.

Operating Frequency Information

Operating frequency information for a typical device (Figure 3) is presented as a guide for estimating device performance for a specific application. Other typical frequency vs collector current (I_{CE}) plots are possible using the information shown for a typical unit in Figures 5, 6, 7, 8, 9 and 11. The operating frequency plot (Figure 3) of a typical device shows f_{MAX1} or f_{MAX2}; whichever is smaller at each point. The information is based on measurements of a typical device and is bounded by the maximum rated junction temperature.

f_{MAX1} is defined by $f_{MAX1} = 0.05/(t_{d(OFF)I}+ t_{d(ON)I})$. Deadtime (the denominator) has been arbitrarily held to 10% of the on-state time for a 50% duty factor. Other definitions are possible. $t_{d(OFF)I}$ and $t_{d(ON)I}$ are defined in Figure 27. Device turn-off delay can establish an additional frequency limiting condition for an application other than T_{JM}. $t_{d(OFF)I}$ is important when controlling output ripple under a lightly loaded condition.

f_{MAX2} is defined by $f_{MAX2} = (P_D - P_C)/(E_{OFF} + E_{ON2})$. The allowable dissipation (P_D) is defined by $P_D = (T_{JM} - T_C)/R_{\theta JC}$. The sum of device switching and conduction losses must not exceed P_D. A 50% duty factor was used (Figure 3) and the conduction losses (P_C) are approximated by $P_C = (V_{CE} \times I_{CE})/2$.

E_{ON2} and E_{OFF} are defined in the switching waveforms shown in Figure 27. E_{ON2} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-on and E_{OFF} is the integral of the instantaneous power loss ($I_{CE} \times V_{CE}$) during turn-off. All tail losses are included in the calculation for E_{OFF}; i.e., the collector current equals zero ($I_{CE} = 0$)

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OCX™
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QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
RapidConnect™
SILENT SWITCHER®
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TruTranslation™
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PRODUCT STATUS DEFINITIONS

Definition of Terms

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Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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