

FAIRCHILD
SEMICONDUCTOR™

September 2001
Revised August 2003

FIN1048

3.3V LVDS 4-Bit Flow-Through High Speed Differential Receiver

General Description

This quad receiver is designed for high speed interconnect utilizing Low Voltage Differential Signaling (LVDS) technology. The receiver translates LVDS levels, with a typical differential input threshold of 100mV, to LVTTTL signal levels. LVDS provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed transfer of clock and data.

The FIN1048 can be paired with its companion driver, the FIN1047, or any other LVDS driver.

Features

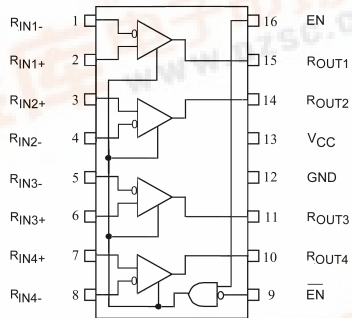
- Greater than 400Mbps data rate
- Flow-through pinout simplifies PCB layout
- 3.3V power supply operation
- 0.4ns maximum differential pulse skew
- 2.5ns maximum propagation delay
- Low power dissipation
- Power-Off protection
- Fail safe protection for open-circuit, shorted and terminated conditions
- Meets or exceeds the TIA/EIA-644 LVDS standard
- Pin compatible with equivalent RS-422 and LVPECL devices
- 16-Lead SOIC and TSSOP packages save space

Ordering Code:

Order Number	Package Number	Package Description
FIN1048M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
FIN1048MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Name	Description
ROUT1, ROUT2, ROUT3, ROUT4	LVTTTL Data Outputs
RIN1+, RIN2+, RIN3+, RIN4+	Non-Inverting LVDS Inputs
RIN1-, RIN2-, RIN3-, RIN4-	Inverting LVDS Inputs
EN	Driver Enable Pin
EN-bar	Inverting Driver Enable Pin
VCC	Power Supply
GND	Ground

Function Table

Inputs				Outputs
EN	EN-bar	RIN+	ROUT-	ROUT
H	L or Open	H	L	H
H	L or Open	L	H	L
H	L or Open	Fail Safe Condition		H
X	H	X	X	Z
L or Open	X	X	X	Z

H = HIGH Logic Level L = LOW Logic Level X = Don't Care
Z = High Impedance Fail Safe = Open, Shorted, Terminated

FIN1048 3.3V LVDS 4-Bit Flow-Through High Speed Differential Receiver



Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_{IN})	-0.5V to +4.6V
DC Input Voltage (V_{OUT})	-0.5V to 6V
DC Output Current (I_O)	16 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C
Max Junction Temperature (T_J)	150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C
ESD (Human Body Model)	≥ 10,000V
ESD (Machine Model)	≥ 450V

Recommended Operating Conditions

Supply Voltage (V_{CC})	3.0V to 3.6V
Magnitude of Differential Voltage ($ V_{ID} $)	100mV to V_{CC}
Common-Mode Input Voltage (V_{IC})	0.05V to 2.35V
Input Voltage (V_{IN})	0 to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. Fairchild does not recommend operation of circuits outside databook specification.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Units
V_{TH}	Differential Input Threshold HIGH	See Figure 1 and Table 1			100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 1 and Table 1	-100			mV
I_{IN}	Input Current	$V_{IN} = 0V$ or V_{CC}			±20	μA
$I_{I(OFF)}$	Power-Off Input Current	$V_{CC} = 0V$, $V_{IN} = 0V$ or 3.6V			±20	μA
V_{IH}	Input High Voltage (\overline{EN} or \overline{EN})		2.0		$V_{CC} + 1.0$	V
V_{IL}	Input Low Voltage (\overline{EN} or \overline{EN})		GND		0.8	V
V_{OH}	Output HIGH Voltage	$I_{OH} = -100 \mu A$	$V_{CC} - 0.2$			V
		$I_{OH} = -8 mA$	2.4			
V_{OL}	Output LOW Voltage	$I_{OH} = 100 \mu A$			0.2	V
		$I_{OL} = 8 mA$			0.5	
I_{OZ}	Disabled Output Leakage Current	$\overline{EN} = 0.8$ and $\overline{EN}^* = 2V$, $V_{OUT} = 3.6V$ or 0V			±20	μA
V_{IK}	Input Clamp Voltage	$I_{IK} = -18 mA$	-1.5			V
I_{CCZ}	Disabled Power Supply Current	Receiver Disabled			5	mA
I_{CC}	Power Supply Current	Receiver Enabled, ($R_{IN+} = 1V$ and $R_{IN-} = 1.4V$) or ($R_{IN+} = 1.4V$ and $R_{IN-} = 1V$)			15	mA
C_{IN}	Input Capacitance			3.5		pF
C_{OUT}	Output Capacitance			6		pF

Note 2: All typical values are at $T_A = 25^\circ C$ and with $V_{CC} = 3.3V$.

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified

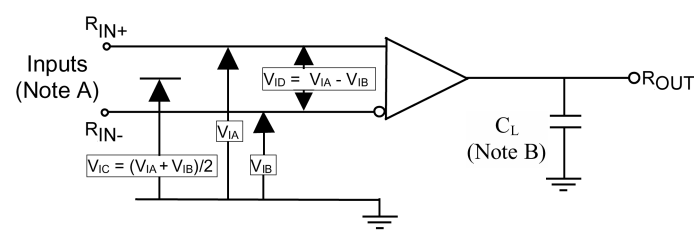
Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Units
t_{PLH}	Propagation Delay LOW-to-HIGH	$ V_{ID} = 400 \text{ mV}, C_L = 10 \text{ pF},$ $R_L = 1 \text{ k}\Omega$ See Figure 1 and Figure 2	1.0		2.5	ns
t_{PHL}	Propagation Delay HIGH-to-LOW		1.0		2.5	ns
t_{TLH}	Output Rise Time (20% to 80%)		0.7		1.2	ns
t_{THL}	Output Fall Time (80% to 20%)		0.7		1.2	ns
$t_{SK(P)}$	Pulse Skew $ t_{PLH} - t_{PHL} $				0.4	ns
$t_{SK(LH)}$	Channel-to-Channel Skew (Note 4)				0.3	ns
$t_{SK(HL)}$	Channel-to-Channel Skew (Note 4)				0.3	ns
$t_{SK(PP)}$	Part-to-Part Skew (Note 5)			1.0	ns	
f_{MAX}	Maximum Operating Frequency (Note 6)	$R_L = 1 \text{ k}\Omega, C_L = 10 \text{ pF},$ see Figure 1 and Figure 2	200	375		MHz
t_{ZH}	LVTTTL Output Enable Time from Z to HIGH	$R_L = 1 \text{ k}\Omega, C_L = 10 \text{ pF},$ See Figure 3			6.0	ns
t_{ZL}	LVTTTL Output Enable Time from Z to LOW				6.0	ns
t_{HZ}	LVTTTL Output Disable Time from HIGH to Z				6.0	ns
t_{LZ}	LVTTTL Output Disable Time from LOW to Z				6.0	ns

Note 3: All typical values are at $T_A = 25^\circ\text{C}$ and with $V_{CC} = 3.3\text{V}$.

Note 4: $t_{SK(LH)}, t_{SK(HL)}$ is the skew between specified outputs of a single device when the outputs have identical loads and are switching in the same direction.

Note 5: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW-to-HIGH or HIGH-to-LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

Note 6: f_{MAX} Criteria: Input $t_R = t_F < 1 \text{ ns}, V_{ID} = 300 \text{ mV}, (1.05\text{V to } 1.35\text{V pp}), 50\%$ duty cycle; Output duty cycle 40% to 60%, $V_{OL} < 0.5\text{V}, V_{OH} > 2.4\text{V}$. All channels switching in phase.



Note A: All differential input pulses have frequency = 10MHz, t_R or $t_F = 1 \text{ ns}$

Note B: C_L includes all probe and jig capacitances

FIGURE 1. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

TABLE 1. Receiver Minimum and Maximum Input Threshold Test Voltages

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	-100	1.2
2.4	2.3	100	2.35
2.3	2.4	-100	2.35
0.1	0	100	0.05
0	0.1	-100	0.05
1.5	0.9	600	1.2
0.9	1.5	-600	1.2
2.4	1.8	600	2.1
1.8	2.4	-600	2.1
0.6	0	600	0.3
0	0.6	-600	0.3

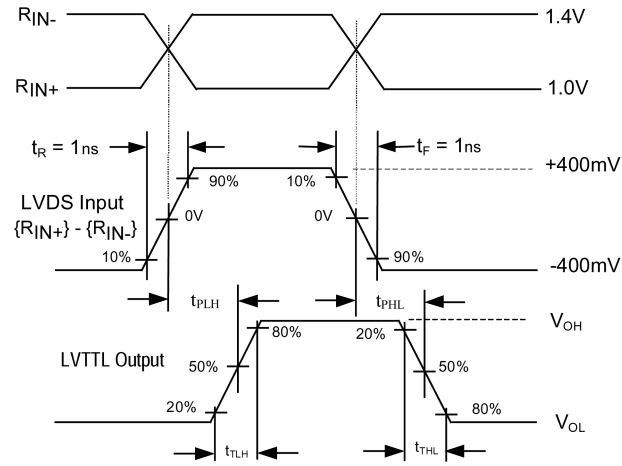
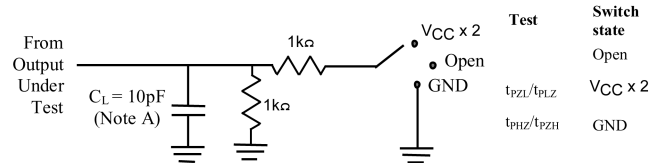


FIGURE 2. LVDS Input to LVTTTL Output AC Waveforms

Test Circuit for LVTTTL Outputs



Voltage Waveforms Enable and Disable Times

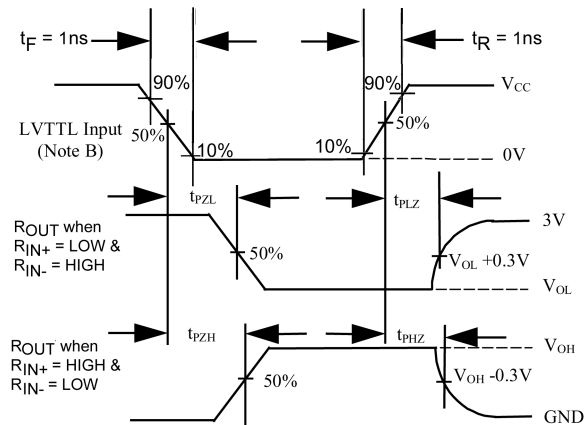
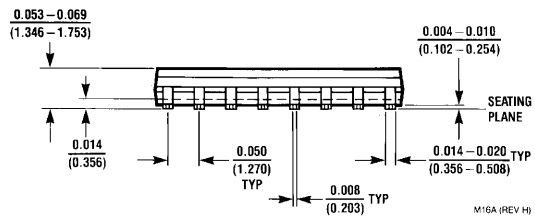
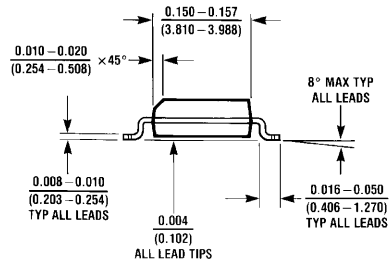
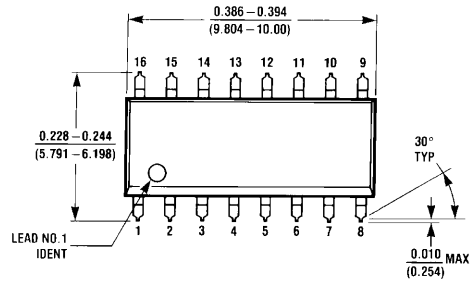


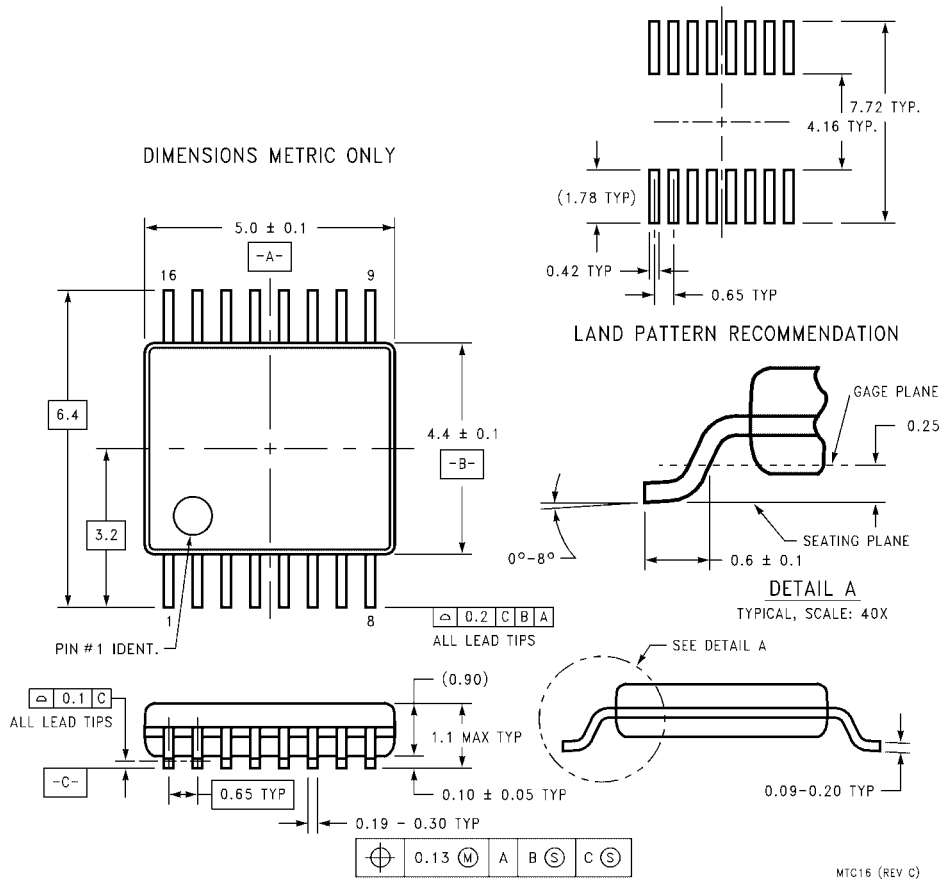
FIGURE 3. LVTTTL Outputs Test Circuit and AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com