FAIRCHILD SEMICONDUCTOR™

February 2002

FM25C041U
4K-Bit SPI™ Interface Serial CMOS EEPROM

General Description

The FM25C041U is a 4K (4,096) bit serial interface CMOS EEPROM (Electrically Erasable Programmable Read-Only Memory). This device fully conforms to the SPI 4-wire protocol which uses Chip Select (/CS), Clock (SCK), Data-in (SI) and Data-out (SO) pins to synchronously control data transfer between the SPI microcontroller and the EEPROM. In addition, the serial interface allows a minimal pin count, packaging designed to simplify PC board layout requirements and offers the designer a variety of low voltage and low power options.

This SPI EEPROM family is designed to work with the 68HC11 or any other SPI-compatible, high-speed microcontroller and offers both hardware (/WP pin) and software ("block write") data protection. For example, entering a 2-bit code into the STATUS REGISTER prevents programming in a selected block of memory and all programming can be inhibited by connecting the /WP pin to V_{SS}; allowing the user to protect the entire array or a selected section. In addition, SPI devices feature a /HOLD pin, which allows a temporary interruption of the datastream into the EEPROM.

Fairchild EEPROMs are designed and tested for applications requiring high endurance, high reliability, and low power consumption for a continuously reliable non-volatile solution for all markets.

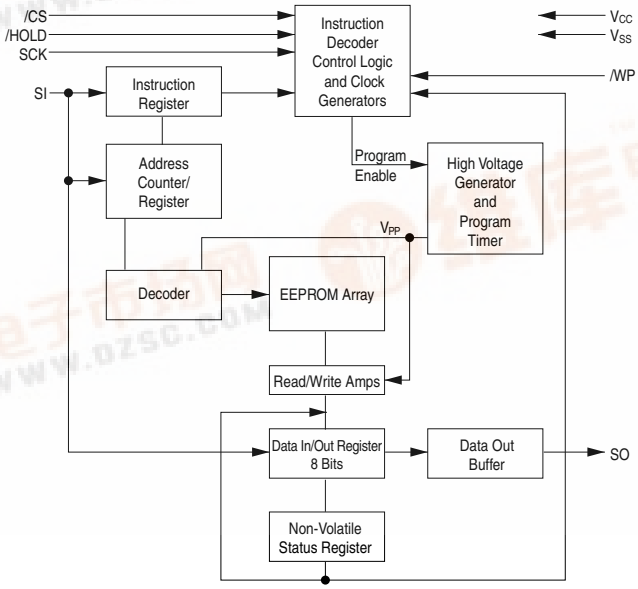
Functions

- **SPI MODE 1 interface**
- 4,096 bits organized as 512 x 8
- Extended 2.7V to 5.5V operating voltage
- 2.1 MHz operation @ 4.5V - 5.5V
- Self-timed programming cycle
- "Programming complete" indicated by STATUS REGISTER polling
- /WP pin and BLOCK WRITE protection

Features

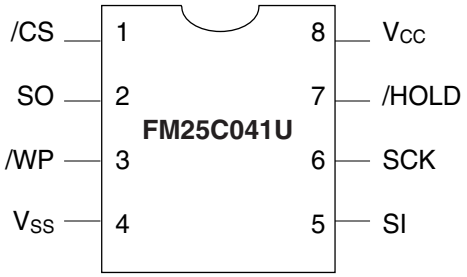
- Sequential read of entire array
- 4 byte "Page write" mode to minimize total write time per byte
- /WP pin and BLOCK WRITE protection to prevent inadvertent programming as well as programming ENABLE and DISABLE opcodes.
- /HOLD pin to suspend data transfer
- Typical 1µA standby current (I_{SB}) for "L" devices and 0.1µA standby current for "LZ" devices.
- Endurance: Up to 1,000,000 data changes
- Data retention greater than 40 years

Block Diagram



Connection Diagram

Dual-In-Line Package (N), SO Package (M8), and TSSOP Package (MT8)



Top View
See Package Number N08E (N), M08A (M8), and MTC08 (MT8)

Pin Names

/CS	Chip Select Input
SO	Serial Data Output
/WP	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
/HOLD	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

FM	25	C	XX	U	LZ	E	XX		Letter	Description
								Package	N	8-pin DIP
									M8	8-pin SO
									MT8	8-pin TSSOP
								Temp. Range	None	0 to 70°C
									V	-40 to +125°C
									E	-40 to +85°C
								Voltage Operating Range	Blank	4.5V to 5.5V
									L	2.7V to 5.5V
									LZ	2.7V to 5.5V and <1μA Standby Current
									Ultralite	CS100UL Process
								Density/Mode	041	4K, mode 1
									C	CMOS technology
								Interface	25	SPI
									FM	**Fairchild Nonvolatile Memory Prefix**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
FM25C041U	0°C to +70°C
FM25C041UE	-40°C to +85°C
FM25C041UV	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	/CS = V_{IL}		3	mA
I_{CCSB}	Standby Current	/CS = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	CMOS Input High Voltage		0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.1	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	190		ns
t_{CLL}	Clock Low Time	(Note 2)	190		ns
t_{CSH}	Min /CS High Time	(Note 3)	240		ns
t_{CSS}	/CS Setup Time		240		ns
t_{DIS}	Data Setup Time		100		ns
t_{HDS}	/HOLD Setup Time		90		ns
t_{CSN}	/CS Hold Time		240		ns
t_{DIN}	Data Hold Time		100		ns
t_{HDN}	/HOLD Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		240	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	/HOLD to Output Low Z			100	ns
t_{DF}	Output Disable Time	C_L = 200 pF		240	ns
t_{HZ}	/HOLD to Output High Z			100	ns
t_{WP}	Write Cycle Time	1–16 Bytes		10	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, for a f_{OP} of 2.1MHz, the period equals 476ns. In this case if t C_{LH} = is set to 190ns, then t_{CLL} must be set to a minimum of 286ns.

Note 3: /CS must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
FM25C041UL/LZ	0°C to +70°C
FM25C041ULE/LZE	-40°C to +85°C
FM25C041ULV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V (unless otherwise specified)

				25C041UL/LE 25C041ULZ/ZE		25C041ULV		
Symbol	**Parameter**	**Part**	**Conditions**	**Min.**	**Max.**	**Min**	**Max**	**Units**
I_{CC}	Operating Current		/CS = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	/CS = V_{CC}		10 1		10 N/A	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	V_{CC} * 0.3	-0.3	V_{CC} * 0.3	V
V_{IH}	Input High Voltage			V_{CC} * 0.7	V_{CC} + 0.3	V_{CC} * 0.7	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 0.8 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				1.0		1.0	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	410		410		ns
t_{CLL}	Clock Low Time		(Note 6)	410		410		ns
t_{CSH}	Min. /CS High Time		(Note 7)	500		500		ns
t_{CSS}	/CS Setup Time			500		500		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	/HOLD Setup Time			240		240		ns
t_{CSN}	/CS Hold Time			500		500		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	/HOLD Hold Time			240		240		ns
t_{PD}	Output Delay		C_L = 200 pF		500		500	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	/HOLD Output Low Z				240		240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		500		500	ns
t_{HZ}	/HOLD to Output Hi Z				240		240	ns
t_{WP}	Write Cycle Time		1-16 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 6: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, for a f_{OP} of 1MHz, the period equals 1000ns. In this case if t_{CLH} = is set to 410ns, then t_{CLL} must be set to a minimum of 590ns.

Note 7: /CS must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

FIGURE 1. Synchronous Data Timing Diagram

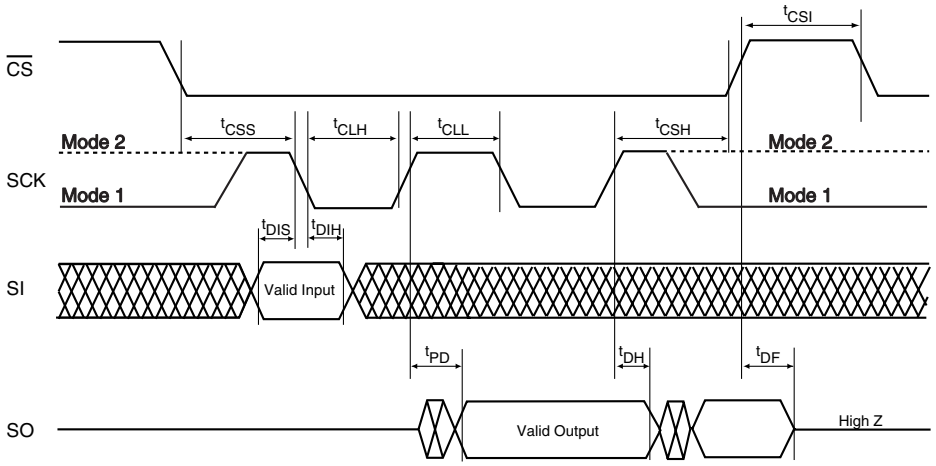


FIGURE 2. SPI Protocol

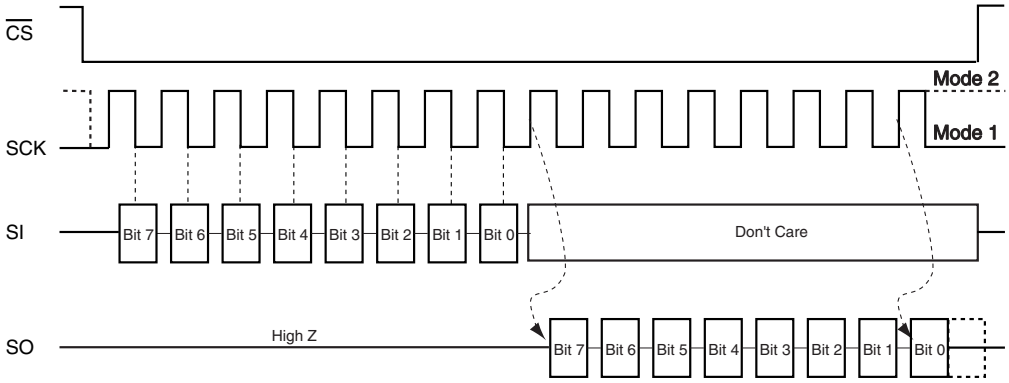
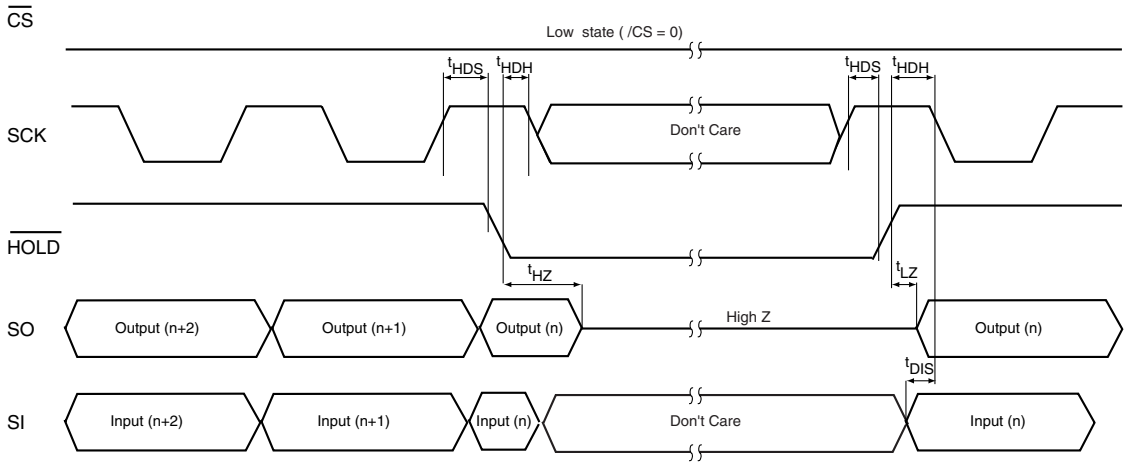


FIGURE 3. HOLD Timing



Pin Description

Chip Select (/CS)

This is an active low input pin to the EEPROM and is generated by a master that is controlling the EEPROM. A low level on this pin selects the EEPROM and a high level deselects the EEPROM. All serial communications with the EEPROM is enabled only when this pin is held low.

Serial Clock (SCK)

This is an input pin to the EEPROM and is generated by the master that is controlling the EEPROM. This is a clock signal that synchronizes the communication between a master and the EEPROM. All input information (SI) to the EEPROM is latched on the falling edge of this clock input, while output data (SO) from the EEPROM is driven after the rising edge of this clock input.

Serial Input (SI)

This is an input pin to the EEPROM and is generated by the master that is controlling the EEPROM. The master transfers Input information (Instruction Opcodes, Array addresses and Data) serially via this pin into the EEPROM. This Input information is latched on the falling edge of the SCK.

Serial Output (SO)

This is an output pin from the EEPROM and is used to transfer Output data via this pin to the controlling master. Output data is serially shifted out on this pin after the rising edge of the SCK.

Hold (/HOLD)

This is an active low input pin to the EEPROM and is generated by the master that is controlling the EEPROM. When driven low, this pin suspends any current communication with the EEPROM. The suspended communication can be resumed by driving this pin high. This feature eliminates the need to re-transmit the entire sequence by allowing the master to resume the communication from where it was left off. This pin should be tied high if this feature is not used. Refer **Hold Function** description for additional details.

Write Protect (/WP)

This is an active low input pin to the EEPROM. This pin allows enabling and disabling of writes to memory array and status register of the EEPROM. When this pin is held low, writes to the memory array and status register are disabled. When this pin is held high, writes to the memory array and status register are enabled. Status of this pin does not affect operations other than array write and status register write. /WP signal going low at any time will inhibit programming, except when an internal write has already begun. If an internal write cycle has already begun, /WP signal going low will have no effect on the write. Refer Table1 for Write Protection matrix.

Functional Description

The Serial Peripheral Interface (SPI) of FM25C041U consists of an 8-bit Instruction register to decode a specific instruction to be executed. Six different instructions (Opcodes) are incorporated on FM25C041U for various operations. Table2 lists the instructions set and the format for proper operation. All Opcodes, Array addresses and Data are transferred in “MSB first-LSB last” fashion. Detailed information is provided under individual instruction descriptions.

TABLE 2. Instruction Set

Instruction Name	Instruction Opcode	Operation
WREN	00000110	Write Enabled
WRDI	00000100	Write Disabled
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	0000A011	Read Data from Memory Array
WRITE	0000A010	Write Data to Memory Array

Note: As the FM25C041U requires 9 address bits (4,096 ÷ 8 = 512 bytes = 2^9), the 9th bit (for R/W instructions) is inputted in the Instruction Set Byte in bit I_3. **This convention only applies to 4K SPI protocol.**

In addition to the Instruction register, FM25C041U also contains an 8-bit Status register that can be accessed by RDSR and WRSR instructions. Only the least significant (LSB) 4 bits are defined at present and the most significant (MSB) 4 bits are undefined (don’t care). The LSB 4 bits define Block Write Protection levels (BP1and BP0), Write-enable status (WEN) and Busy/Rdy status (/RDY) of the EEPROM. Table 3 illustrates the format:

TABLE 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{\text{RDY}}$

Refer RDSR and WRSR instruction descriptions for additional information on Status register operations.

Table1. Write Protection Matrix

/WP Pin	WEN Bit	Status Register	Protected Blocks (by BP1-BP0)	Unprotected Blocks
Low	X	Write Protected	Write Protected	Write Protected
High	0	Write Protected	Write Protected	Write Protected
High	1	Write Allowed	Write Protected	Write Allowed

Functional Description (Continued)

SPI communication

As mentioned before, serial communication with the EEPROM is enabled when the /CS pin is held low and the /HOLD pin is held high. Input data (Instruction Opcodes, Array addresses and Data) on the SI pin is latched in on the falling edges of SCK clock signal, starting from the first falling edge after the /CS pin goes low. During the time the SI data is input into the EEPROM, the SO pin remains in high impedance state. If the intended instruction is of read nature (Array read and Status register read), then data from the EEPROM is driven out actively on the SO pin from every rising edge of the SCK after the last input data (SI) is latched in. During the time the SO data is output from the EEPROM, the data on the SI pin is ignored. *Figure 2* illustrates the above. Refer *Figure 1* for timing information.

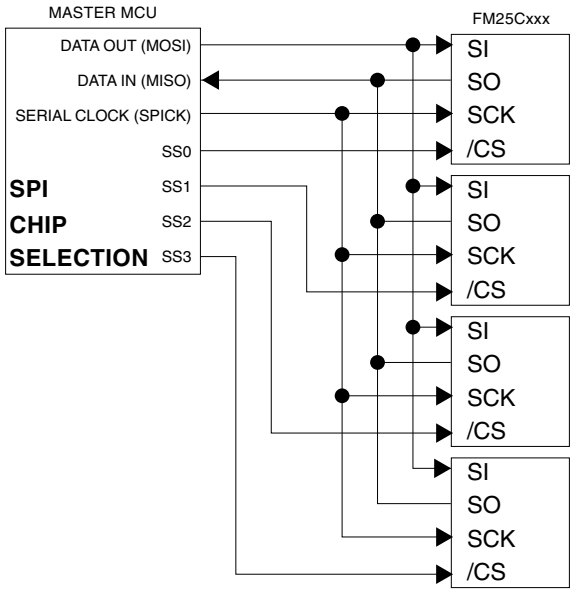
HOLD function

An active communication with the EEPROM can be temporarily suspended by bringing the /HOLD pin low when a EEPROM is selected (/CS pin should be low) and a serial sequence with the EEPROM is currently underway. To suspend the communication, /HOLD pin must be driven low while SCK is high, otherwise the Hold function will not be invoked until the next SCK low to high transition. The EEPROM must remain selected during this sequence. Transitions on the SCK and SI pins are ignored during the time the part is suspended and the SO pin will be in high impedance state. Releasing the /HOLD pin back to high state will allow the operation to resume from the point it was suspended. /HOLD pin must be driven high while the SCK pin is high, otherwise serial communication will not resume until the next SCK low to high transition. Asserting a low on the /HOLD pin at any time will tri-state the SO pin. *Figure 3* illustrates Hold timing.

System Configuration

When multiple SPI peripherals (for e.g. EEPROMs) are present on the bus, the SI, SO and the SCK signals can be tied together. *Figure* 4 illustrates a typical system configuration with respect to /CS, SCK, SI and SO pins.

FIGURE 4. System Configuration



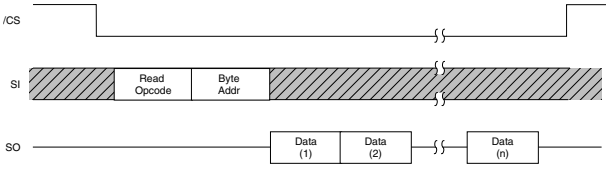
SPI Modes 1 and 2

FM25C041U supports both MODE 1 and MODE 2 of operations. The difference between MODE 1 and MODE 2 is determined by the state of the SCK clock signal when a SPI cycle starts (when / CS is driven low) as well as when the SPI cycle ends (when /CS is driven high). Under MODE 2 of operation, the SCK signal is held low both at the start and at the end of a SPI cycle. Under Mode 1 of operation, the SCK signal is held high both at the start and at the end of a SPI cycle. However in both of these two modes, the input data (SI) is sampled (latched in) at the falling edge of the SCK clock signal and the output data (SO) is driven after the rising edge of the SCK clock signal. See *Figure* 1 and *Figure* 2.

READ SEQUENCE (READ)

Reading the memory via the serial SPI link requires the following sequence. The /CS pin is pulled low to select the EEPROM. The READ opcode is transmitted on the SI pin followed by the byte address (A7–A0) to be read. After this is done, data on the SI pin becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO pin. If only one byte is to be read, the /CS pin can be pulled back to the high level. It is possible to continue the READ sequence as the byte address is automatically incremented and data will continue to be shifted out as clock pulses are continuously applied. When the end of memory array is reached (last byte location), the address counter rolls over to the start of memory array (first byte location) allowing the entire memory to be read in one continuous READ cycle. See *Figure* 5.

FIGURE 5. Read Sequence



READ STATUS REGISTER (RDSR):

The Read Status Register (RDSR) instruction provides read access to the status register. As mentioned before, of the 8bits of data, only the LSB 4bits are valid and they indicate Block Protection information (BP1 and BP0), Write Enable status (WEN) and Busy/Ready status (/RDY) of the EEPROM. MSB 4bits of are invalid (Don't cares) Following is the format of RDSR data:

TABLE 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

Bit3 (BP1) and Bit2 (BP0) together indicate Block write protection previously set on the EEPROM. Refer Table 2.

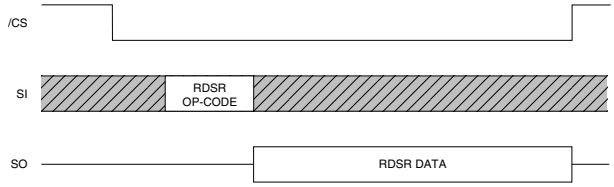
Bit1 (WEN) indicates the Write enable status of the EEPROM. This bit is a read-only bit and is read by executing RDSR instruction. If this bit is "1" then the EEPROM is write enabled. If this bit is "0" then the EEPROM is write disabled.

Bit0 (/RDY) indicates the Busy/Ready status of the EEPROM. This bit is a read-only bit and is read by executing RDSR instruction. If this bit is "1" then the EEPROM is busy doing a program cycle. If this bit is "0" then the EEPROM is ready.

Note that if a RDSR instruction is executed when an internal programming cycle is in progress, only the /RDY bit is valid. All other bits are don't cares.

The RDSR command requires the following sequence. The /CS pin is pulled low to select the EEPROM and then the RDSR opcode is transmitted on the SI pin. After this is done, data on the SI pin becomes don't care. The data from the Status Register is then shifted out on the SO pin starting with D7 bit first and D0 last. See *Figure 6.*

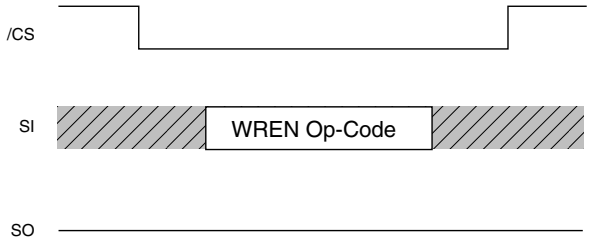
FIGURE 6. Read Status Register



WRITE ENABLE (WREN):

When V_{CC} is applied to the EEPROM, it "powers up" in a write-disabled state. Therefore, all programming modes (Write to memory array and Status register), must be preceded by a WRITE ENABLE (WREN) instruction. See *Figure* 7.

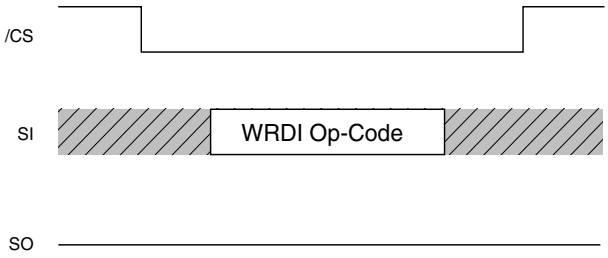
FIGURE 7. Write Enable



WRITE DISABLE (WRDI):

Executing this instruction disables all programming modes (Write to memory array and Status register), preventing the EEPROM from accidental writes. Once WRDI instruction is executed, WREN instruction should be executed to re-enable all programming modes. See *Figure* 8.

FIGURE 8. Write Disable



WRITE SEQUENCE (WRITE):

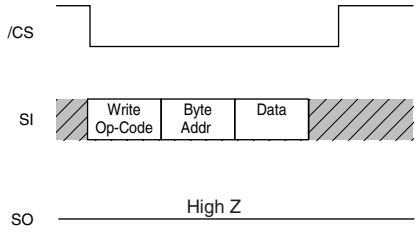
Write to the array is enabled only when /WP pin is held high and the EEPROM is write enabled previously (via WREN instruction). Also, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 4.

TABLE 4. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	180-1FF
2	1	0	100-1FF
3	1	1	000-1FF

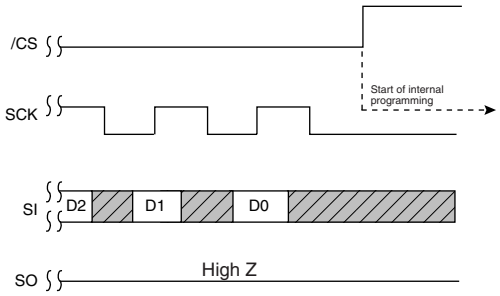
A WRITE command requires the following sequence. The /CS pin is pulled low to select the EEPROM, then the WRITE opcode is transmitted on the SI pin followed by the byte address (A7-A0) and followed by the data (D7-D0) to be written. See *Figure 9*.

FIGURE 9. Byte Write



Internally, the programming will start after the /CS pin is brought back to a high level. Note that the LOW to HIGH transition of the /CS pin must occur during the SCK low time immediately after clocking in the D0 data bit. See *Figure* 10.

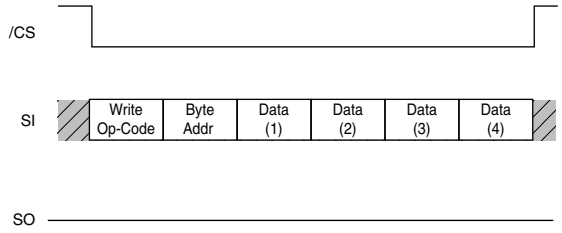
FIGURE 10. Start of Programming



Programming status (Busy/Ready) of the EEPROM can be determined by executing a READ STATUS REGISTER (RDSR) instruction after a write command. Upon executing the RDSR instruction, if Bit 0 of the RDSR data is "1", it indicates the WRITE cycle is still in progress. If it is "0" then the WRITE cycle has ended. Note that while the internal programming is still in progress (Bit 0 = 1), only the RDSR instruction is enabled. It is recommended that no other instruction be issued till the internal programming is complete.

The FM25C041U is also capable of a 4 byte PAGE WRITE operation. Page write is performed similar to byte write operation described above. During a Page write operation, after the first byte of data, additional bytes (up to 3 bytes) can be input, before bringing the /CS pin high to start the programming. After receipt of each byte of data, the EEPROM internally increments the two low order address bits (A1-A0) by one. The high order address bits (A8-A2) will remain constant. If the master should transmit more than 4 bytes of data, the address counter (A1-A0) will "roll over" and the previously loaded data will be reloaded. See *Figure* 11.

FIGURE 11. Page Write



At the completion of a write cycle the EEPROM is automatically returned to the write disabled state. Note that if the EEPROM is not write enabled (WEN=0) before issuing the WRITE instruction, the EEPROM will ignore the WRITE instruction and return to the standby state when /CS is brought high.

WRITE STATUS REGISTER (WRSR):

The Write Status Register (WRSR) instruction provides write access to the status register. This instruction is used to set Block Write protection to a portion of the array as defined under Table 4. During a WRSR instruction only Bit3 (BP1) and Bit2 (BP0) can be written with valid information while other bits are ignored. Following is the format of WRSR data:

Status Register Write Data

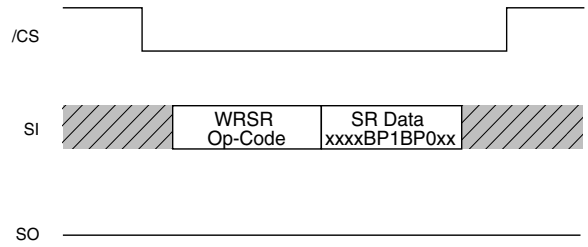
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	X	X

X = Don't Care

Note that the first four bits are don't care bits followed by BP1 and BP0 and two more don't care bits.

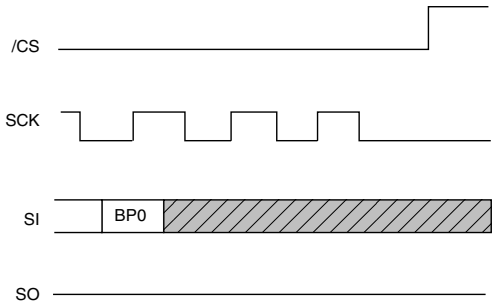
WRSR instruction is enabled only when /WP pin is held high and the EEPROM is write enabled previously (via WREN instruction). WRSR command requires the following sequence. The /CS pin is pulled low to select the EEPROM and then the WRSR opcode is transmitted on the SI pin followed by the data to be programmed. See *Figure 12.*

FIGURE 12. Write Status Register



Programming will start after the /CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the /CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See *Figure 13.*

FIGURE 13. Start WRSR Condition

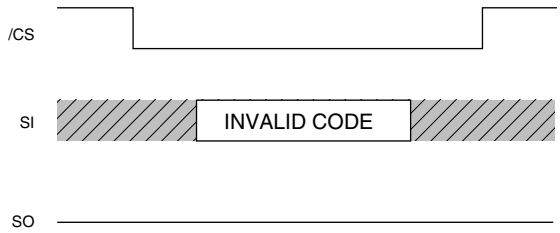


At the completion of this instruction the EEPROM is automatically returned to write disabled state.

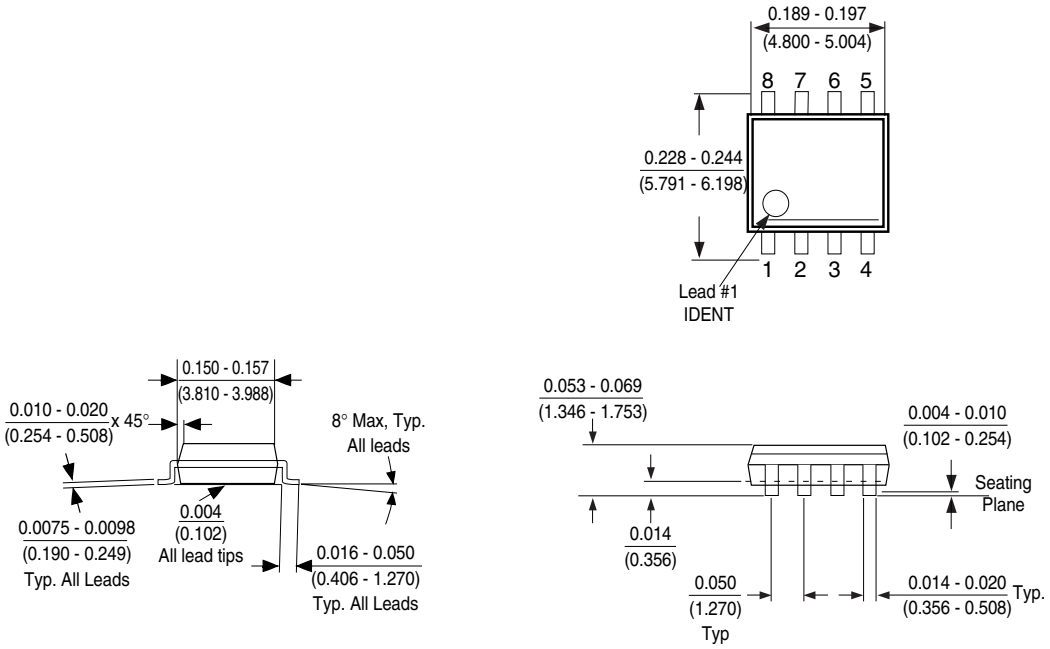
INVALID OPCODE

If an invalid code is received, then no data is shifted into the EEPROM, and the SO data output pin remains high impedance state until a new /CS falling edge reinitializes the serial communication. See *Figure* 14.

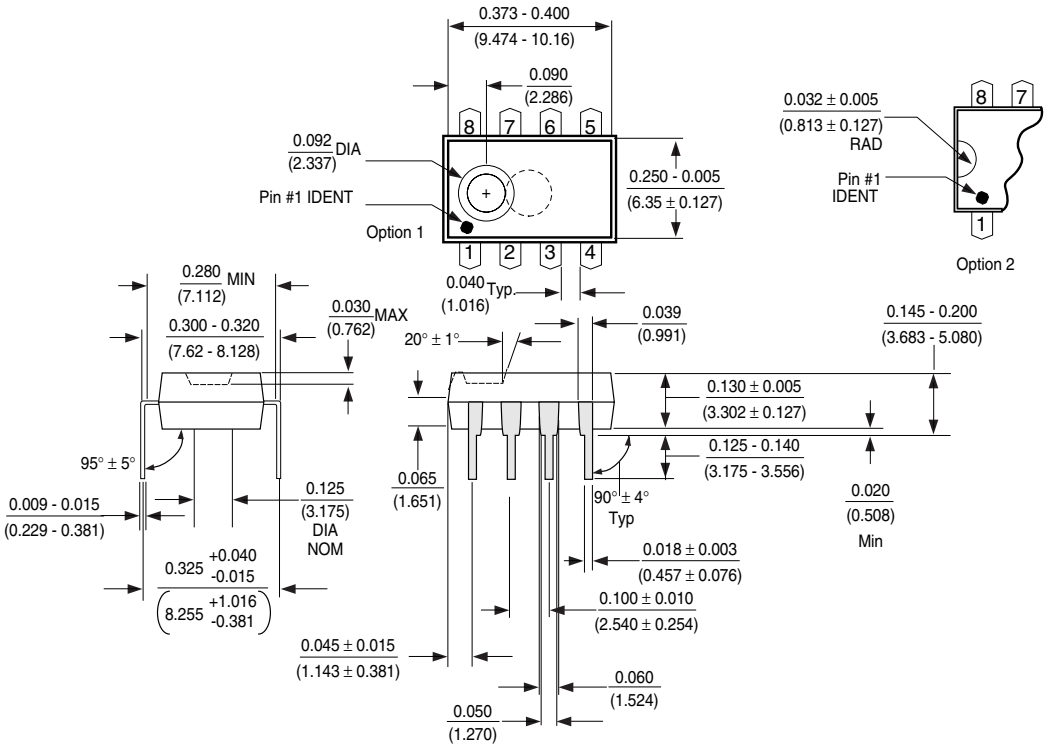
FIGURE 14. Invalid Op-Code



Physical Dimensions inches (millimeters) unless otherwise noted

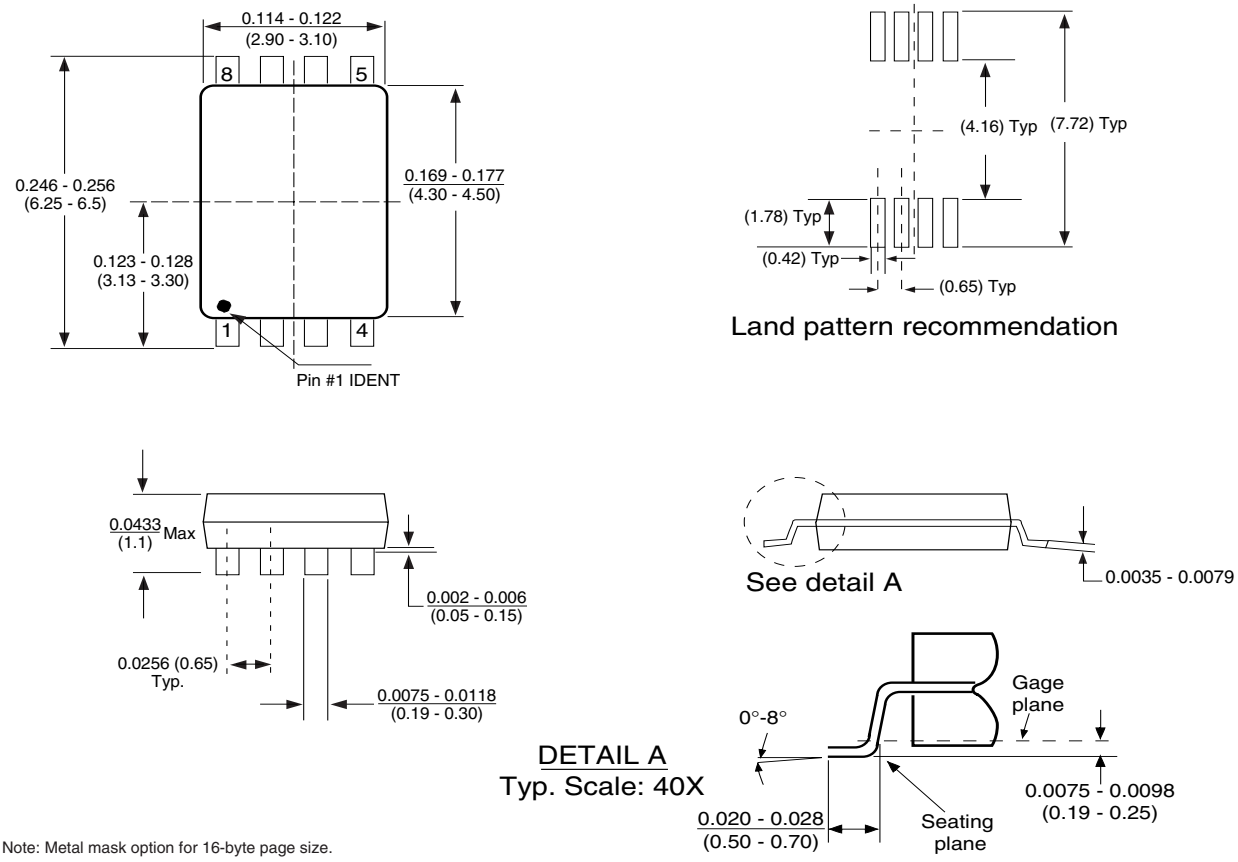


Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Physical Dimensions inches (millimeters) unless otherwise noted



Note: Metal mask option for 16-byte page size.

Notes: Unless otherwise specified

1. Reference JEDEC registration MO153. Variation AA. Dated 7/93

8-Pin Molded TSSOP, JEDEC (MT8)
Package Number MTC08

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