Preliminary Data Sheet, May 2001

FOA2322A

3.2 Gbit/s Laser Driver IC for Telecom and Datacom Applications

ICs for Communications

Infineon technologies

Never stop thinking.

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FOA2322A

1 Overview

1.1 Features

- Data rate up to 3.2 Gbit/s
- Supply range from +3.0 V to +5.5 V
- Modulation current adjustable up to 75 mA
- Bias current adjustable up to 80 mA
- Choice between temperature compensation and integrated Two-Loop-Control of bias and modulation current
- Integrated laser supervisor
- Monitor output for optical output power

1.2 Applications

- Fiber optics telecom and data communication systems
- SDH / SONET, Fiber Channel, Gigabit Ethernet

1.3 Technology

- Bicmos B6HFC

1.4 General

This document defines the ratings and characteristics of a laser driver circuit dedicated for applications within telecom and datacom modules with respect to various transmission standards and laser safety requirements. A block diagram of this circuit is shown in **Figure 1**.

Modulation Control / Modulator / Input Stage

The modulator is capable of driving modulation currents up to 75 mA. There are two modes for adjusting the modulation current:

Mode 1: The modulation current is adjusted by an external resistor (R_{MOD}). The IC has an internal temperature compensation circuit for compensating the temperature characteristic of laser diode slope efficiency. With the external resistor (R_{TC}) the modulation current temperature coefficient is adjustable. The temperature input itself is derived from chip junction temperature.

Mode 2: The modulation current is controlled by using a low frequency pilot signal. The controller cutoff frequency is adjustable by external capacitor (C_{MOD}). Mode 2 is suitable for data rates 1.25 Gbit/s (depending on laser diode).

There is an option for using data input latch.

Input Signal Monitor

An input signal monitor circuit delivers a logic signal HWA and an internal signal which is used for laser disabling if data input is constantly high or low.

Bias Control / Bias Generator

The bias controller controls the LD optical output power by adjusting the bias current. The controller cutoff frequency is adjustable by external capacitor (C_{BIAS}). A min. cutoff frequency is integrated. The laser bias current will start at < 500 µA after laser enable.

Laser Supervisor / V_{CC} Supervisor

The laser supervisor circuit monitors the laser output power by the means of monitor diode feedback. The voltage generated by monitor diode circuit is compared to a reference. If the input voltage deviates more than ±2 dB (optical power ±1 dB) from this reference the laser diode is switched off and a fault indication is generated. The V_{CC} supervisor monitors the circuit power supply and switches off the laser if the V_{CC} level is below the reset threshold. It is keeping the laser output down for the adjusted delay time (power on delay) after V_{CC} has risen above the V_{CC} reset threshold.

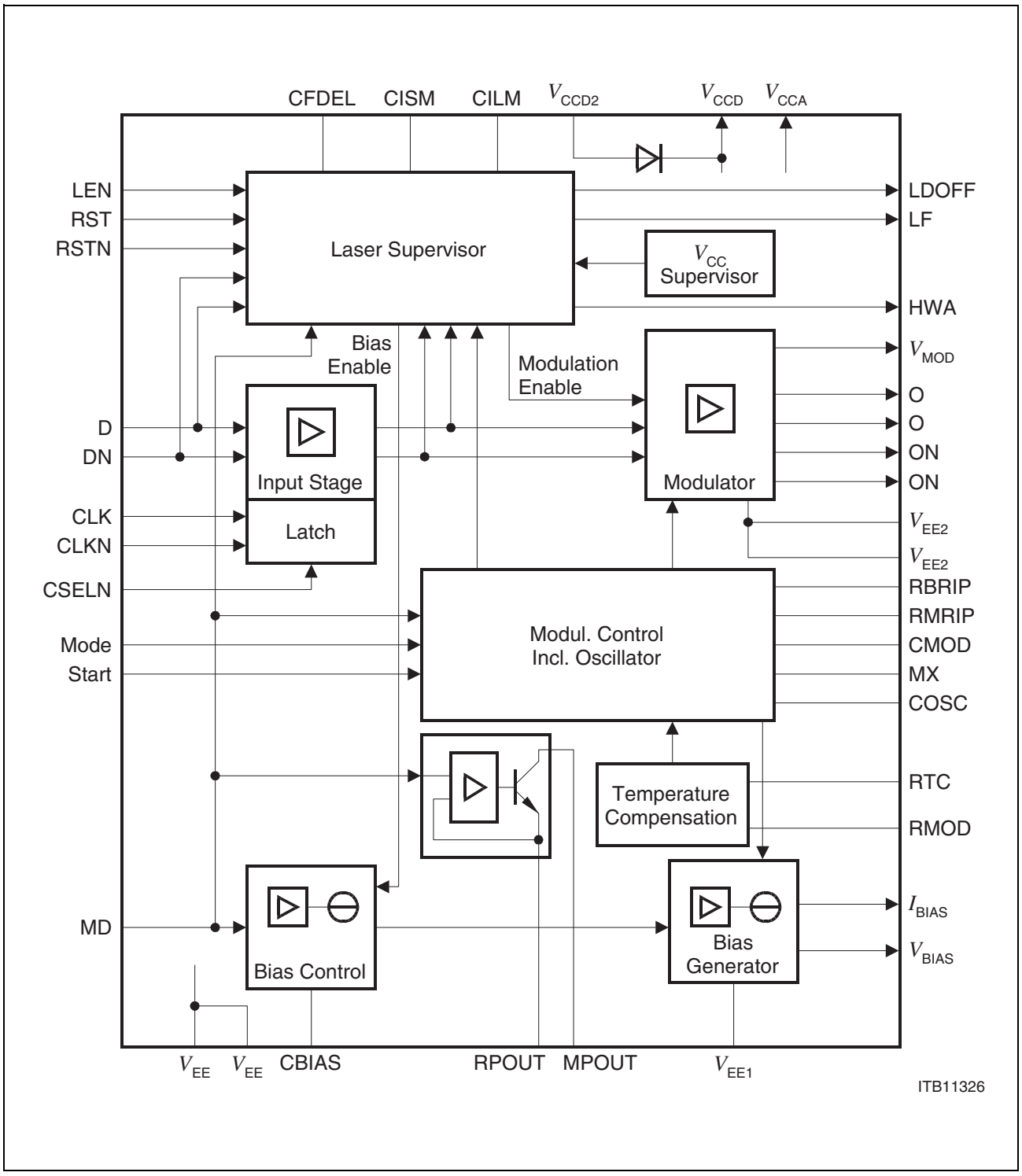

Figure 1 General Circuit Block Diagram

– Number of pins: 42
– IC available as die

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings which may not be exceeded to the device without causing permanent damage or degradation. Exposure to these values for extended periods may effect device reliability. If the device is operated beyond the range of Operating Conditions and Characteristics functionality is not guaranteed. All voltages given within this data sheet are referred to V_{EE} if not otherwise mentioned.

Table 1 Absolute Maximum Ratings

Parameter	Sym-bol	Limit Values		Unit	Condi-tions
		min.	max.		
Supply Voltage		-0.3	6	V	–
Output Voltage at O, ON		V_{CC} - 2.6	V_{CC} + 0.3	V	1)
Output Voltage at MPOUT		-0.3	V_{CC} + 0.3	V	1)2)
Output Voltage at Logic Output LF, HWA		-0.3	V_{CC} + 0.3	V	1)
Output Voltage at IBIAS		-0.3	V_{CC} + 0.3	V	1)2)
Input Voltage at Logic Inputs LEN, RST, RSTN, CSELN		-0.3	V_{CC} + 0.3	V	1)
Differential Data Input Voltage $\|V_D - V_{DN}\|$		–	2.5	V	–
Differential Data Input Voltage $\|V_{CLK} - V_{CLKN}\|$		–	2.5	V	–
Sink Current at Logic Output LF, HWA		–	5	mA	–
Source Current at LDOFF		-4	–	mA	–
Source Current at RPOUT		-2	–	mA	–
Modulation Current at O, ON (both Outputs)		–	80	mA	–
Bias Current at IBIAS		–	95	mA	–
Modulation Control Sink Current at VMOD (Input Current for Current Mirror 1:10)		–	9.6	mA	–
Bias Control Sink Current at VBIAS (Input Current for Current Mirror 1:25)		–	4.8	mA	–
Modulation Current Adjust Resistor R_{MOD}		800	–	Ω	–

Table 1 Absolute Maximum Ratings (cont'd)

Parameter	Sym-bol	Limit Values		Unit	Condi-tions
		min.	max.		
Modulation Temperature Coefficient Resistor R_{TC}		50	–	Ω	–
Junction Temperature		-40	125	°C	–
Storage Temperature		-55	150	°C	–
Relative Humidity (non-condensing)		–	95	%	–
Electrostatic Discharge Voltage Capability		–	1	kV	–

1) Maximum voltage is 6 V.

2) For applications with V_{CC} + 5 V (please refer to **Figure 13**).

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2.2 General Operating Conditions

Under the below defined operating conditions all specified characteristics will be met unless otherwise noted.

Table 2 General Operating Conditions

Parameter	Sym-bol	Limit Values		Unit	Condi-tions
		min.	max.		
Environmental					
Junction Temperature		-40	125	°C	1)
		-40	110		2)
Relative Humidity (non-condensing)		–	95	%	–
Supply Voltage					
V_{CC} Range		3	5.5	V	3)

1) For modulation current $I_{OH} \leq 50$ mA

2) For modulation current 50 mA < $I_{OH} \leq 75$ mA

3) Valid for V_{CCA} and V_{CCD}; $V_{CCA} \geq V_{CCD}$

2.3 Characteristics and Operating Conditions

Table 3 Characteristics and Operating Conditions

SP	Parameter	Sym-bol	Limit Values			Unit	Condi-tion
			min.	typ.	max.		
Modulator / Modulation Control							
1	Data Transmission Rate	DR	0	–	2.5	Gbit/s	1)
2	Supply Current	I_{CC}	–	30	63	mA	2)3)
3	Modulation Current High at O/ON for V_{CC} = 3.3 V for V_{CC} = 5 V	I_{OH} - I_{OL}	 5 5	 – –	 65 75	mA	4)5)
4	Modulation Current Low at O/ON	I_{OL}	0	–	2	mA	6) Offset
5	Modulation Current at Laser Shut Down	I_{OSD}	0	–	200	µA	7)
6	O, ON Output Voltage Range for V_{CC} = 3.3 V for V_{CC} = 5 V	V_O, V_{ON}	 V_{CC} - 1.65 V V_{CC} - 2.0 V	 – –	 V_{CC} V_{CC}	V	8)
7	Modulation Current Adjust Resistor Range (MOD-Resistor)	R_{MOD}	800	–	Open Input	Ω	9)10)
8	Modulation Temperature Coefficient Resistor Range	R_{TC}	50	–	Open Input	Ω	9)11)
Serial Data/Clock Input							
9	Data Input Voltage High	V_{IHD}	–	–	V_{CCD}	V	–
10	Data Input Voltage Low for V_{CCD} = 3.3 V for V_{CCD} = 5 V	V_{ILD}	 1.0 2.2	 – –	 – –	V	–
11	Data Input Voltage Swing	$\|V_D$ - $V_{DN}\|$	250	–	1600	mV	–
12	Clock Input Voltage High	V_{IHCLK}	–	–	V_{CCD} - 0.65	V	–

Table 3 Characteristics and Operating Conditions (cont'd)

SP	Parameter	Sym-bol	Limit Values			Unit	Condi-tion
			min.	typ.	max.		
13	Clock Input Voltage Low for V_{CCD} = 3.3 V for V_{CCD} = 5 V	V_{ILCLK}	 1.0 2	 – –	 – –	V	–
14	Clock Input Voltage Swing	$\|V_{CLK} - V_{CLKN}\|$	250	–	1100	mV	–
15	Bias Voltage at D/DN	V_{BBD}	–	V_{CCD} - 1.0	–	V	12)
16	Bias Voltage at CLK/CLKN	V_{BBC}	–	V_{CCD} - 1.3	–	V	12)
17	Differential Data/Clock Input Termination	R_{IN}	80	100	120	Ω	12)13)
19	Input Capacitance D/DN/CLK/CLKN	C_{IN}	–	–	0.6	pF	–
20	Setup Time (Data/Clock)	t_{SETUP}	–	20	–	ps	–
21	Hold Time (Data/Clock)	t_{HOLD}	–	20	–	ps	–
22	Eye Opening at 2.5 Gbit/s (w. Latch)	t_{EO}	–	360	–	ps	–
	Input Signal Monitor (ISM)						
23	Internal ISM cutoff frequency	f_{ISM}	165	238	372	kHz	14)
24	Cutoff frequency of ISM with external C_{ISM}	f_{ISM}	(6.1 µs + 84 kΩ × C_{ISM})$^{-1}$	(4.2 µs + 70 kΩ × C_{ISM})$^{-1}$	(2.7 µs + 56 kΩ × C_{ISM})$^{-1}$		14)15)
25	Internal ILM cutoff frequency	f_{ILM}	–	160	–	kHz	14)
26	Cutoff frequency of ILM with external C_{ILM} = 1nF	f_{ILM}	–	73	–	kHz	14)15)
27	Duty Cycle for laser enable		25	–	75	%	–
28	Duty Cycle for laser disable		0	–	5	%	Input low
29	Duty Cycle for laser disable		95	–	100	%	Input high

Table 3 Characteristics and Operating Conditions (cont'd)

SP	Parameter	Sym-bol	Limit Values			Unit	Condi-tion
			min.	typ.	max.		
Laser Power Control							
30	Bias Current	$I_{IBIASmax}$	0	–	80	mA	–
31	Start Bias Current	$I_{IBIASmin}$	–	–	500	µA	–
32	Bias Current at Laser Shut Down	$I_{IBIASSD}$	–	–	500	µA	–
33	Output Voltage Range IBIAS	V_{IBIAS}	0.5	–	V_{CC}	V	–
34	Power Monitor Current	I_{MPOUT}	0	$\frac{V_{MD}}{R_{POUT}}$	1	mA	16)
35	Output Voltage Range MPOUT	V_{MPOUT}	V_{RPOUT} + 0.5	–	V_{CC}	V	–
36	Resistor Range RPOUT	R_{POUT}	2.4	–	Open Input	kΩ	–
37	Output Voltage Range RPOUT	V_{RPOUT}	0	V_{MD}	V_{CC} - 1.2	V	–
38	Internal cutoff frequency of bias controller	f_{BIAS}	23	37	62	kHz	17)
39	Cutoff frequency of bias controller with external C_{BIAS}	f_{BIAS}	(44 µs + 306 kΩ × C_{BIAS})$^{-1}$	(27 µs + 204 kΩ × C_{BIAS})$^{-1}$	(16 µs + 131 kΩ × C_{BIAS})$^{-1}$		15)17)
40	Conversion gain of bias generator	G_{BIAS}	–	100	–	mA/V	–
Laser Supervising Circuit							
41	MD Failure Voltage High		–	V_{MDnom} + 1.5 dB	V_{MDnom} + 2 dB		18)
42	MD Failure Voltage Low		V_{MDnom} - 2 dB	V_{MDnom} - 1.55 dB	–		18)
43	MD Range without Failure Recognition		V_{MDnom} - 1.2 dB	–	V_{MDnom} + 1.2 dB	V	19)
44	Internal Failure Recognition Time	t_{FDEL}	38	60	86	µs	17)20)
45	Additional Failure Recognition Time by external C_{FDEL}	t_{FDEL}	C_{FDEL} × 0.7 µs/pF	C_{FDEL} × 1.0 µs/pF	C_{FDEL} × 1.3 µs/pF		15)17)20)

Table 3 Characteristics and Operating Conditions (cont'd)

SP	Parameter	Sym-bol	Limit Values			Unit	Condi-tion
			min.	typ.	max.		
46	Shut Off Time after LF transition or Laser Disable	t_{LDdis}	0	–	3	µs	21)
47	V_{CC} Reset Threshold for Laser Enable/Disable		2.5	2.75	2.99	V	22)
48	Internal Power On Delay	t_{PDEL}	213	333	480	µs	23)
49	Additional Power On Delay by external C_{OSC}	t_{PDEL}	$64 \times C_{OSC}$ $\times$ 138 kΩ	$64 \times C_{OSC}$ $\times$ 173 kΩ	$64 \times C_{OSC}$ $\times$ 208 kΩ		15)23)
50	LDOFF low Output Current		1.5	–	4	mA	sink current
51	LDOFF high Output Current		–	–	2	µA	sink current
52	LDOFF high Output Voltage		V_{CC} - 0.1	–	–	V	–
53	LDOFF low Output Voltage		V_{CC} - 2.0	–	V_{CC} - 1.2	V	without external load
	Reference Voltage						
54	MD Reference Value	V_{MDR}	1.12	–	1.32	V	24)
55	V_{MDR} Drift over Temperature Range	$\lvert\Delta V_{MDR}/V_{MDR}\rvert$	–	–	5	%	–
56	V_{MDR} Drift over Supply Voltage Range 3 V … 5.5 V	$\lvert\Delta V_{MDR}/V_{MDR}\rvert$	–	–	10	%	–
57	V_{MDR} Drift over Temperature Range at Supply Voltage Range 3 V … 3.6 V	$\lvert\Delta V_{MDR}/V_{MDR}\rvert$	–	–	5	%	–
58	V_{MDR} Drift over Temperature Range at Supply Voltage Range 4.7 V … 5.3 V	$\lvert\Delta V_{MDR}/V_{MDR}\rvert$	–	–	5	%	–

Table 3 Characteristics and Operating Conditions (cont'd)

SP	Parameter	Sym-bol	Limit Values			Unit	Condi-tion
			min.	typ.	max.		
Logic Inputs RSTN, RST, LEN							
59	Input Voltage High	$V_{IHLOGIC}$	2.0	–	V_{CC}	V	25)
60	Input Voltage Low	$V_{ILLOGIC}$	0	–	0.8	V	25)
61	Input Current High	$I_{IHLOGIC}$	–	–	5	µA	–
62	Input Current Low	$I_{ILLOGIC}$	-5	–	–	µA	–
Logic Inputs CSELN							
63	Input Voltage High for disabling data input latch (nonclocked mode) or let CSELN open	$V_{IHLOGIC}$	2.2	–	V_{CC}	V	–
64	Input Voltage Low for enabling data input latch (clocked mode)	$V_{ILLOGIC}$	0	–	0.8	V	–
65	Internal Pull-Up-Resistor	R_{CSELN}	8	10	12	kΩ	–
Logic Outputs LF, HWA							
66	Output Voltage Low	$V_{OLLOGIC}$	–	–	0.4	V	–
67	Output Current High (Leakage Current)	$I_{OHLOGIC}$	–	–	100	µA	open collector
68	Output Current Low	$I_{OLLOGIC}$	2	–	–	mA	sink current
Modulation Control (Mode 2)							
69	Mode 1 select	V_{MODE}	V_{CC} - 0.8	–	V_{CC}	V	–
70	Mode 2 select	V_{MODE}	0	–	0.8	V	–
71	Internal pilot frequency	f_{PILOT}	7.7	12	17.3	kHz	–
72	Pilot frequency with external C_{OSC}	f_{PILOT}	(130 µs + 16 × C_{OSC} × 208 kΩ)$^{-1}$	(83 µs + 16 × C_{OSC} × 173 kΩ)$^{-1}$	(58 µs + 16 × C_{OSC} × 138 kΩ)$^{-1}$		15)
73	Effective pilot current amplitude on modulation current high level (default)	am_{PILOT}	–	3.5	–	%	26)

Table 3 Characteristics and Operating Conditions (cont'd)

SP	Parameter	Sym-bol	Limit Values			Unit	Condi-tion
			min.	typ.	max.		
74	Pilot current amplitude on bias current (default)	ab_{PILOT}	–	5.05	–	%	26)
75	Cutoff frequency of modulation controller with external C_{MOD}	f_{MOD}	(306 kΩ × C_{MOD})$^{-1}$	(204 kΩ × C_{MOD})$^{-1}$	(131 kΩ × C_{MOD})$^{-1}$		15)17)

1) Measured into 25 Ω.

2) The bias-, modulation-, the LF-, HWA- and MPOUT- output currents are not included.

3) The typical supply current is defined for driving a laser with about 20 mA bias current and about 20 mA modulation current and a IC junction temperature of about 50 °C and a V_{CC} of 5 V. The maximum supply current is defined for driving the upper limits of bias current and modulation current with worst case junction temperature and with a V_{CC} of 5.5 V (V_{CC} = V_{CCA} = V_{CCD}).

4) This describes the AC modulation current (the DC component is the overall offset current). AC modulation current is drawn by O at $V_D > V_{DN}$, it is drawn by ON at $V_D < V_{DN}$. I_{OH} refers to drawn modulation current (AC + DC). I_{OL} refers to an inactive current output (DC current only).

5) See **Table 2** for operating conditions junction temperature.

6) Inactive current output (see also 4)).

7) Modulation current when the laser diode is disabled.

8) Valid for V_{CC} = V_{CCA} = V_{CCD} = 5 V. It is possible to increase the output voltage range for the V_{CC} range of 5 V ± 0.5 V of about 0.85 V by using the Pad V_{CCD2} instead of V_{CCD} (see **Figure 14**). The specified limits for data and clock inputs are valid for V_{CCD}.

9) Adjustment of programmable parameter by resistor value within this range (see **Chapter 2.4**).

10) Adjusting the modulation current by R_{MOD} notice that the decreasing of R_{MOD} will increase the modulation current. R_{MOD} in combination with R_{TC} has to be adjusted that the modulation current is smaller than 50 mA or 75 mA respectively over specified temperature range. If R_{MOD}-Pad is not connected (open input) there will be no modulation current at the output O/ON.

11) Modulation current adaptation within junction temperature range. Low junction temperature represents a low additional modulation current. High junction temperature represents a high additional modulation current. If R_{TC}-Pad is not connected there will be no noteworthy modulation current adaptation.

12) Data/clock inputs are internally connected to V_{BBD}/V_{BBC} by resistor R_1/R_2 with a differential termination by R_{IN}. See data input stage description (see **Figure 9**).

13) The resistance is guaranteed for junction temperature 25 °C.

14) If data input duty cycle falls below lower limit or exceeds upper limit the laser will be disabled by ISM circuit. On the other hand, the laser will be enabled whenever the data input duty cycle goes back to the allowed range. Data input duty cycle refers to the quotient given by number of ones divided by number of zeros within serial data stream. The ISM-circuit evaluates the mean value of the duty cycle (integrator). The cutoff frequency of ISM f_{ISM} is defined for data pattern 1010 …. In case of data frequency is to small the ISM circuit will disable the laser because of long High- or Low-series. The ISM-circuit can be deactivated by a 25 kΩ resistor from CISM to V_{EE}. The ILM-circuit additionally is used for ac-coupled data inputs. It works as a peak detector. The laser will be disabled if data are set to a static state. The cutoff frequency of ILM fILM is defined for data pattern 1010 …. (Specified value is for data input voltage swing of 400 mV).The ILM-circuit is direct AC-coupled to the data input. So the cutoff frequency depends on data input swing. The ILM-circuit can be deactivated by a short from CILM to V_{CC}.

15) A capacitor within this range programs the time (or frequency).

16) Open collector output for pulling up a resistor to monitor the current.

17) Difference and temperature drift of passive IC component parameters match to passive IC component parameters in other circuit parts.

18) The supervisor circuit will detect a failure condition if MD voltage exceeds $V_{MDnom} \pm 2$ dB range. V_{MDnom} is given by nominal voltage level at MD which is set by V_{MDR}. The deviation is calculated with $20\lg(V_{MD}/V_{MDnom})$. The deviation of optical power is calculated with $10\lg(V_{MD}/V_{MDnom})$.

19) The supervisor circuit will detect no failure condition if MD input voltage ranges from V_{MDnom} - 1.2 dB to V_{MDnom} + 1.2 dB. V_{MDnom} is given by nominal voltage level at MD which is set by V_{MDR}. The deviation is calculated with $20\lg(V_{MD}/V_{MDnom})$. The deviation of optical power is calculated with $10\lg(V_{MD}/V_{MDnom})$.

20) A failure condition will be reported by LF = H if this condition lasts for t_{FDEL}. Minimal capacitor on CFDEL has to be chosen that the failure recognition time is longer than the setting time of the bias controller.

21) Time between LF high (or LEN high) and LDOFF high.

22) At supply voltages below V_{CC} threshold the laser diode bias and modulation current will be held disabled and LDOFF will be held high. Above the laser diode will be enabled after the Power On Delay.

23) The Power On Delay is the Reset time after V_{CC} voltage has risen above the V_{CC} reset threshold. During the Power On Delay the Laser diode bias and modulation current will be held disabled and LDOFF will be held high.

24) Temperature and voltage drift are included.

25) The minimal enable pulse width time for RST = L or RSTN = H or LEN = L has to be longer then t_{FDEL}.

26) Out of am_{PILOT} and ab_{PILOT} a factor K = ab_{PILOT}/am_{PILOT} can be defined, which is an important factor for the pilot control (for definition of am_{PILOT} and ab_{PILOT} see **Figure 8**). For most laser diodes the optimum value of K is 1.44 (default value). If K is set close to factor 2 the modulation current and jitter may increase. If K is set close to factor 1 the modulation current may decrease. In both cases a malfunction of laser control is possible. A resistor between V_{CC} and RMRIP can be used for decreasing am_{PILOT}. Further a resistor between V_{CC} and RBRIP can be used for decreasing ab_{PILOT}. So the factor K can be adjusted. For default factor K let RBRIP and RMRIP connected to V_{CC} (= V_{CCA}).

2.4 Typical Characteristics of Temperature Compensation (Mode 1)

2.4.1 Modulation Current Swing versus R_{MOD}, R_{TC}, Junction Temperature and Supply Voltage / High Current Drive

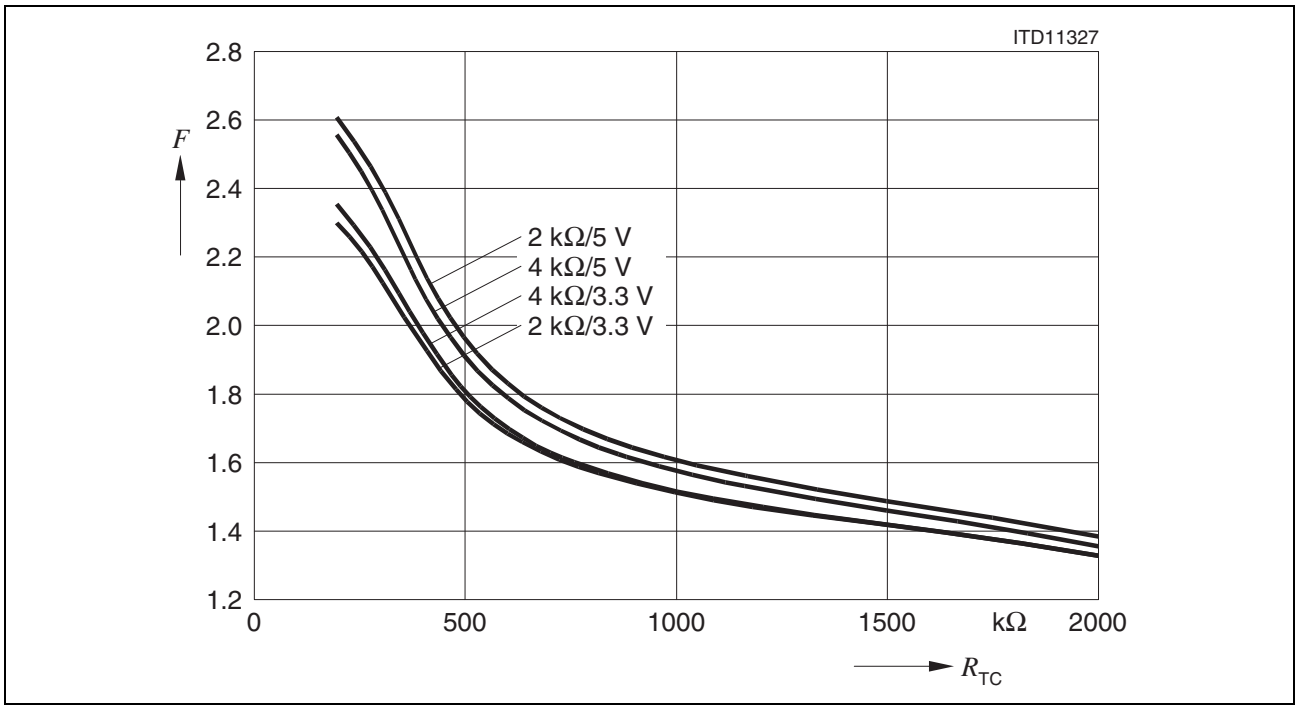

Figure 2 $F = I_{100\,°C}/I_{0\,°C}$ versus R_{TC}, Parameter R_{MOD}, V_{CC}

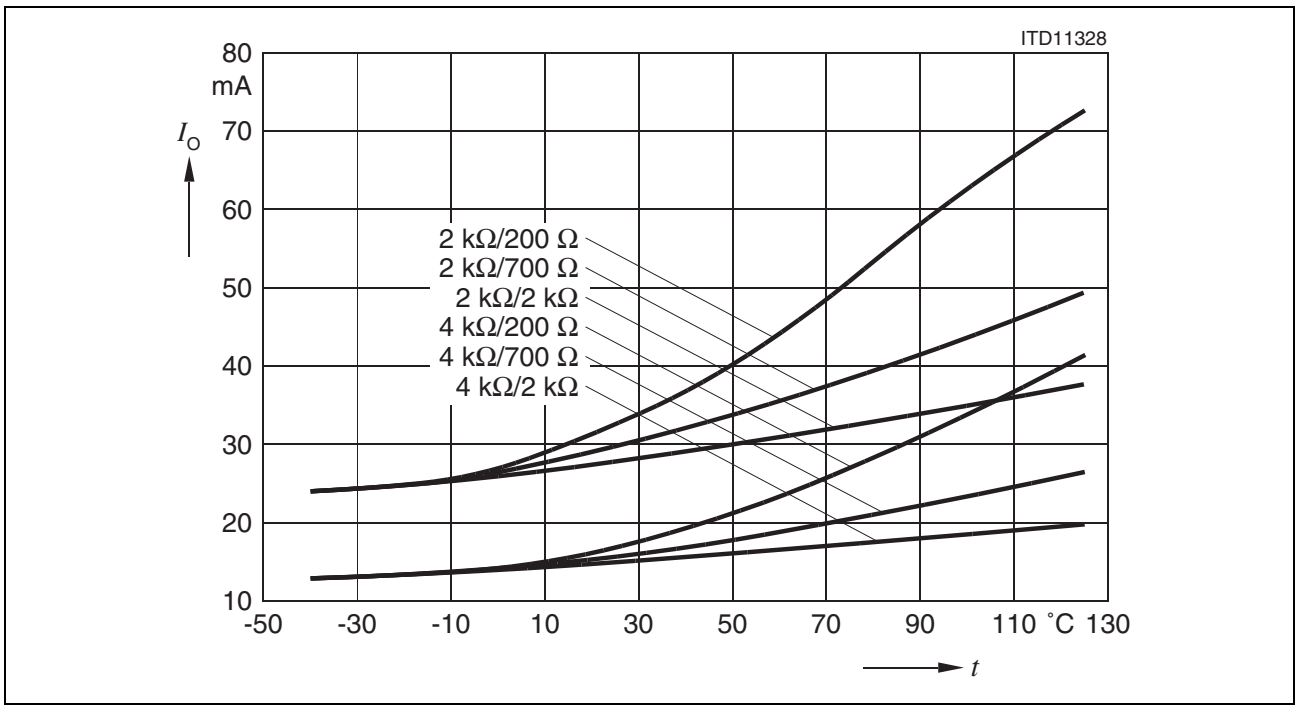

Figure 3 I_0 versus T_j, Parameter R_{MOD}, R_{TC} (V_{CC} = 3.3 V)

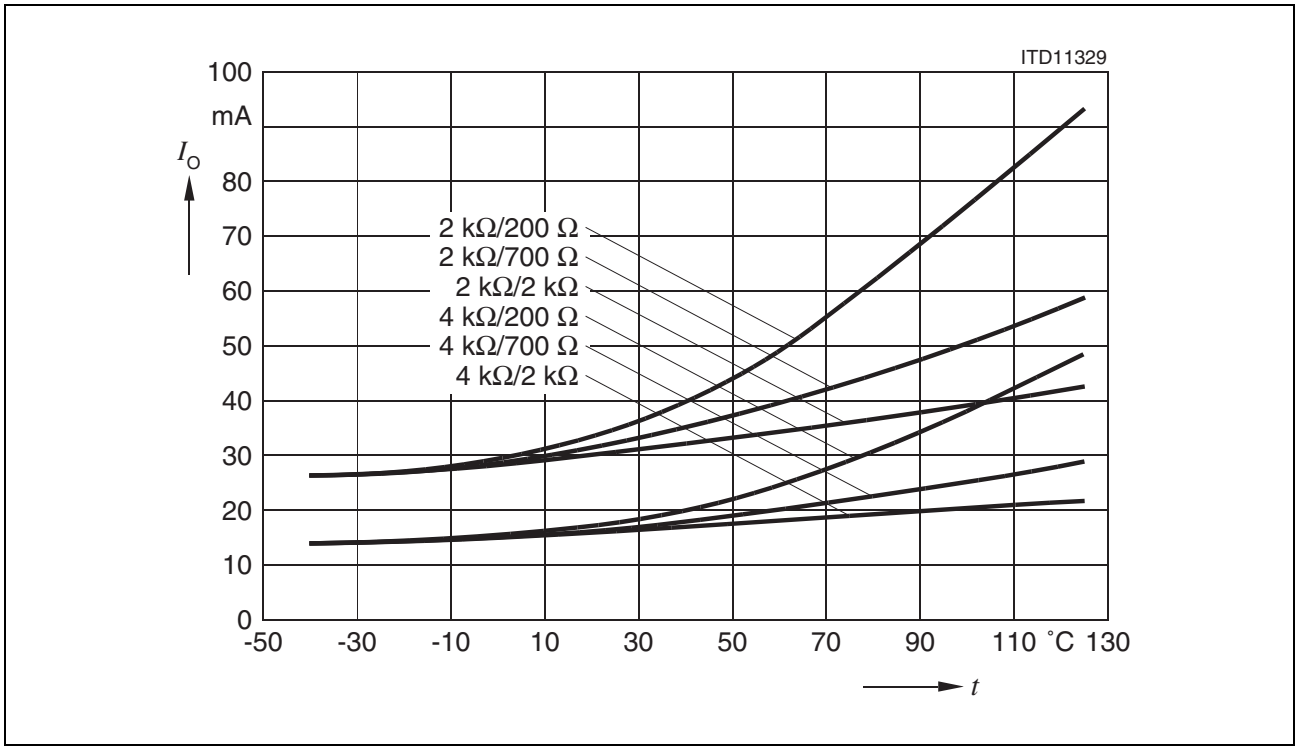

Figure 4 I_0 **versus** T_j**, Parameter** R_{MOD}**,** R_{TC} **(**V_{CC} **= 5.0 V)**

2.4.2 Modulation Current Swing versus R_{MOD}, R_{TC}, Junction Temperature and Supply Voltage / Low Current Drive

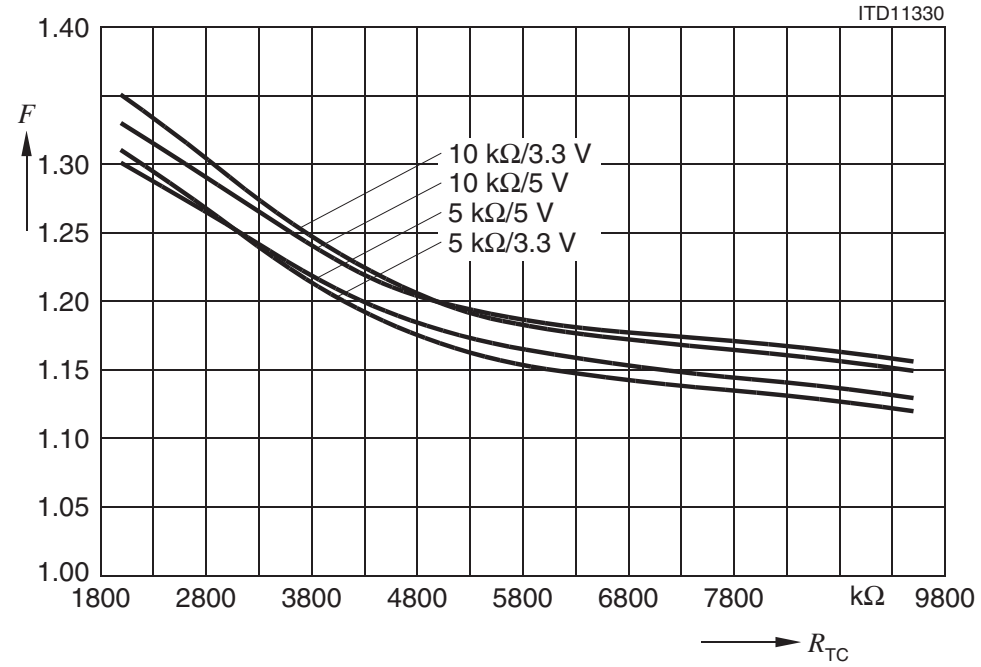

Figure 5 $F = I_{100\,°C}/I_{0\,°C}$ versus R_{TC}, Parameter R_{MOD}, V_{CC}

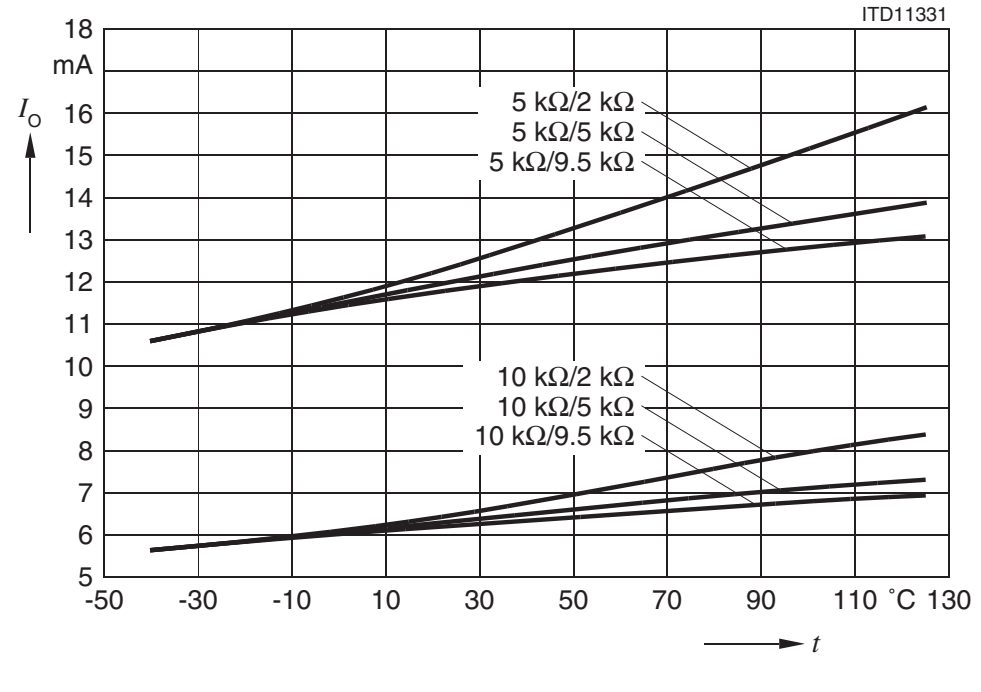

Figure 6 I_0 versus T_j, Parameter R_{MOD}, R_{TC} (V_{CC} = 3.3 V)

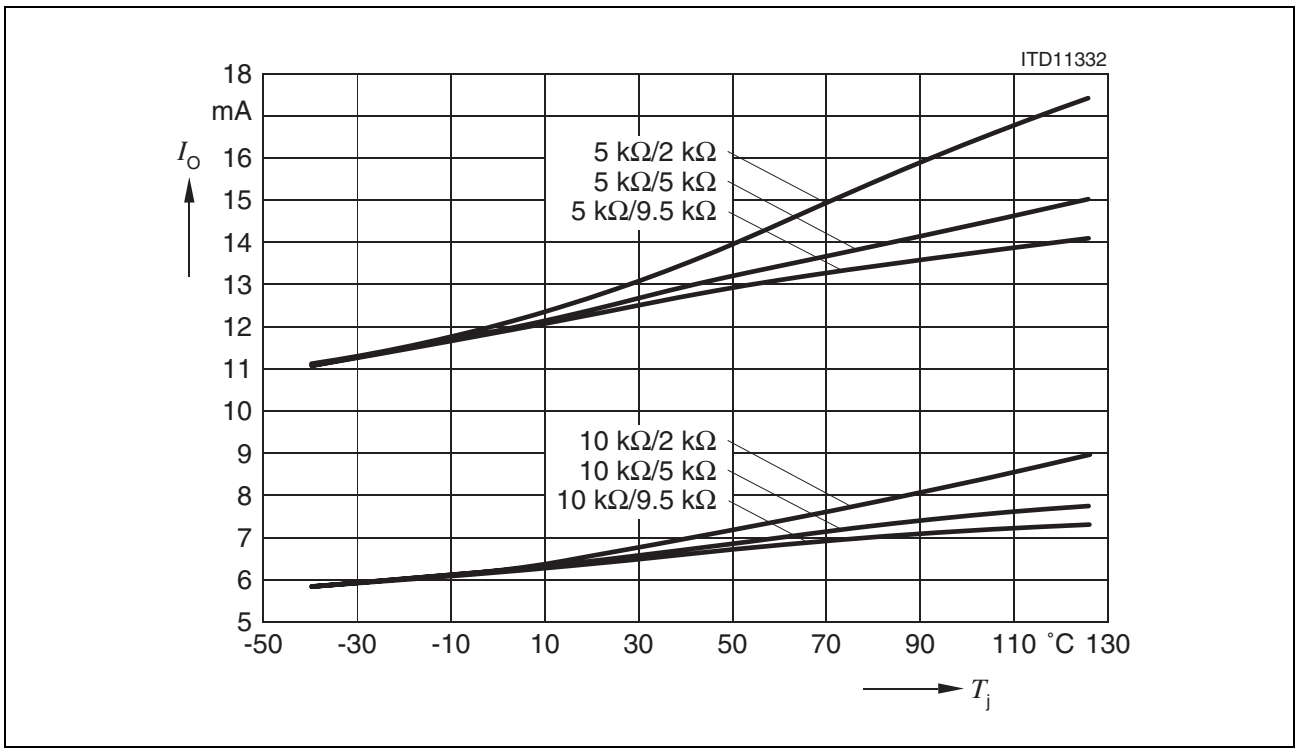

Figure 7 I_0 **versus** T_j**, Parameter** R_{MOD}**,** R_{TC} **(**V_{CC} **= 5.0 V)**

2.5 Principle of Modulation Current Control by Using a Pilot Signal (Mode 2)

The DC-part of the monitor current controls the bias current. The difference of the optical low frequency AC-part ΔPpp is used for the modulation current control. ΔPpp is measured over the monitor current. The aim of the control is to settle ΔPpp to Zero. (That means a part of the pilot current amplitude on bias current is modulated below laser current threshold. Therefore please take into account the laser characteristics, e.g. switch-on delay, for higher data rates.) Mode 2 can only be used for DC-coupled laser diodes.

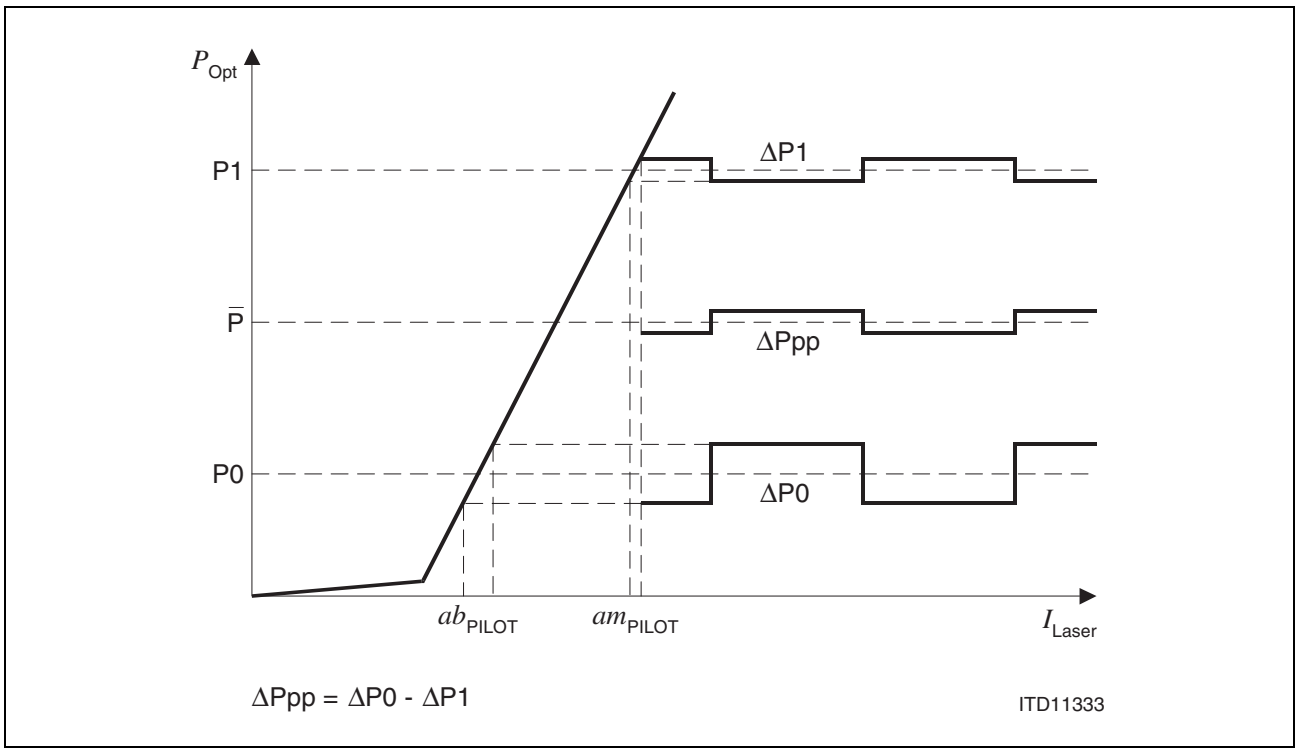

Figure 8 Modulation Current Control by Using a Pilot Signal

2.6 Data / Clock Input Stage

Data and clock inputs are terminated with 100 Ω and are connected to a V_{BB} reference by resistors R_1/R_2. (V_{BB} for Clock input is V_{BBC}, V_{BB} for Data input is V_{BBD}.) This easily provides the input reference voltage at AC coupling. A schematic of the input stage is shown below:

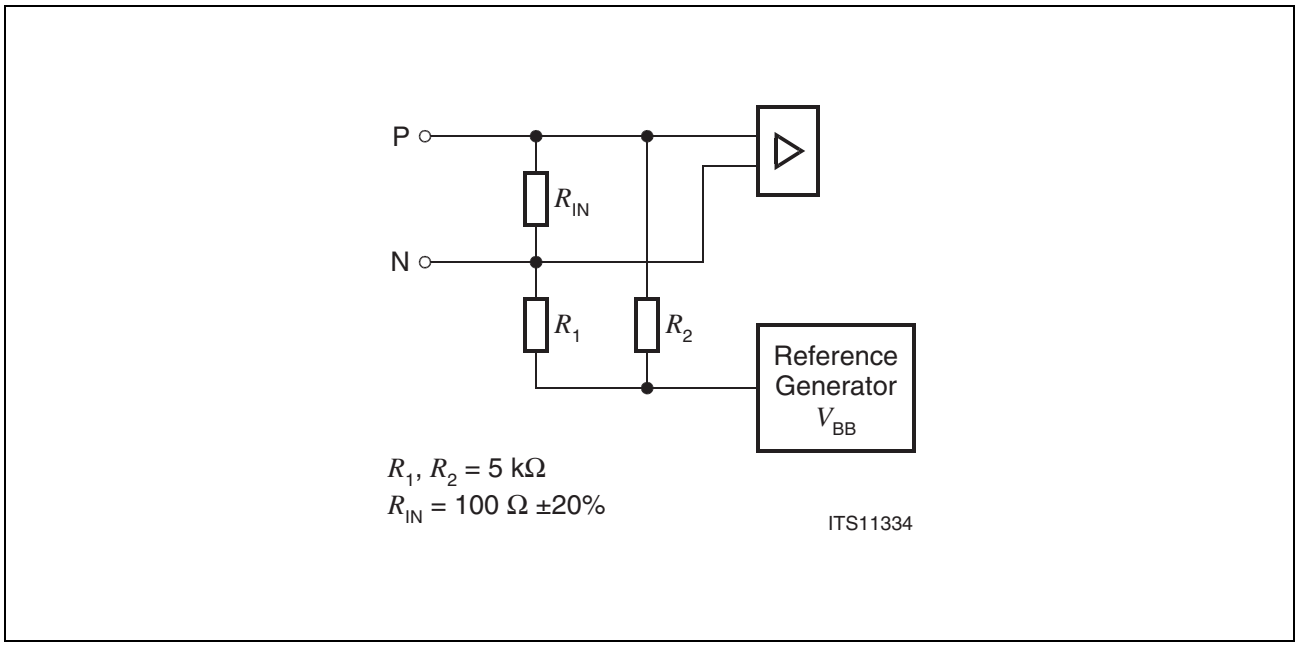

Figure 9 Data/Clock Input Stage

2.7 Timing of Clock and Data

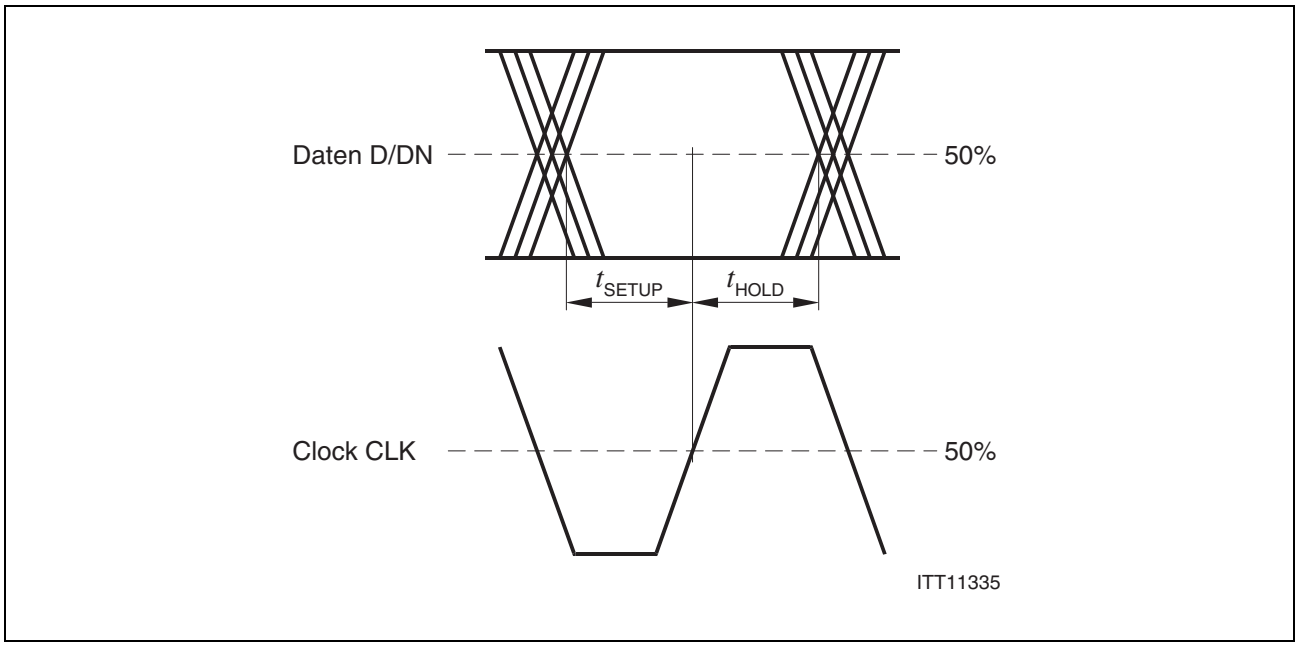

Figure 10 Timing of Clock and Data

2.8 Laser and V_{CC} Supervising Circuit

If there is a laser fault (optical power deviates ±1 dB) this signal is stored and indicated by LF (logic high). The fault indication (LF) can be reset with low level at RSTN or with high level at RST or with power down (V_{CC} < V_{CC} Reset Threshold) only. After power up, LF will always be cleared. Disabling the laser by LEN does not influence a previous fault indication by LF. The laser fault generation can be switched off by connecting CFDEL to V_{CC}. During RSTN is logic low or RST is logic high the circuit is in Reset state.

In case of changing RST = H or RSTN = L after laser fault recognition LF = H (after t_{FDEL}) there is an additional delay time implemented which has the same value as the Power On Delay.

If the supply voltage is lower than the V_{CC} reset threshold the indicator Hardware Alarm (HWA) is still at the low level and the circuit is in Reset state.

During Power On Delay the circuit is in Reset state too. The Power On Delay is defined as the delay after V_{CC} voltage has risen above the V_{CC} reset threshold. This time can be adjusted by an external capacitor at COSC (Mode 1). The Reset N-Output of the MAX 809S Power Supervisor IC can be connected to RSTN to use the reset function of the MAX 809S.

The laser control by RST and RSTN is fully redundant. This means only an AND combination of RST = 0 / RSTN = 1 can switch the laser on. The OR combination of RST = 1 / RSTN = 0 switches the laser off (see **Table 4** for clarification).

Table 4 Laser Diode Currents Enable / Disable Signals

RST	LEN	RSTN	In Case of Laser Fault	V_{CC} < Reset Threshold V_{CC}	LDOFF	Modulation Enable[1)]	Bias Enable[1)]	LF (high active)
X	1	X	0	X	1	0	0	0
1	X	X	X	X	1	0	0	0
X	X	0	X	X	1	0	0	0
X	X	X	X	yes	1	0	0	0
0	0	1	1	no[2)]	1[3)]	0	0	1[3)]
0	0	1	0	no[2)]	0[4)]	1	1	0

1) Internal signal

2) After Power On Delay

3) After t_{FDEL}

4) Sink current enabled = Low

Table 4 shows the static states of these signals. Dynamic changes or delays due to external delay capacitors are not shown.

Bias current is disabled by setting Bias Enable low, modulation current is disabled by setting Modulation Enable low.

LEN do not effect LF. This means LF can not be reset by LEN.

2.9 Input Signal Monitoring and Hardware Alarm (Consideration in absence of Laser Fault)

Table 5 Function of ISM Circuit and Hardware Alarm Indicator (HWA)

Data Level (after delay of ISM)	V_{CC} < Reset Threshold of V_{CC} /Circuit in Reset state	ISM Laser Enable[1)]	LDOFF	HWA (low active)	Modulation Enable[1)]	Bias Enable[1)]
Constant High	No	0	1	0	0	0
Constant Low	No	0	1	0	0	0
Constant High	Yes	0	1	0	0	0
Constant Low	Yes	0	1	0	0	0
Duty Cycle ok	Yes	1	1	0	0	0
Duty Cycle ok	No	1	0[2)]	1	1	1

1) Internal signal

2) Sink current enabled = Low

3 Pin Description

Table 6 Pin Definitions and Functions

Signal Name	Function	Explanation
D / DN	Differential Input	Differential data input. D corresponds to O and DN to ON current output. With a high level at D and a low level at DN modulation current is drawn by O and ON is inactive. With a low level at D and a high level at DN modulation current is drawn by ON and O is inactive. Both inputs are prebiased to internal V_{BBD}. The input termination is 100 Ω.
CLK / CLKN	Differential Input	Differential clock input for input data latch. The input termination is 100 Ω.
CSELN	Logic Input	A low level at CSELN enables the data input latch (clocked mode), a high level or an open input disables the data input latch (nonclocked mode). It has an internal pull-up-resistor of about 10 kΩ.
O / ON	Differential Current Output	These output signals drive the modulation current switched by D / DN data inputs.
CMOD	Control	The modulation controller characteristic can be set to an i-controller with an external capacitor at CMOD to V_{EE} and the time constants are adjustable in mode 2. Let open if mode 1 is used.
VMOD	Output	Base of the output current mirror 1:10. For normal application it can be leave open if not used.
CISM	Control	With an external capacitor at CISM to V_{CC} the delay time for detection of a bad duty cycle data input situation can be increased. If the input signal monitor is not used CISM has to be pulled down by 25 kΩ resistor to V_{EE}.
CILM	Control	With an external capacitor at CILM to V_{CC} the delay time for detection of static data input situation can be increased. If the peak detector is not used CILM has to short to V_{CC}.
HWA	Logic Output	HWA is an open collector output (indicator output). A low level is generated whenever a bad duty cycle data input situation is detected by the input signal monitor circuit or if the supply voltage is lower than the V_{CC} reset. Let open if not used.

Table 6 Pin Definitions and Functions (cont'd)

Signal Name	Function	Explanation
IBIAS	Bias Output	A sink current drawn by IBIAS determines the laser diode bias current.
CBIAS	Control	The bias controller characteristic is set to an i-controller. The cutoff frequency can be decreased by an external capacitor at CBIAS to V_{EE}.
MPOUT	Monitor Output	MPOUT is an open collector output for pulling up a resistor to monitor the deviation of the optical power over the monitor diode current. Let open if not used.
RPOUT	Control	A resistor between RPOUT and V_{EE} can adjust the relation of optical power measured over the monitor diode current to output current at MPOUT. Let open if the monitoring of the optical power is not used.
VBIAS	Bias Output	This output can be connected to the base of an external bias current NPN transistor. It can be leave open if not used. It is dedicated for applications which can not use the internal bias transistor. Base of the output current mirror 1:25.
MD	Monitor Diode Input	This is the controller feedback input. The voltage at this input represents the monitor diode current and by this the laser output power. The bias current will be controlled to an equal level of V_{MD} and V_{MDR}.
LDOFF	Laser Shut Down Output	Whenever the laser diode is disabled LDOFF will deliver a high voltage level closed to V_{CC}. If the laser diode is enabled there is a sink current to drive the base of an external pnp transistor to support a laser diode supply shut down. If not used this output can be leave open without Laser Driver performance restrictions. There is an internal pull up resistor between LDOFF and V_{CCA} of 10k.
RSTN	Logic Input	Low active reset input. This input resets the LF indication if present. Further the laser diode is held within shut down mode if this signal is at low level. For constant laser diode enable this signal can be tied to V_{CC}.

Table 6 Pin Definitions and Functions (cont'd)

Signal Name	Function	Explanation
RST	Logic Input	High active reset input. This input resets the LF indication if present. Further the laser diode is held within shut down mode if this signal is at low level. For constant laser diode enable this signal can be tied to V_{EE}.
LEN	Logic Input	A low level at LEN enables the laser diode, a high level disables the laser diode. For constant enable this input can be tied to V_{EE}.
LF	Logic Output	Fault Indicator. A high level is generated whenever a fault situation is detected by the supervisor circuit. Fault situations are laser power failures indicated by MD input voltage deviation from V_{MDnom}. Let open if not used.
CFDEL	Control	With an external capacitor at CFDEL to V_{EE} the laser fault detection delay time can be increased. This means if a constant fault condition is present a laser fault indication will be generated and the laser will be shut down after this delay time. The laser safety circuit can be switched off if CFDEL is connected to V_{CC}.
COSC	Control	With an external capacitor at COSC to V_{EE} the piloton frequency can be decreased (mode 2). COSC determines the power on delay.
MODE	Logic Input	A high level at MODE sets the modulation control circuit to mode 1 (using temperature compensation circuit). A low level at MODE sets the modulation control circuit to mode 2 (using modulation control by pilot signal).
RMOD	Control	An external resistor at RMOD to V_{EE} sets the modulation current level (in mode 1). Let open if mode 2 is used.
RTC	Control	An external resistor at RTC to V_{EE} sets the modulation current temperature coefficient. The temperature information is derived from chip junction temperature (in mode 1). Let open if mode 2 is used.

Table 6 Pin Definitions and Functions (cont'd)

Signal Name	Function	Explanation
RBRIP	Control	The pilot current amplitude on bias current (mode 2) can be decreased by connecting a resistor between RBRIP and V_{CC}. For default values do connect to V_{CC}. It has no influence if using mode 1. Let open if mode 1 is used.
RMRIP	Control	The pilot current amplitude on modulation current high level (mode 2) can be decreased by connecting a resistor between RMRIP and V_{CC}. For default values do connect to V_{CC}. It has no influence if using mode 1. Let open if mode 1 is used.
START	–	Do not connect.
MX	–	Do not connect.
V_{CCA}	Power Supply	Positive power supply for analog circuit part.
V_{CCD}	Power Supply	Positive power supply for digital circuit part.
V_{CCD2}	Power Supply	Positive power supply for digital circuit part with an additional serial diode to increase the modulation output voltage range of about 0.85 V for V_{CC} range of 5 V ± 0.5 V. Let open if it is not used.
V_{EE1}	Power Supply	Negative power supply, only connected to the output current mirror stage of bias generator, normally GND.
V_{EE2}	Power Supply	Negative power supply, only connected to the output stage, normally GND.
V_{EE}	Power Supply	Negative power supply of the rest of circuit, normally GND.

3.1 Pad Layout

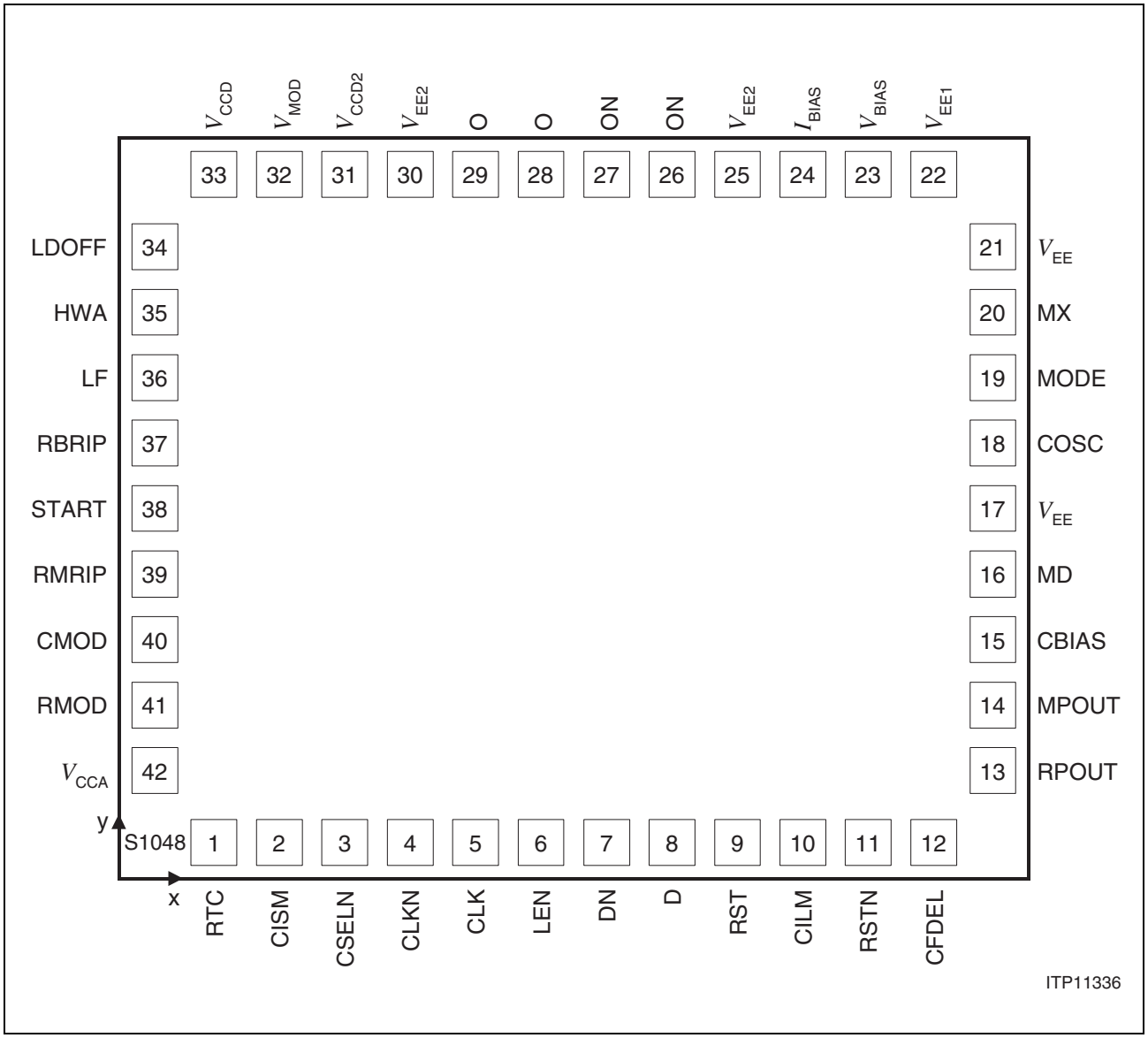

Figure 11

The pad center x/y positions are given in **Table 7** (related to the chip origin 0/0 excl. Seal ring):

Table 7 Pad Positions

Bottom:	1-12	Right:	13-21	Top:	33-22	Left:	42-34
x / µm	y / µm	x / µm	y / µm	x / µm	y / µm	x / µm	y / µm
271	137	1777	267	271	1498	141	267
396	137	1777	391	396	1498	141	391
521	137	1777	516	521	1498	141	516
646	137	1777	693	646	1498	141	693
771	137	1777	818	771	1498	141	818
896	137	1777	943	896	1498	141	943
1021	137	1777	1119	1021	1498	141	1119
1146	137	1777	1244	1146	1498	141	1244
1271	137	1777	1369	1271	1498	141	1369
1396	137	–	–	1396	1498	–	–
1521	137	–	–	1521	1498	–	–
1646	137	–	–	1646	1498	–	–

– Die size: 1.92 mm × 1.64 mm (excl. seal ring)
– Chip thickness: 300 µm
– Frame grid: 2.024 mm × 1.75 mm
– Bondpad window: 80 µm × 80 µm
– Bondpad material: Aluminium
– Substrate: V_{EE}

4 Application Examples

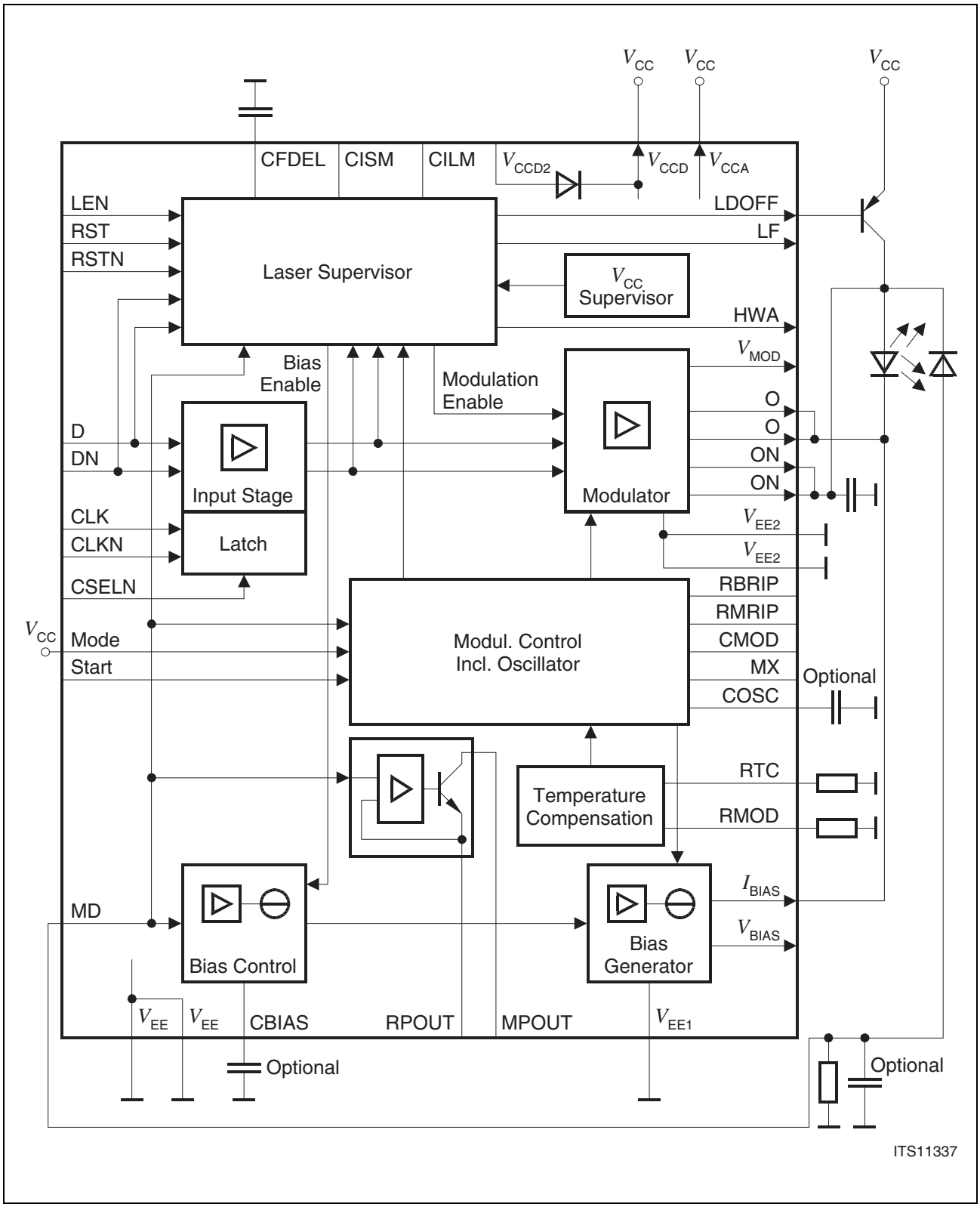

Figure 12 Application Example A:
Using Mode 1

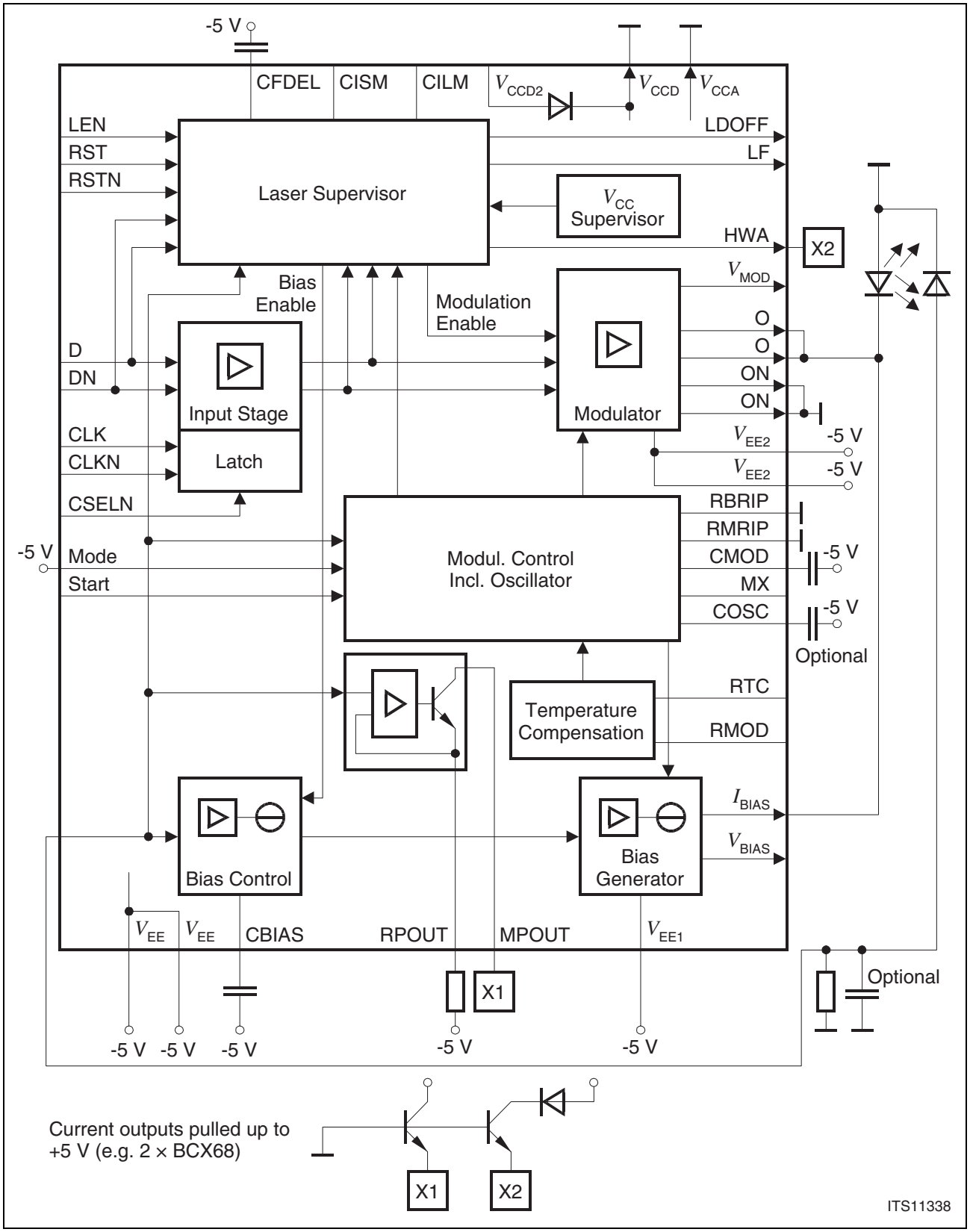

Figure 13 **Application Example B: Power Supply with +5 V … 0 V (GND) … -5 V** Using Mode 2

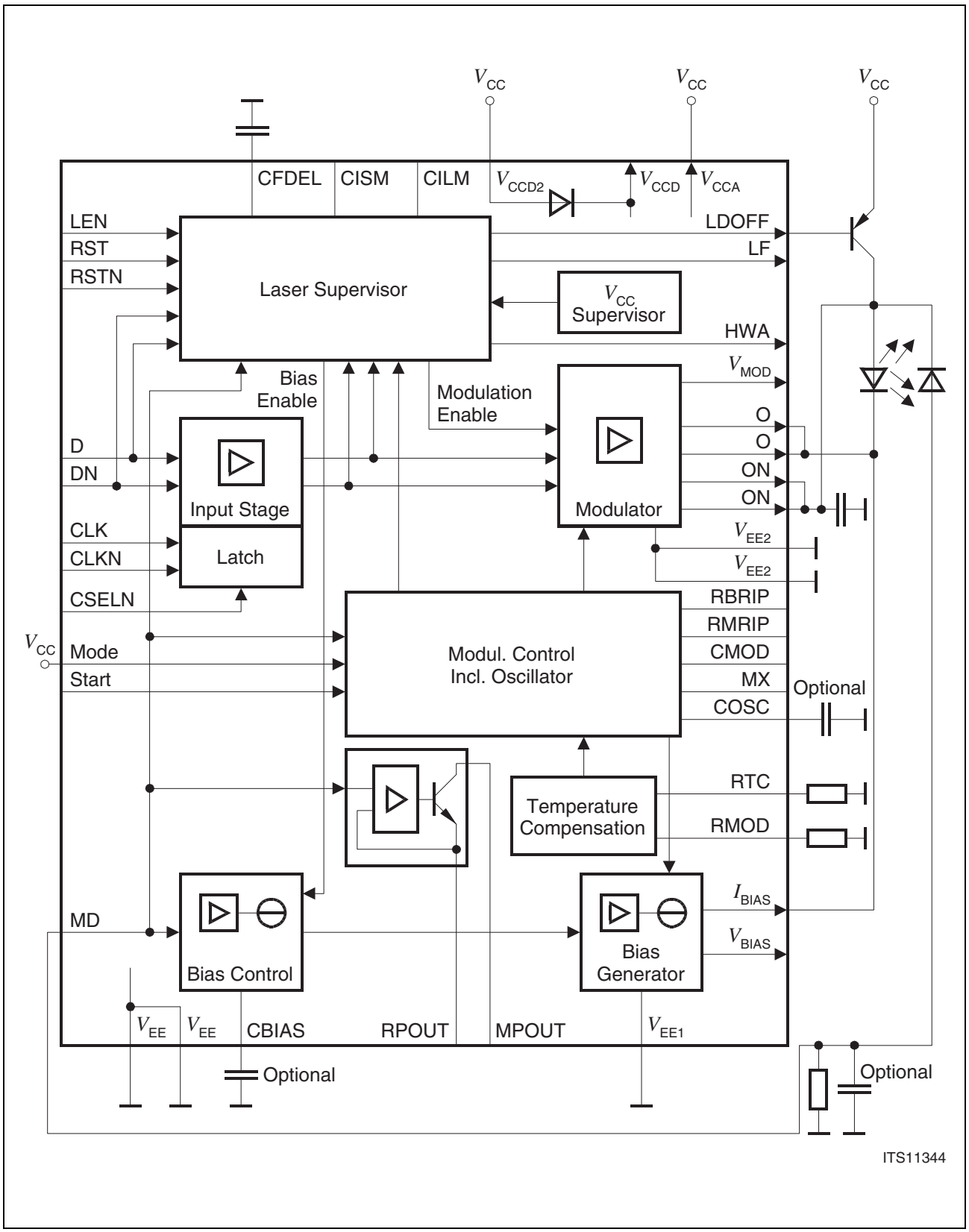

Figure 14 Application Example C: Using V_{CCD2} for increasing the Modulation Output Voltage Range for the V_{CC} Range of 5 V ± 0.5 V (here mode 1)

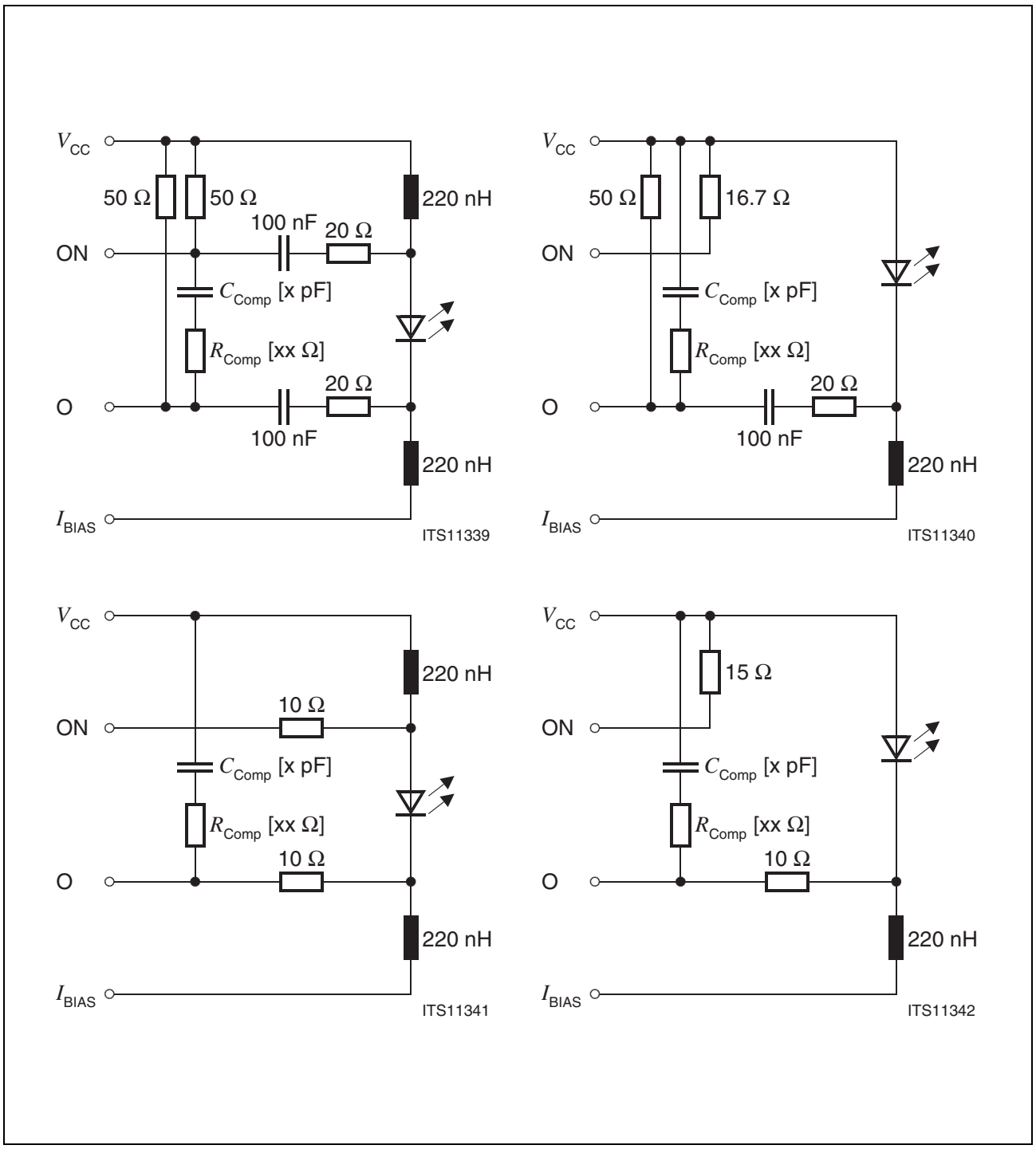

Figure 15 Application Example D: Several Kinds for Connecting Laser Diode (1300 nm-FP-laser, 5 Ω);

Resistor values are proposed values. They depend on used laser diodes, currents and mechanical and PCB design.

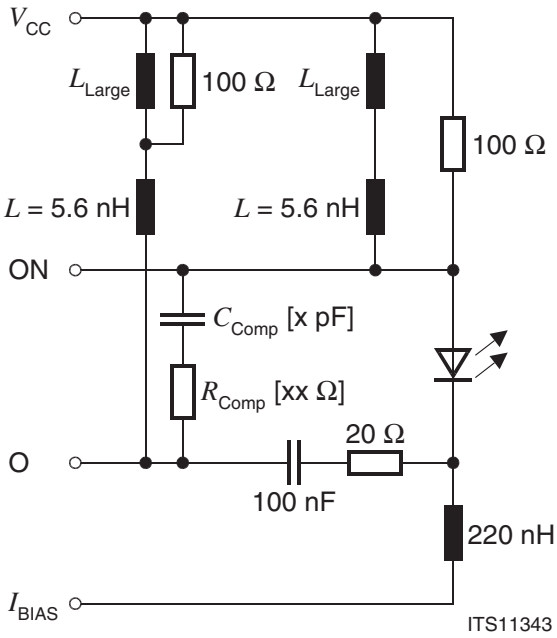

Figure 16 Application Example D: Several Kinds for Connecting Laser Diode (1300 nm-FP-laser, 5 Ω) (cont'd)**;**

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