

Semiconductor Solutions for High Speed Communication and Fiber Optic Applications

FOA41001B1 16:1

Multiplexer with Clock Multiplication Unit Chip
MUX 9.95 - 10.7 Gbit/s, 3.3 V

FOA51001B1 1:16

Demultiplexer with Clock and Data Recovery Chip
DEMUX 9.95 - 10.7 Gbit/s, 3.3 V

The transceiver chipset (MUX + DEMUX) is compliant with the Optical Internetworking Forum (OIF)-Physical Layer Group's OIF99.102 recommendation. These devices offer differential interfaces at 622 Mbit/s without external components. The multiplexer integrates a low noise LC VCO, meets Bellcore's OC-192 jitter requirements and incorporates pseudo 8-Bit FIFO (First in, First out).

The companion FOA51001B1 10 Gbit/s 1:16 demultiplexer encompasses a complete CDR with high data system sensitivity to enhance the system margin. Each device runs on a single 3.3 V power supply, with consumption of approximately 1.25 W and incorporates an integrated low noise Phase Locked Loop (PLL).



Features

- Compliant to the Optical Internetworking Forum (OIF)-Physical Layer Group's OIF99.102 recommendation
- Jitter performance compliant with ITU-T and Bellcore
- Internal low phase noise LC-VCO
- Differential input voltage range: 40 mV - 800 mV (pk-pk)
- Two reference clock options: 155 MHz or 622 MHz
- MUX only: Two receiver clock modes, 311 MHz or 622 MHz
- Adjustment of sampling threshold and phase

- Loss of lock detection
- Tunable center frequency from 9.95 GHz to 10.7 GHz

Typical Applications

- Fiber optics telecom and datacom applications
- SONET/SDH OC-192/STM-64 with and without FEC

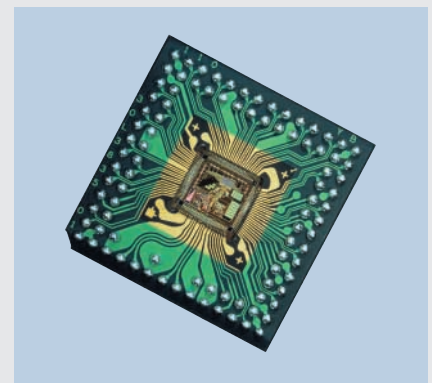
Main Advantages

- Data rate from 9.95 Gbit/s to 10.7 Gbit/s
- Single supply voltage 3.3 V

- Industry's lowest power consumption of typical 2.5 W for MUX and DEMUX Chipset (1.2 W for MUX; 1.3 W for DEMUX)
- Real differential LVDS interface (100 Ω termination on-chip)
- MUX only: advanced FIFO architecture (±2.4 ns drift tolerance at 9.95 Gbit/s)

Packing

Type	Sales Code	Package
MUX 16:1	FOA41001B1	P-HBGA-92
MUX 16:1	FOA41002B1	Bare Die
DEMUX 1:16	FOA51001B1	P-HBGA-92
DEMUX 1:16	FOA51002B1	Bare Die



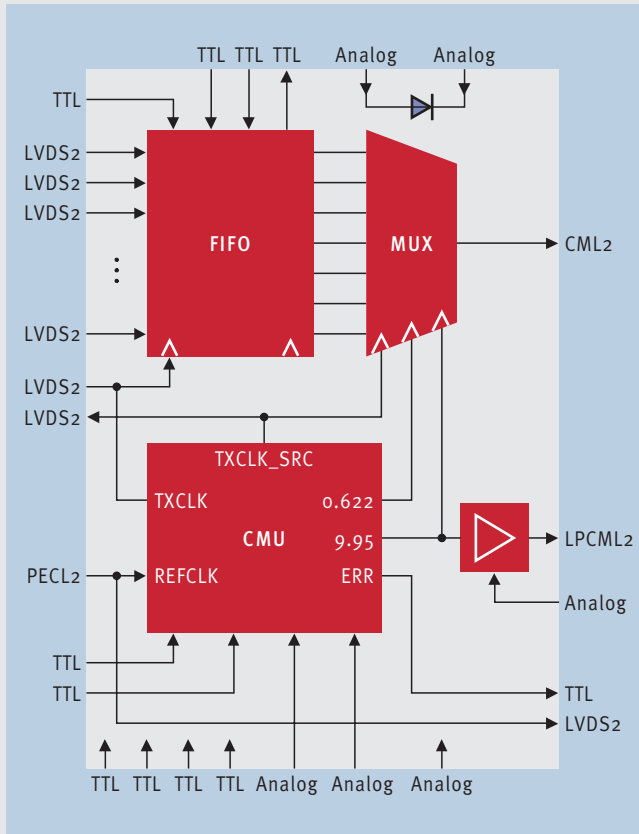
FOA 4 1 0 0 / 5 1 0 0

MUX/DEMUX

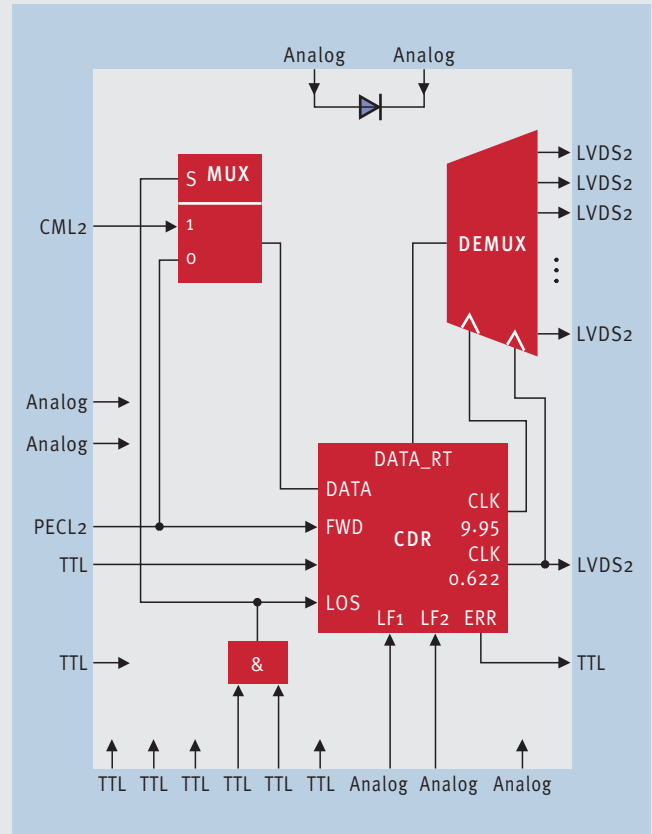
9.95 - 10.7 Gbit/s, 3.3 V



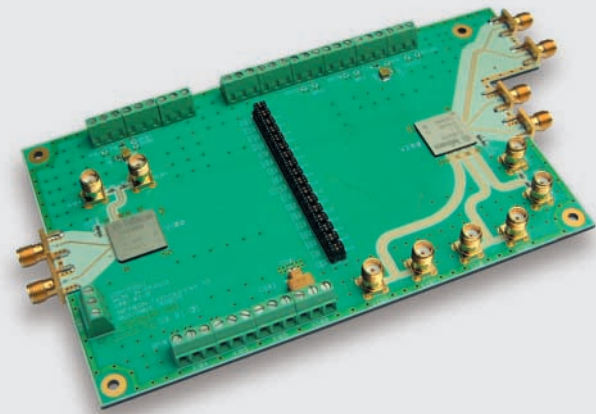
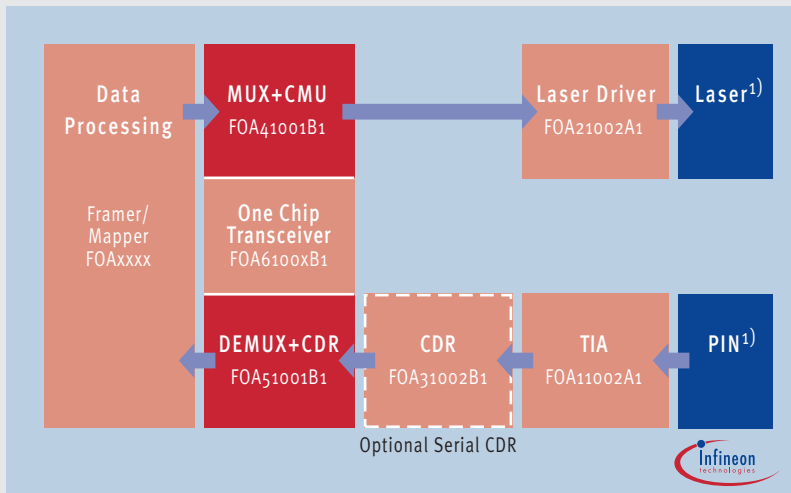
FOA41001B1 MUX Block Diagram



FOA51001B1 DEMUX Block Diagram



10 Gbit/s Chipset Overview



How to reach us:
<http://www.infineon.com>

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 St.-Martin-Strasse 53,
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