Ordering number:EN4494

FP205

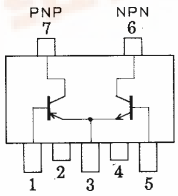
PNP/NPN Epitaxial Planar Silicon Transistors

Push-Pull Circuit Applications

Features

- Composite type with a PNP transistor and an NPN transistor in one package, facilitating high-density mounting.
- The FP205 is composed of 2 chips, one being equivalent to the 2SA1416 and the other 2SC3646, which are placed in one package.

Electrical Connection

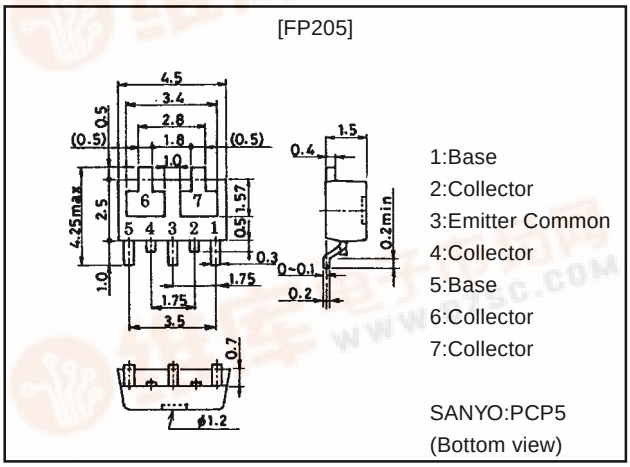


1:Base
2:Collector
3:Emitter Common
4:Collector
5:Base
6:Collector
7:Collector
(Top view)

Package Dimensions

unit:mm

2097A



1:Base
2:Collector
3:Emitter Common
4:Collector
5:Base
6:Collector
7:Collector

SANYO:PCP5
(Bottom view)

Specifications

Absolute Maximum Ratings at Ta = 25°C

( ) : PNP

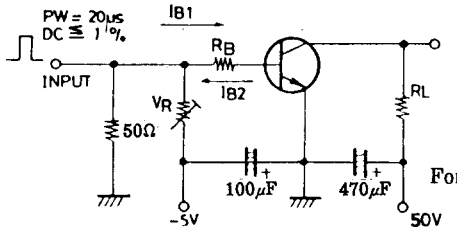
Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V_{CBO}		(–)120	V
Collector-to-Emitter Voltage	V_{CEO}		(–)100	V
Emitter-to-Base Voltage	V_{EBO}		(–)6	V
Collector Current	I_C		(–)1	A
Collector Current (Pulse)	I_{CP}		(–)2	A
Base Current	I_B		(–)0.2	A
Collector Dissipation	P_C	Mounted on ceramic board (250mm²×0.8mm) 1unit	0.8	W
Total Power Dissipation	P_T	Mounted on ceramic board (250mm²×0.8mm)	1.1	W
Junction Temperature	Tj		150	°C
Storage Temperature	Tstg		–55 to +150	°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditons	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	V_{CB}=(–)100V, I_E=0			(–)100	nA
Emitter Cutoff Current	I_{EBO}	V_{EB}=(–)4V, I_C=0			(–)100	nA
DC Current Gain	h_{FE}	V_{CE}=(–)5V, I_C=(–)100mA	140		400	
Gain-Bandwidth Product	f_T	V_{CE}=(–)10V, I_C=(–)100mA		120		MHz
Output Capacitance	Cob	V_{CB}=(–)10V, f=1MHz		(13)		pF
				8.5		pF
C-E Saturation Voltage	$V_{CE(sat)}$	I_C=(–)400mA, I_B=(–)40mA		(–0.2)	(–0.6)	V
				0.1	0.4	V
B-E Saturation Voltage	$V_{BE(sat)}$	I_C=(–)400mA, I_B=(–)40mA		(–)0.85	(–)1.2	V
C-B Breakdown Voltage	$V_{(BR)CBO}$	I_C=(–)10μA, I_E=0	(–)120			V
C-E Breakdown Voltage	$V_{(BR)CEO}$	I_C=(–)1mA, R_{BE}=∞	(–)100			V
E-B Breakdown Voltage	$V_{(BR)EBO}$	I_E=(–)10μA, I_C=0	(–)6			V
Turn-ON Time	t_{on}	See specified Test Circuit		(80)80		ns
Storage Time	t_{stg}	See specified Test Circuit		(700) 850		ns
Fall Time	t_f	See specified Test Circuit		(40)50		ns

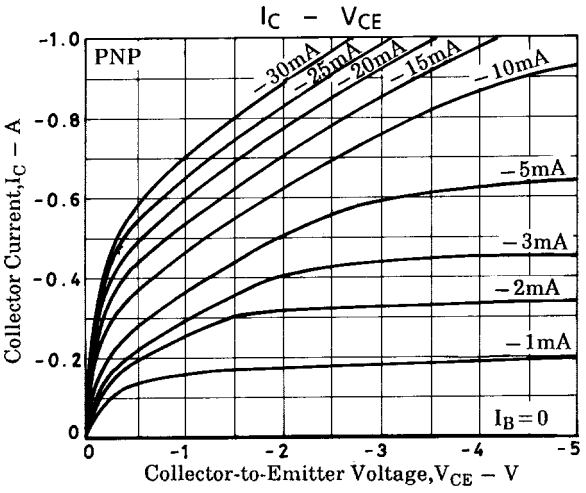
Marking:205

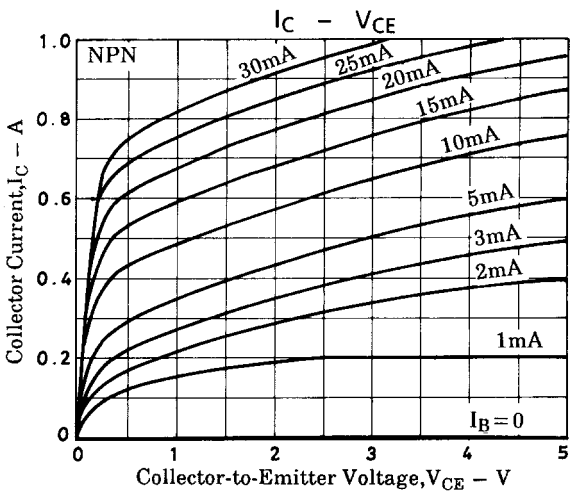
Switching Time Test Circuit

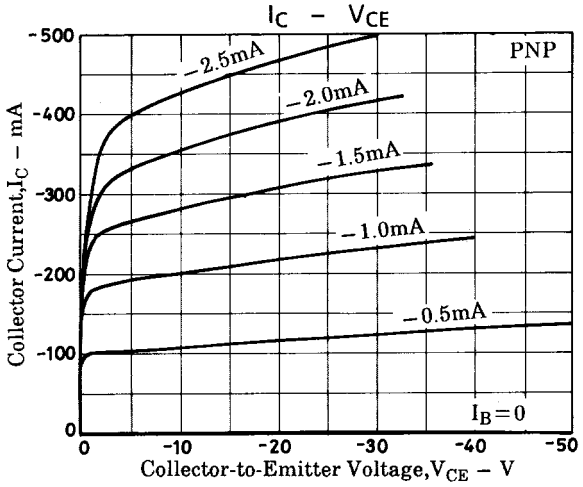


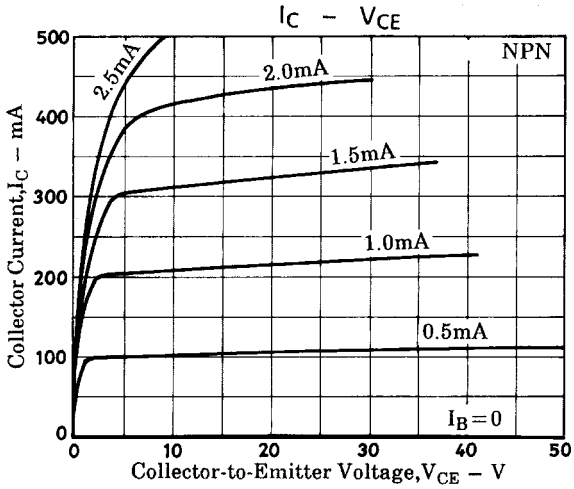
For PNP, the polarity is reversed.

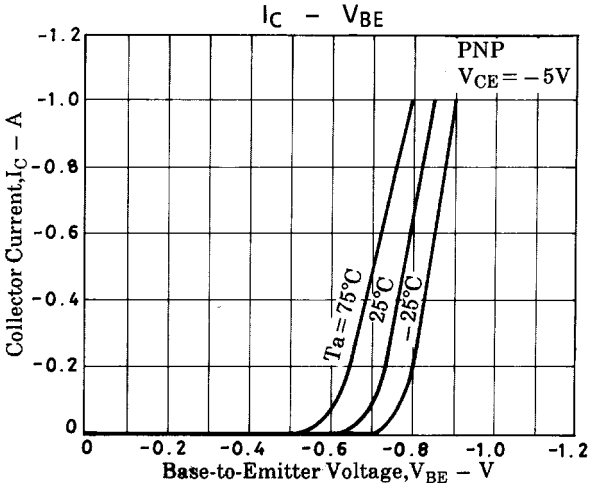
$10I_{B1} = -10I_{B2} = I_C = 400mA$

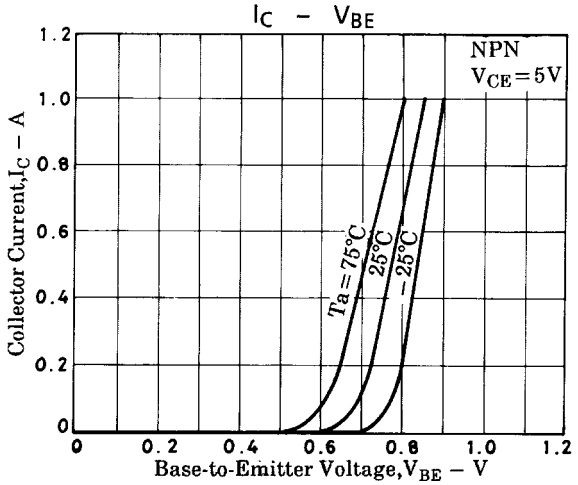




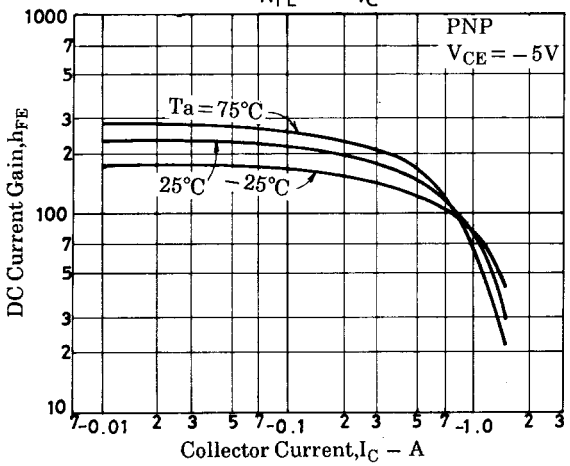




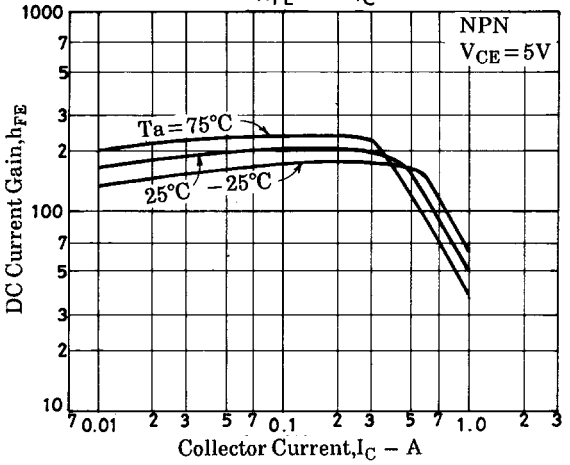




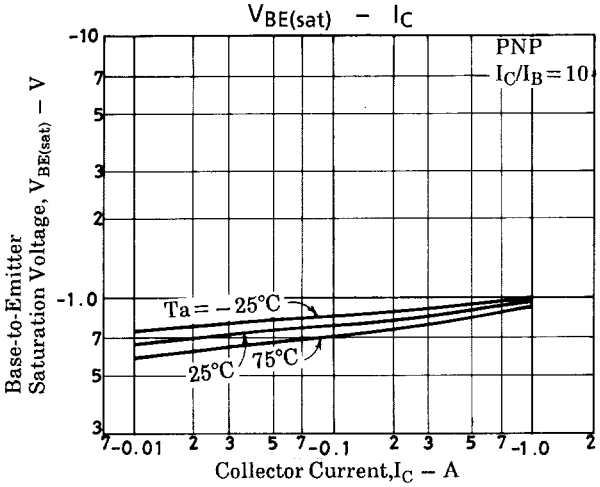
h_{FE} – I_C



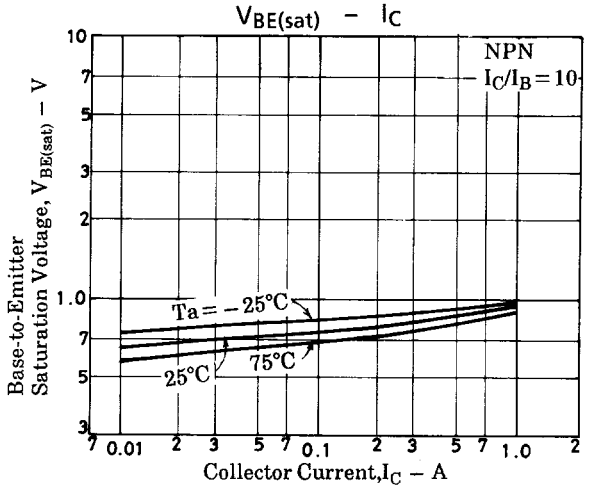
h_{FE} – I_C



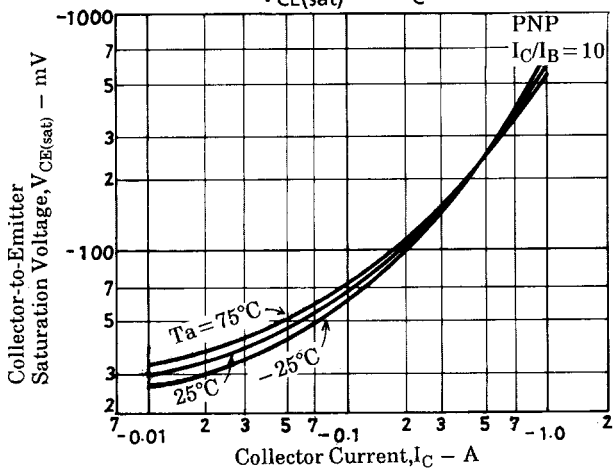
$V_{BE(sat)}$ – I_C



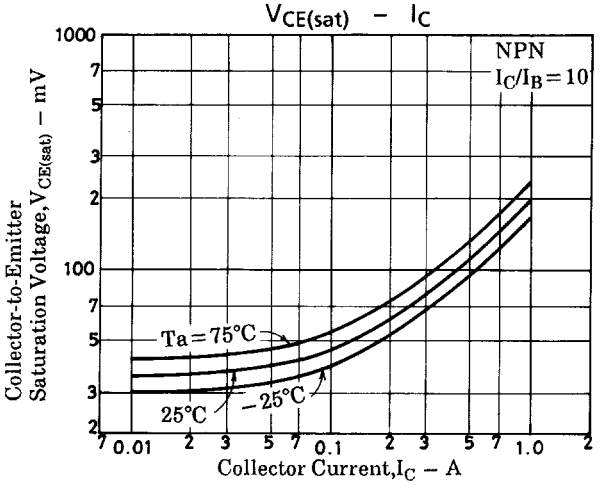
$V_{BE(sat)}$ – I_C



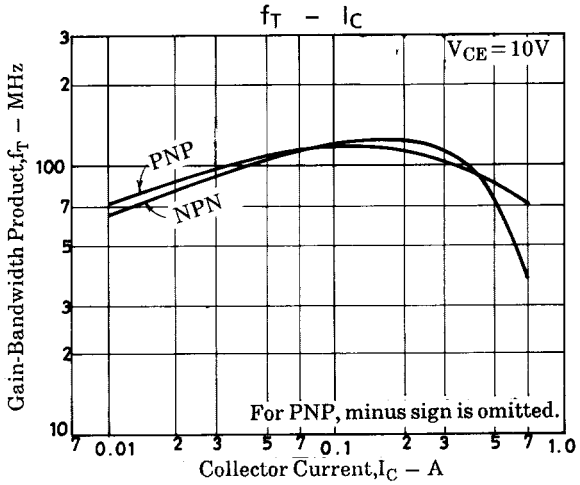
$V_{CE(sat)}$ – I_C



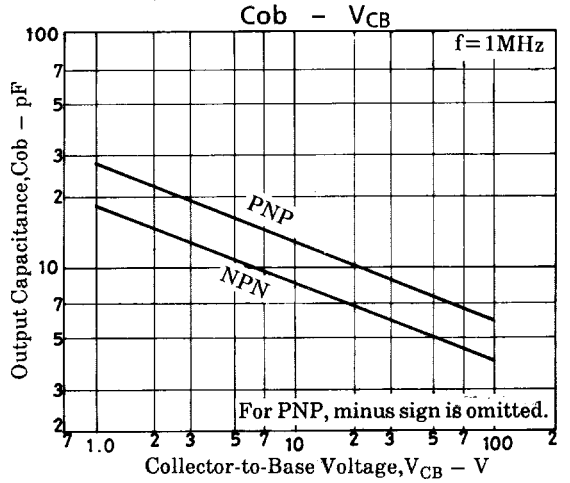
$V_{CE(sat)}$ – I_C



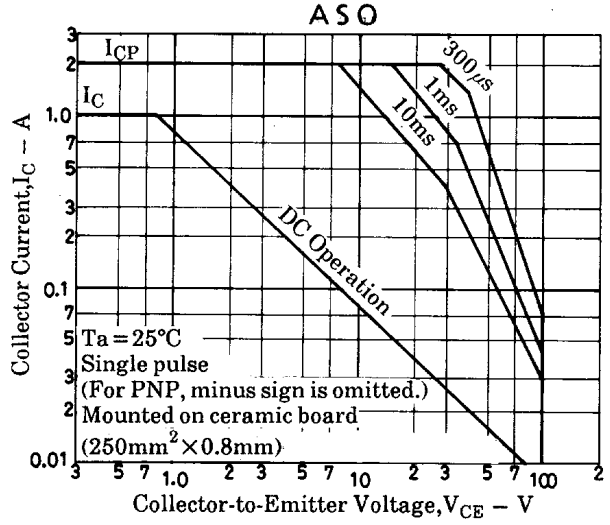
f_T – I_C



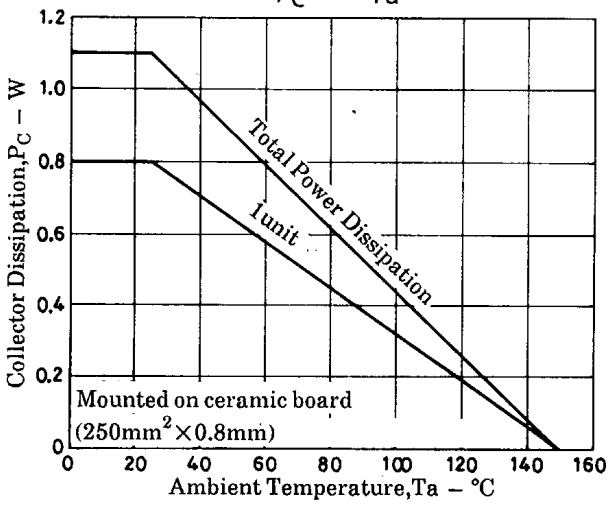
Cob – V_{CB}



ASO



PC – Ta



PC (NPN) – PC (PNP)