

25A, 100V, 0.150 Ohm, P-Channel Power MOSFET

This advanced power MOSFET is designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. It is a P-Channel enhancement mode silicon-gate power field effect transistor designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

The P-Channel IRFP9150 is an approximate electrical complement to the N-channel IRFP150.

Formerly developmental type TA49230.

Ordering Information

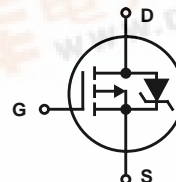
PART NUMBER	PACKAGE	BRAND
IRFP9150	TO-247	IRFP9150

NOTE: When ordering, use the entire part number.

Features

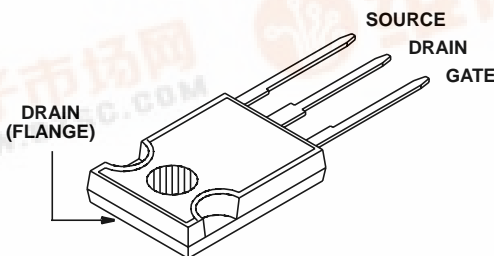
- 25A, 100V
- $r_{DS(ON)} = 0.150\Omega$
- Single Pulse Avalanche Energy Rated
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

Symbol



Packaging

JEDEC STYLE TO-247



IRFP9150

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

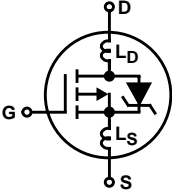
	IRFP9150	UNITS
Drain to Source Voltage (Note 1)	V_{DS}	-100 V
Drain to Gate Voltage ($R_{GS} = 10\text{k}\Omega$) (Note 1)	V_{DGR}	-100 V
Continuous Drain Current	I_D	-25 A
$T_C = 100^\circ\text{C}$	I_D	-18 A
Pulsed Drain Current	I_{DM}	-100 A
Gate to Source Voltage	V_{GS}	± 20 V
Maximum Power Dissipation	P_D	150 W
Linear Derating Factor		1.2 W/ $^\circ\text{C}$
Single Pulse Avalanche Energy Rating (Note 3)	E_{as}	1300 mJ
Operating and Storage Temperature	T_J, T_{STG}	-55 to 150 $^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	T_L	300 $^\circ\text{C}$
Package Body for 10s, See Techbrief 334	T_{pkg}	260 $^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- $T_J = 25^\circ\text{C}$ to 125°C

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Drain to Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$ (Figure 10)	1	-	-	V	
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-2.0	-	-4.0	V	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}$	-	-	25	μA	
		$V_{DS} = 0.8 \times \text{Rated } BV_{DSS}, V_{GS} = 0\text{V}, T_C = 125^\circ\text{C}$	-	-	250	μA	
On-State Drain Current (Note 2)	$I_{D(ON)}$	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10\text{V}$	-25	-	-	A	
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA	
Drain to Source On Resistance (Note 2)	$r_{DS(ON)}$	$V_{GS} = -10\text{V}, I_D = -10\text{A}$ (Figure 8, 9)	-	0.090	0.150	Ω	
Forward Transconductance (Note 2)	g_{fs}	$V_{DS} \leq -10\text{V}, I_D = -12.5\text{A}$ (Figure 12)	4	10	-	S	
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = -50\text{V}, I_D \approx -25\text{A}, R_G = 6.8\Omega, R_L = 2\Omega$ (Figures 17 and 18) MOSFET switching times are essentially independent of operating temperature).	-	16	24	ns	
Rise Time	t_r		-	110	160	ns	
Turn-Off Delay Time	$t_{d(OFF)}$		-	65	100	ns	
Fall Time	t_f		-	46	70	ns	
Total Gate Charge (Gate to Source + Gate to Drain)	$Q_{g(TOT)}$	$V_{GS} = -10\text{V}, I_D = -25\text{A}, V_{DS} = 0.8 \times \text{Rated } BV_{DSS}$ $I_{g(REF)} = -1.5\text{mA}$ (Figures 14, 19, 20) (Gate Charge is Essentially Independent Of Operating Temperature)	-	82	120	nC	
Gate to Source Charge	Q_{gs}		-	14	-	nC	
Gate to Drain "Miller" Charge	Q_{gd}		-	42	-	nC	
Input Capacitance	C_{ISS}		$V_{GS} = 0\text{V}, V_{DS} = -25\text{V}, f = 1.0\text{MHz}$ (Figure 11)	-	2400	-	pF
Output Capacitance	C_{OSS}		-	850	-	pF	
Reverse Transfer Capacitance	C_{RSS}		-	400	-	pF	
Internal Drain Inductance	L_D		Measured From the Drain Lead, 6mm (0.25in) From the Package to the Center of the Die	-	5.0	-	nH
Internal Source Inductance	L_S	Measured From the Source Pin, 6mm (0.25in) From Header to the Source Bonding Pad	-	13	-	nH	
							
Thermal Resistance Junction to Case	$R_{\theta JC}$		-	-	0.83	$^\circ\text{C/W}$	
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation	-	-	30	$^\circ\text{C/W}$	

IRFP9150

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I_{SD}	Modified MOSFET Symbol Showing the Integral Reverse P-N Junction Diode	-	-	-25	A
Pulse Source to Drain Current (Note 3)	I_{SDM}		-	-	-100	A
Source to Drain Diode Voltage (Note 2)	V_{SD}	$T_J = 25^\circ\text{C}$, $I_{SD} = -25\text{A}$, $V_{GS} = 0\text{V}$ (Figure 13)	-	-0.9	-1.5	V
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ\text{C}$, $I_{SD} = -25\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	150	300	ns
Reverse Recovered Charge	Q_{RR}	$T_J = 25^\circ\text{C}$, $I_{SD} = -25\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	0.3	0.7	1.5	μC

NOTES:

- Pulse test: pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Repetitive Rating: Pulse width limited by Maximum junction temperature. See Transient Thermal Impedance curve (Figure 3)
- $V_{DD} = 25\text{V}$, start $T_J = 25^\circ\text{C}$, $L = 3.2\text{mH}$, $R_G = 25\Omega$, peak $I_{AS} = 25\text{A}$ (Figures 15, 16).

Typical Performance Curves Unless Otherwise Specified

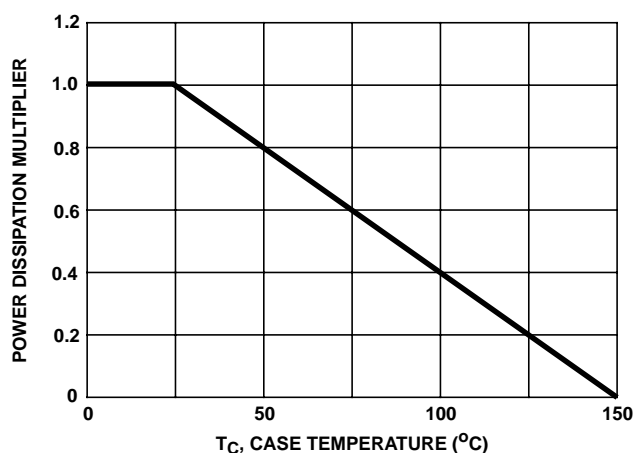


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

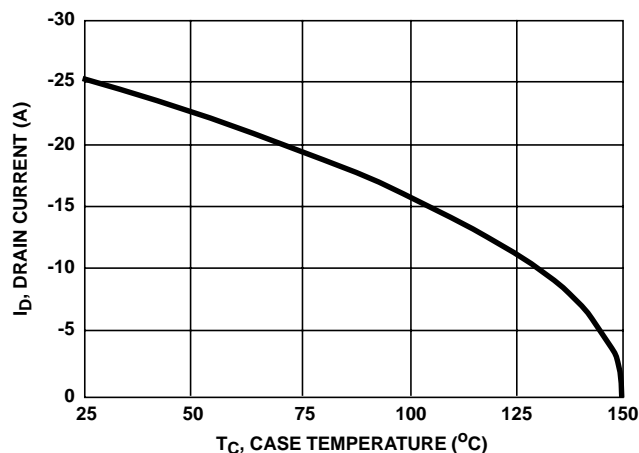


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

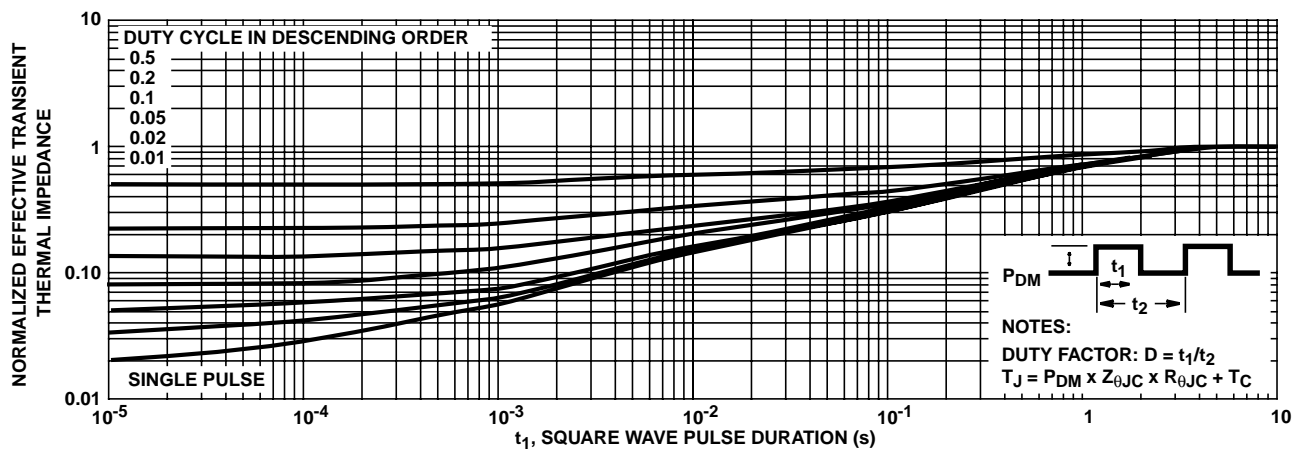


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

IRFP9150

Typical Performance Curves Unless Otherwise Specified (Continued)

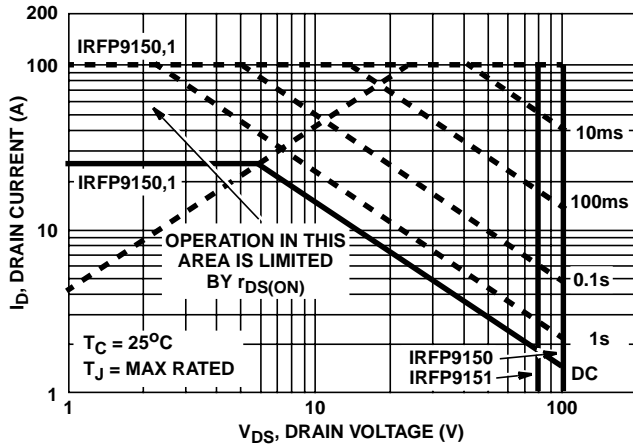


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

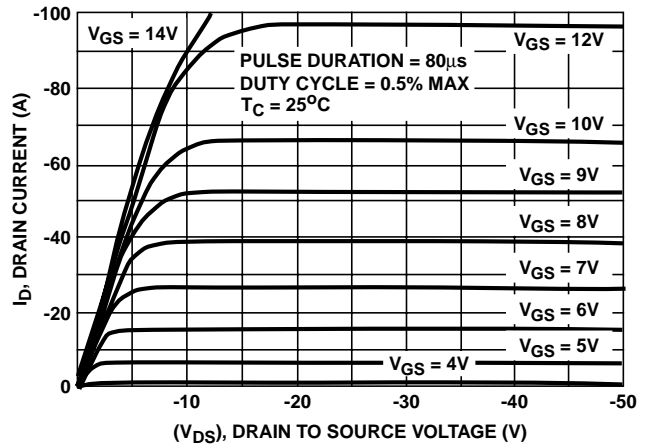


FIGURE 5. OUTPUT CHARACTERISTICS

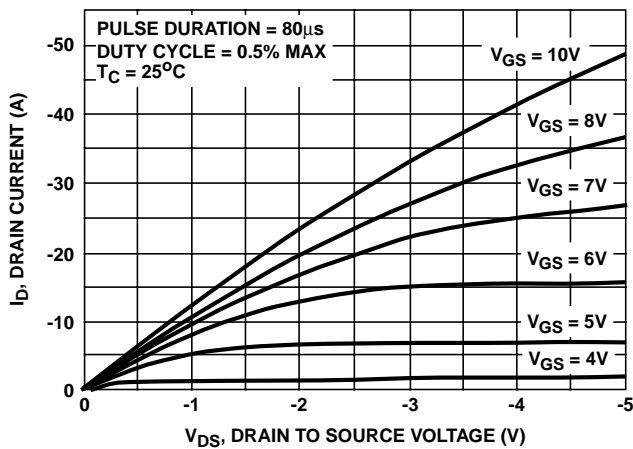


FIGURE 6. SATURATION CHARACTERISTICS

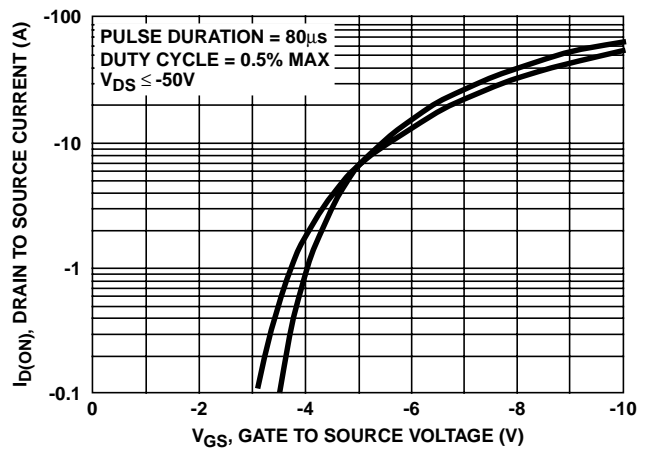


FIGURE 7. TRANSFER CHARACTERISTICS

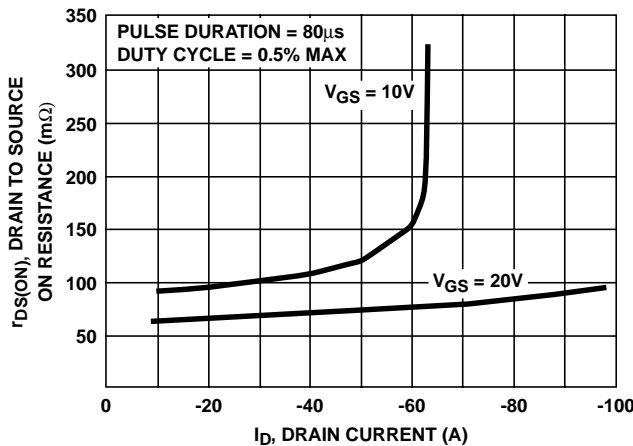


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

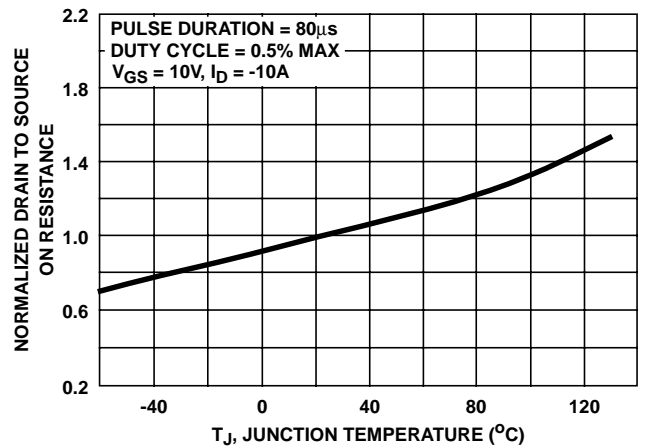


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

IRFP9150

Typical Performance Curves Unless Otherwise Specified (Continued)

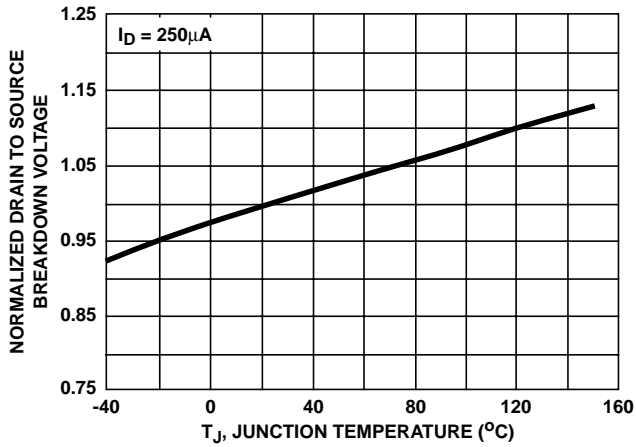


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

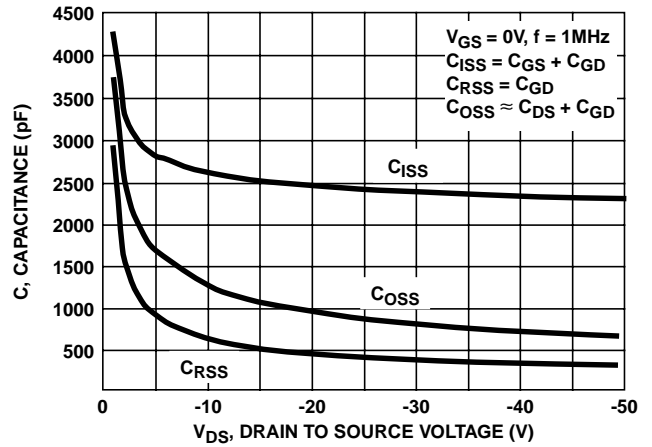


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

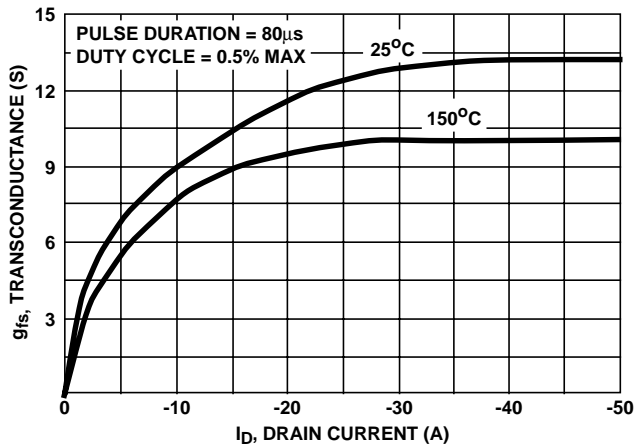


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

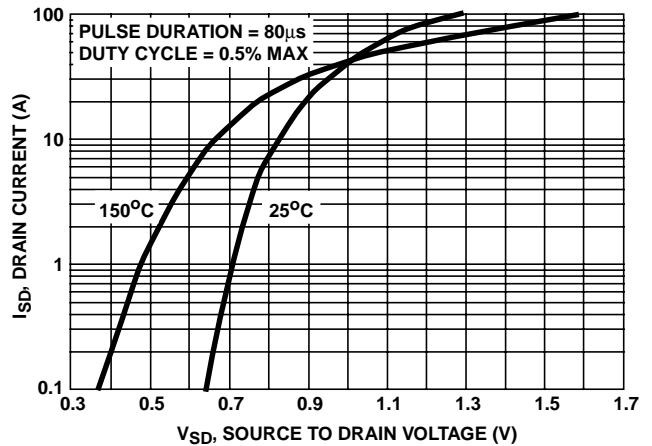


FIGURE 13. SOURCE TO DRAIN DIODE VOLTAGE

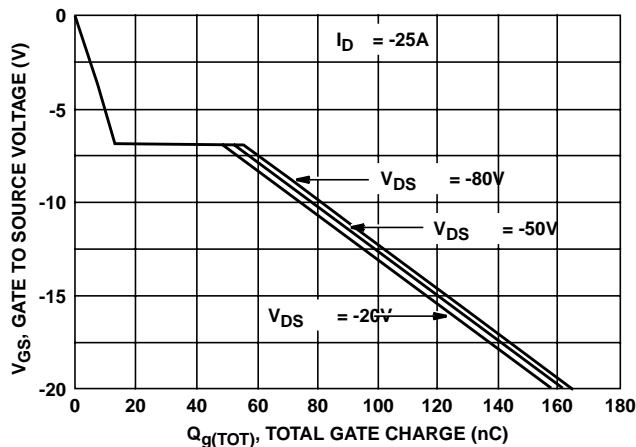


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

Test Circuits and Waveforms

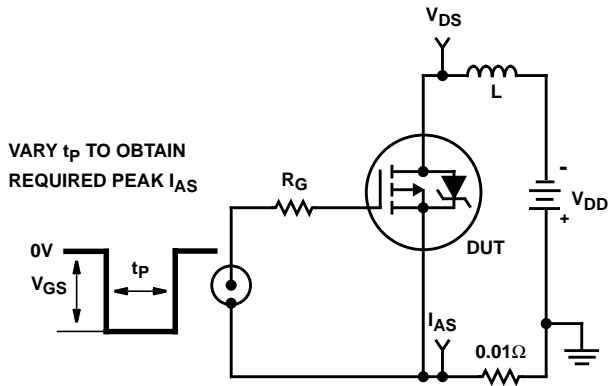


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

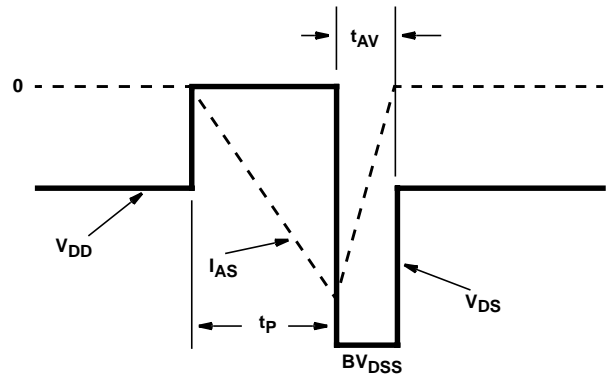


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

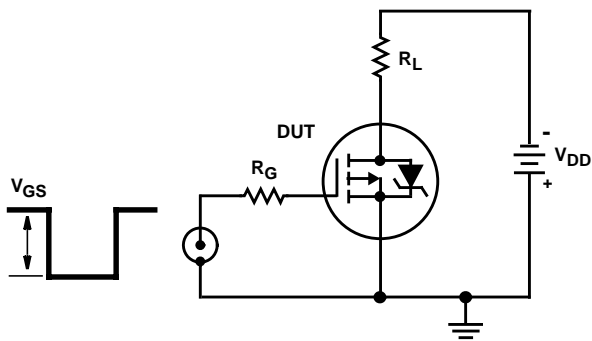


FIGURE 17. SWITCHING TIME TEST CIRCUIT

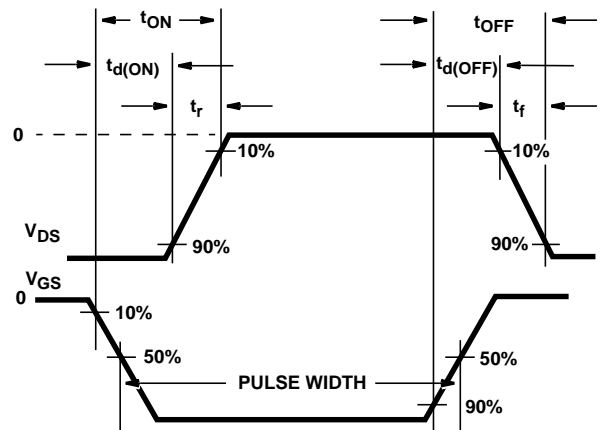


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

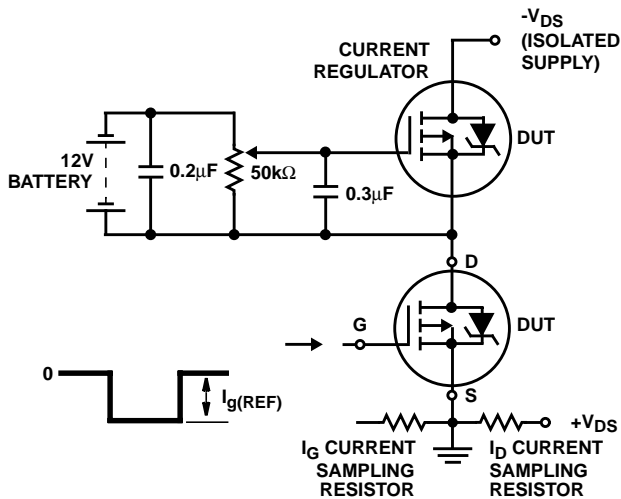


FIGURE 19. GATE CHARGE TEST CIRCUIT

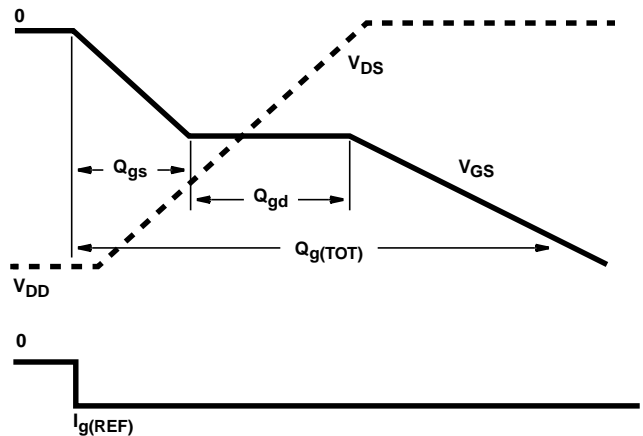


FIGURE 20. GATE CHARGE WAVEFORMS

IRFP9150

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>

Sales Office Headquarters

NORTH AMERICA

Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE

Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029