



FPAL15SL60

Smart Power Module (SPM)

General Description

FPAL15SL60 is an advanced smart power module (SPM) that Fairchild has newly developed and designed to provide very compact and low cost, yet high performance ac motor drives mainly targeting low speed low-power inverter-driven application like air conditioners. It combines optimized circuit protection and drive matched to low-loss IGBTs. Highly effective short-circuit current detection/protection is realized through the use of advanced current sensing IGBT chips that allow continuous monitoring of the IGBTs current. System reliability is further enhanced by the built-in over-temperature and integrated under-voltage lock-out protection. The high speed built-in HVIC provides opto-coupler-less IGBT gate driving capability that further reduce the overall size of the inverter system design. In addition the incorporated HVIC facilitates the use of single-supply drive topology enabling the FPAL15SL60 to be driven by only one drive supply voltage without negative bias.

Features

- UL Certified No. E209204
- 600V-15A 3-phase IGBT inverter bridge including control ICs for gate driving and protection
- Single-grounded power supply due to built-in HVIC
- Typical switching frequency of 3kHz
- Built-in thermistor for over-temperature monitoring
- Inverter power rating of 1kW / 100~253 Vac
- Isolation rating of 2500Vrms/min.
- Very low leakage current due to using ceramic substrate
- Adjustable current protection level by varying series resistor value with sense-IGBTs

Applications

- AC 100V ~ 253V three-phase inverter drive for small power (1kW) ac motor drives
- Home appliances applications requiring low switching frequency operation like air conditioners drive system
- Application ratings:
 - Power : 1kW / 100~253 Vac
 - Switching frequency : Typical 3kHz (PWM Control)
 - 100% load current : 7.0A (Irms)

External View and Marking Information

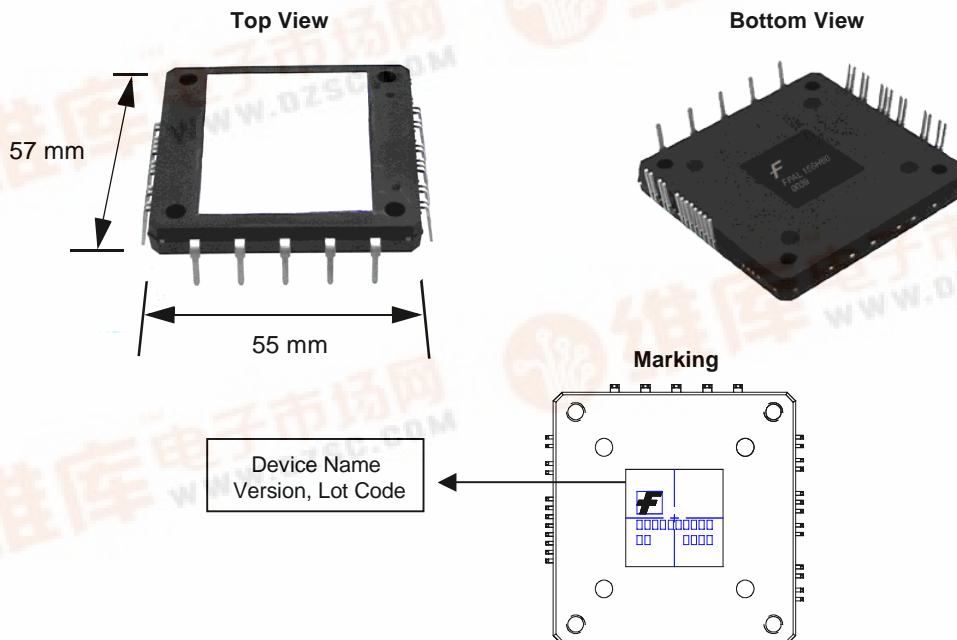


Fig. 1.



Integrated Power Functions

- 600V-15A IGBT inverter for three-phase DC/AC power conversion (Please refer to Fig. 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
Control circuit under-voltage (UV) protection
Note) Available bootstrap circuit example is given in Figs. 11, 16 and 17.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
Control supply circuit under-voltage (UV) protection
- Temperature Monitoring: System over-temperature monitoring using built-in thermistor
Note) Available temperature monitoring circuit is given in Fig. 17.
- Fault signaling: Corresponding to a SC fault (Low-side IGBTs) or a UV fault (Low-side supply)
- Input interface: 5V CMOS/LSTTL compatible, Schmitt trigger input

Pin Configuration

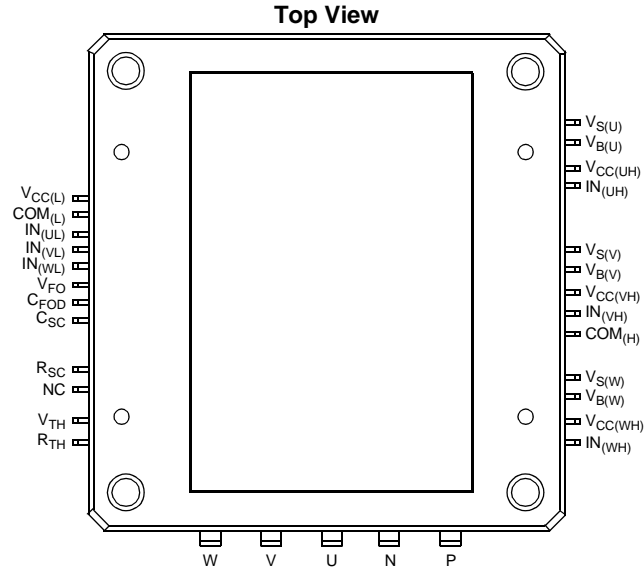


Fig. 2.

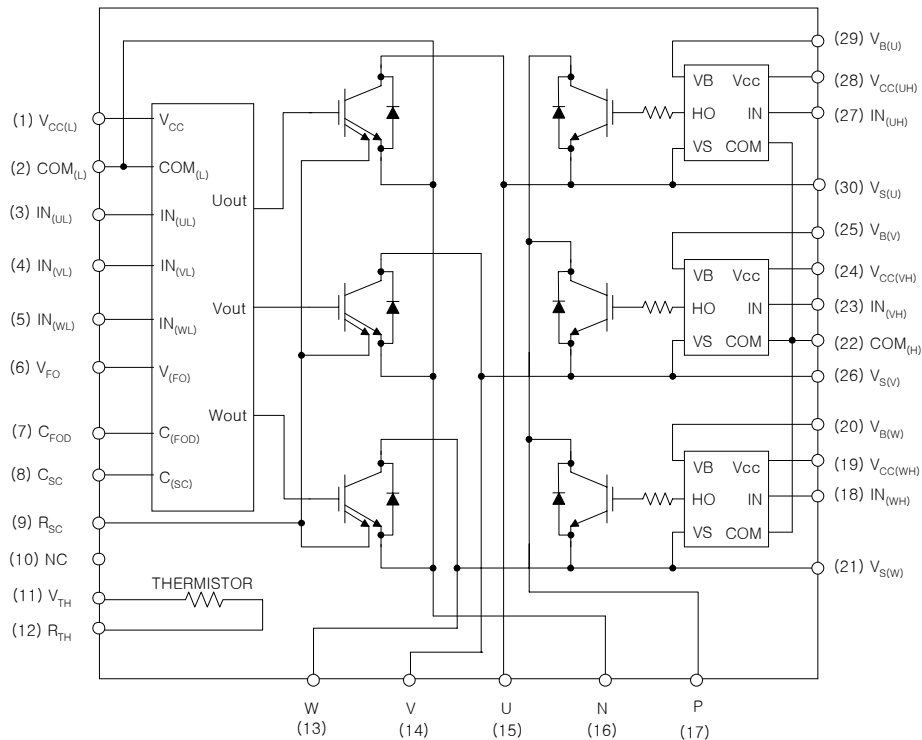
Pin Descriptions

| Pin Number | Pin Name | Pin Description |
|------------|-------------|---|
| 1 | $V_{CC(L)}$ | Low-side Common Bias Voltage for IC and IGBTs Driving |
| 2 | $COM_{(L)}$ | Low-side Common Supply Ground |
| 3 | $IN_{(UL)}$ | Signal Input Terminal for Low-side U Phase |
| 4 | $IN_{(VL)}$ | Signal Input Terminal for Low-side V Phase |
| 5 | $IN_{(WL)}$ | Signal Input Terminal for Low-side W Phase |
| 6 | V_{FO} | Fault Output Terminal |
| 7 | C_{FOD} | Capacitor for Fault Output Duration Time Selection |
| 8 | C_{SC} | Capacitor (Low-pass Filter) for Short-current Detection Input |
| 9 | R_{SC} | Resistor for Short-circuit Current Detection |
| 10 | NC | NO Connection |
| 11 | V_{TH} | Thermistor Bias Voltage |
| 12 | R_{TH} | Series Resistor for the Use of Thermistor (Temperature Detection) |
| 13 | W | Output Terminal for W Phase |
| 14 | V | Output Terminal for V Phase |
| 15 | U | Output Terminal for U Phase |

Pin Descriptions (Continued)

| Pin Number | Pin Name | Pin Description |
|------------|---------------------|--|
| 16 | N | Negative DC-Link Input |
| 17 | P | Positive DC-Link Input |
| 18 | IN _(WH) | Signal Input Terminal for High-side W Phase |
| 19 | V _{CC(WH)} | High-side Bias Voltage for W Phase IC |
| 20 | V _{B(W)} | High-side Bias Voltage for W Phase IGBT Driving |
| 21 | V _{S(W)} | High-side Bias Voltage Ground for W Phase IGBT Driving |
| 22 | COM _(H) | High-side Common Supply Ground |
| 23 | IN _(VH) | Signal Input Terminal for High-side V Phase |
| 24 | V _{CC(VH)} | High-side Bias Voltage for V Phase IC |
| 25 | V _{B(V)} | High-side Bias Voltage for V Phase IGBT Driving |
| 26 | V _{S(V)} | High-side Bias Voltage Ground for V Phase IGBT Driving |
| 27 | IN _(UH) | Signal Input Terminal for High-side U Phase |
| 28 | V _{CC(UH)} | High-side Bias Voltage for U Phase IC |
| 29 | V _{B(U)} | High-side Bias Voltage for U Phase IGBT Driving |
| 30 | V _{S(U)} | High-side Bias Voltage Ground for U Phase IGBT Driving |

Internal Equivalent Circuit and Input/Output Pins



Note

1. Inverter low-side ((1) – (12) pins) is composed of three sense-IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving, current sensing and protection functions.
2. Inverter power side ((13) – (17) pins) is composed of two inverter dc-link input terminals and three inverter output terminals.
3. Inverter high-side ((18) – (30) pins) is composed of three normal-IGBTs including freewheeling diodes and three drive ICs for each IGBT.

Fig. 3.

Absolute Maximum Ratings

Inverter Part ($T_C = 25^\circ\text{C}$, Unless Otherwise Specified)

| Item | Symbol | Condition | Rating | Unit |
|------------------------------------|------------------------|--|-----------|------------------|
| Supply Voltage | V_{DC} | Applied to DC - Link | 450 | V |
| Supply Voltage (Surge) | $V_{PN(\text{Surge})}$ | Applied between P- N | 500 | V |
| Collector-emitter Voltage | V_{CES} | | 600 | V |
| Each IGBT Collector Current | $\pm I_C$ | $T_C = 25^\circ\text{C}$ (Note Fig. 4) | 15 | A |
| Each IGBT Collector Current (Peak) | $\pm I_{CP}$ | $T_C = 25^\circ\text{C}$ (Note Fig. 4) | 30 | A |
| Collector Dissipation | P_C | $T_C = 25^\circ\text{C}$ per One Chip | 47 | W |
| Operating Junction Temperature | T_J | (Note 1) | -55 ~ 150 | $^\circ\text{C}$ |

Note

- It would be recommended that the average junction temperature should be limited to $T_J \leq 125^\circ\text{C}$ ($@T_C \leq 100^\circ\text{C}$) in order to guarantee safe operation.

Control Part ($T_C = 25^\circ\text{C}$, Unless Otherwise Specified)

| Item | Symbol | Condition | Rating | Unit |
|--------------------------------|----------|--|--------------------|------|
| Control Supply Voltage | V_{CC} | Applied between $V_{CC(H)}$ - $COM_{(H)}$, $V_{CC(L)}$ - $COM_{(L)}$ | 18 | V |
| High-side Control Bias Voltage | V_{BS} | Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$ | 20 | V |
| Input Signal Voltage | V_{IN} | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$ $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$ | -0.3 ~ 6.0 | V |
| Fault Output Supply Voltage | V_{FO} | Applied between V_{FO} - $COM_{(L)}$ | -0.3- $V_{CC}+0.5$ | V |
| Fault Output Current | I_{FO} | Sink Current at V_{FO} Pin | 5 | mA |
| Current Sensing Input Voltage | V_{SC} | Applied between C_{SC} - $COM_{(L)}$ | -0.3- $V_{CC}+0.5$ | V |

Total System

| Item | Symbol | Condition | Rating | Unit |
|--|-----------------------|---|-----------|------------------|
| Self Protection Supply Voltage Limit (Short Circuit Protection Capability) | $V_{PN(\text{PROT})}$ | Applied to DC - Link, $V_{CC} = V_{BS} = 13.5 \sim 16.5\text{V}$ $T_J = 125^\circ\text{C}$, Non-repetitive, less than $6\mu\text{s}$ | 400 | V |
| Module Case Operation Temperature | T_C | Note Fig. 4 | -20 ~ 100 | $^\circ\text{C}$ |
| Storage Temperature | T_{STG} | | -55 ~ 150 | $^\circ\text{C}$ |
| Isolation Voltage | V_{ISO} | 60Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat-sink Plate | 2500 | V_{rms} |

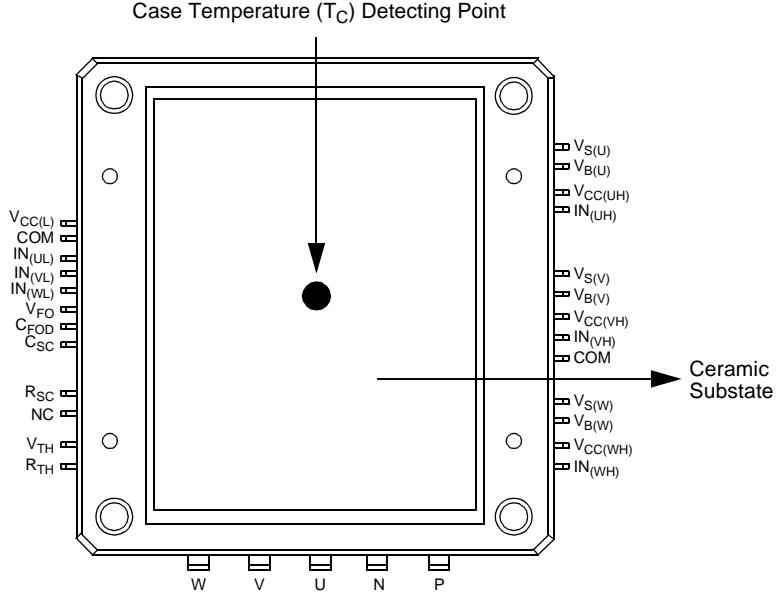


Fig. 4. T_c Measurement Point

Absolute Maximum Ratings

Thermal Resistance

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|-------------------------------------|----------------|--|------|------|------|------|
| Junction to Case Thermal Resistance | $R_{th(j-c)Q}$ | Each IGBT under Inverter Operating Condition (Note 2) | - | - | 2.61 | °C/W |
| | $R_{th(j-c)F}$ | Each FWDi under Inverter Operating Condition (Note 2) | - | - | 3.73 | °C/W |
| Contact Thermal Resistance | $R_{th(c-f)}$ | Ceramic Substrate (per 1 Module) Thermal Grease Applied | - | - | 0.06 | °C/W |

Note

2. For the measurement point of case temperature (T_c), please refer to Fig. 4.

Electrical Characteristics

Inverter Part ($T_j = 25^\circ\text{C}$, Unless Otherwise Specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | |
|--|---------------|--|---|------|------|------|----|
| Collector - emitter Saturation Voltage | $V_{CE(SAT)}$ | $V_{CC} = V_{BS} = 15\text{V}$ $V_{IN} = 0\text{V}$ | $I_C = 15\text{A}, T_j = 25^\circ\text{C}$ | - | - | 2.3 | V |
| | | | $I_C = 15\text{A}, T_j = 125^\circ\text{C}$ | - | - | 2.4 | V |
| FWDi Forward Voltage | V_{FM} | $V_{IN} = 5\text{V}$ | $I_C = 15\text{A}, T_j = 25^\circ\text{C}$ | - | - | 2.5 | V |
| | | | $I_C = 15\text{A}, T_j = 125^\circ\text{C}$ | - | - | 2.3 | V |
| Switching Times | t_{ON} | $V_{PN} = 300\text{V}, V_{CC} = V_{BS} = 15\text{V}$ $I_C = 15\text{A}, T_j = 25^\circ\text{C}$ $V_{IN} = 5\text{V} \leftrightarrow 0\text{V}$, Inductive Load (High-Low Side) | - | 0.39 | - | us | |
| | $t_{C(ON)}$ | | - | 0.12 | - | us | |
| | t_{OFF} | | - | 1.0 | - | us | |
| | $t_{C(OFF)}$ | | - | 0.6 | - | us | |
| | t_{rr} | | (Note 3) | - | 0.1 | - | us |
| Collector - emitter Leakage Current | I_{CES} | $V_{CE} = V_{CES}, T_j = 25^\circ\text{C}$ | - | - | 250 | uA | |

Note

3. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Fig. 5.

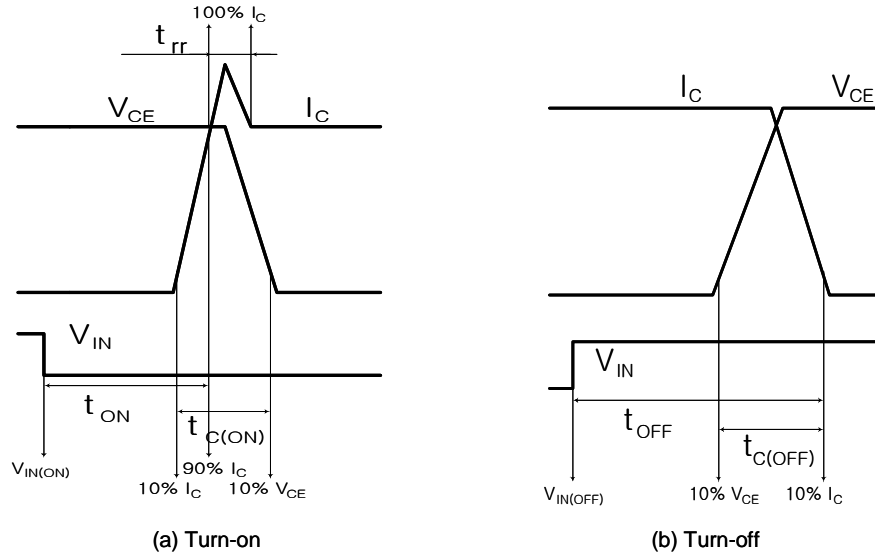


Fig. 5. Switching Time Definition

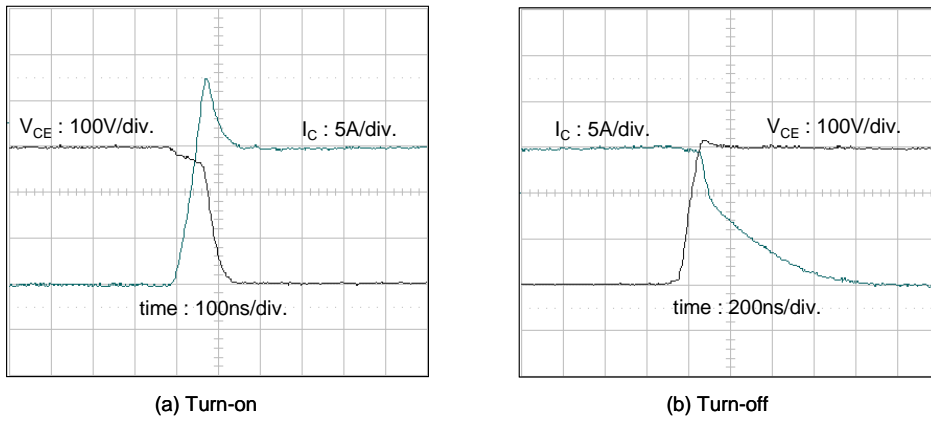


Fig. 6. Experimental Results of Switching Waveforms
 Test Condition: $V_{dc}=300V$, $V_{cc}=15V$, $L=500\mu H$ (Inductive Load), $T_C=25^\circ C$

Electrical Characteristics

Control Part ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | |
|--|---------------|--|--|------|------|------------|----|
| Control Supply Voltage | V_{CC} | Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM | 13.5 | 15 | 16.5 | V | |
| High-side Bias Voltage | V_{BS} | Applied between $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$ | 13.5 | 15 | 16.5 | V | |
| Quiescent V_{CC} Supply Current | I_{QCCL} | $V_{CC} = 15\text{V}$ $I_{N(UL, VL, WL)} = 5\text{V}$ | $V_{CC(L)}$ - $COM_{(L)}$ | - | - | 26 | mA |
| | I_{QCCH} | $V_{CC} = 15\text{V}$ $I_{N(UH, VH, WH)} = 5\text{V}$ | $V_{CC(U)}$, $V_{CC(V)}$, $V_{CC(W)}$ - $COM_{(H)}$ | - | - | 130 | uA |
| Quiescent V_{BS} Supply Current | I_{QBS} | $V_{BS} = 15\text{V}$ $I_{N(UH, VH, WH)} = 5\text{V}$ | $V_{B(U)} - V_{S(U)}$, $V_{B(V)} - V_{S(V)}$, $V_{B(W)} - V_{S(W)}$ | - | - | 420 | uA |
| Fault Output Voltage | V_{FOH} | $V_{SC} = 0\text{V}$, V_{FO} Circuit: 4.7k Ω to 5V Pull-up | 4.5 | - | - | V | |
| | V_{FOL} | $V_{SC} = 1\text{V}$, V_{FO} Circuit: 4.7k Ω to 5V Pull-up | - | - | 1.1 | V | |
| PWM Input Frequency | f_{PWM} | $T_C \leq 100^\circ\text{C}$, $T_J \leq 125^\circ\text{C}$ | - | 3 | - | kHz | |
| Allowable Input Signal Blanking Time considering Leg Arm-short | t_{dead} | $-20^\circ\text{C} \leq T_C \leq 100^\circ\text{C}$ | 3 | - | - | us | |
| Short Circuit Trip Level | $V_{SC(ref)}$ | $T_J = 25^\circ$, $V_{CC} = 15\text{V}$ (Note 4) | 0.45 | 0.51 | 0.56 | V | |
| Sensing Voltage of IGBT Current | V_{SEN} | $-20^\circ\text{C} \leq T_C \leq 100^\circ\text{C}$, @ $R_{SC} = 82 \Omega$ and $I_C = 15\text{A}$ (Note Fig. 8) | 0.37 | 0.45 | 0.56 | V | |
| Supply Circuit Under-Voltage Protection | UV_{CCD} | $T_J \leq 125^\circ\text{C}$ | Detection Level | 11.5 | 12 | 12.5 | V |
| | UV_{CCR} | | Reset Level | 12 | 12.5 | 13 | V |
| | UV_{BSD} | | Detection Level | 7.3 | 9.0 | 10.8 | V |
| | UV_{BSR} | | Reset Level | 8.6 | 10.3 | 12 | V |
| Fault-out Pulse Width | t_{FOD} | $V_{CC} = 15\text{V}$, $C_{(sc)} = 1\text{V}$ $C_{FOD} = 33\text{nF}$ (Note 5) | 1.4 | 1.8 | 2.0 | ms | |
| ON Threshold Voltage | $V_{IN(ON)}$ | High-Side | Applied between $I_{N(UH)}$, $I_{N(VH)}$, $I_{N(WH)}$ - $COM_{(H)}$ | - | - | 0.8 | V |
| OFF Threshold Voltage | $V_{IN(OFF)}$ | | | 3.0 | - | - | V |
| ON Threshold Voltage | $V_{IN(ON)}$ | Low-Side | Applied between $I_{N(UL)}$, $I_{N(VL)}$, $I_{N(WL)}$ - $COM_{(L)}$ | - | - | 0.8 | V |
| OFF Threshold Voltage | $V_{IN(OFF)}$ | | | 3.0 | - | - | V |
| Resistance of Thermistor | R_{TH} | @ $T_C = 25^\circ\text{C}$ (Note Figs. 4 and 7) | - | 50 | - | k Ω | |
| | | @ $T_C = 80^\circ\text{C}$ (Note Figs. 4 and 7) | - | 6.3 | - | k Ω | |

Note

- Short-circuit current protection is functioning only at the low-sides. It would be recommended that the value of the external sensing resistor (R_{SC}) should be selected around 56 Ω in order to make the SC trip-level of about 20A.
Please refer to Fig. 8 which shows the current sensing characteristics according to sensing resistor R_{SC} .
- The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}[\text{F}]$

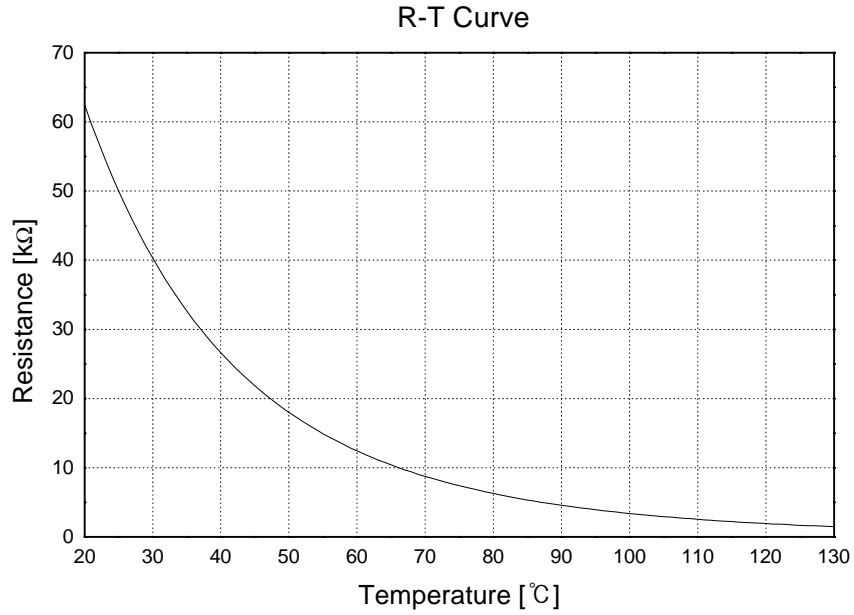


Fig. 7. R-T Curve of The Built-in Thermistor

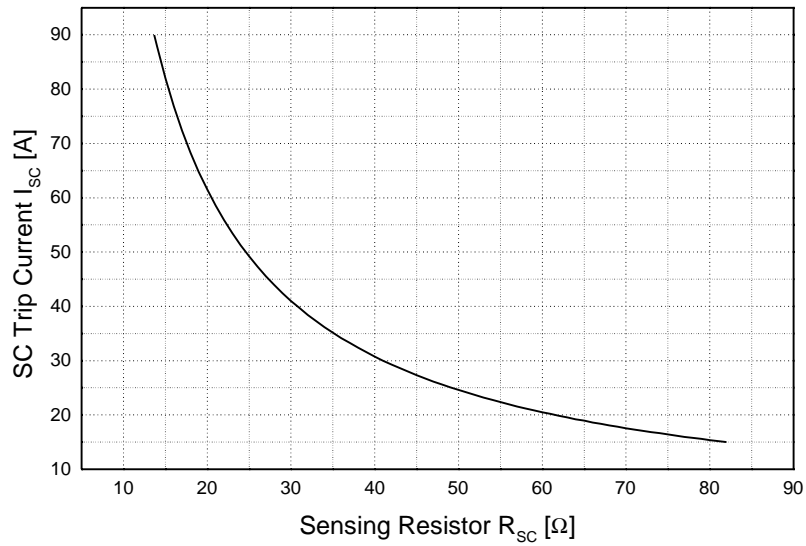


Fig. 8. Relationship between Sensing Resistor and SC Trip Current for Short-Circuit Protection
 $(I_{sc} = 82 \times \text{Rating Current}(15A) / R_{sc})$

Mechanical Characteristics and Ratings

| Item | Condition | Limits | | | Units | |
|------------------|--------------------------------------|---------------------|------|------|-------|-------|
| | | Min. | Typ. | Max. | | |
| Mounting Torque | Mounting Screw: M3 (Note 6 and 7) | Recommended 10Kg•cm | 8 | 10 | 12 | Kg•cm |
| | | Recommended 0.98N•m | 0.78 | 0.98 | 1.17 | N•m |
| Ceramic Flatness | (Note Fig. 9) | 0 | - | +100 | um | |
| Weight | | - | 56 | - | g | |

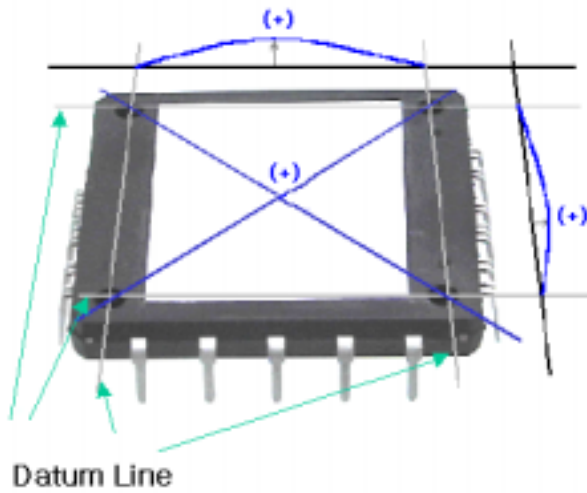


Fig. 9. Flatness Measurement Position of The Ceramic Substrate

Note

- 6. Do not make over torque or mounting screws. Much mounting torque may cause ceramic cracks and bolts and AI heat-fin destruction.
- 7. Avoid one side tightening stress. Fig.10 shows the recommended torque order for mounting screws. Uneven mounting can cause the SPM ceramic substrate to be damaged.

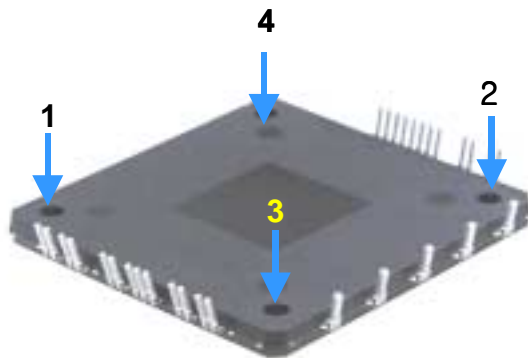
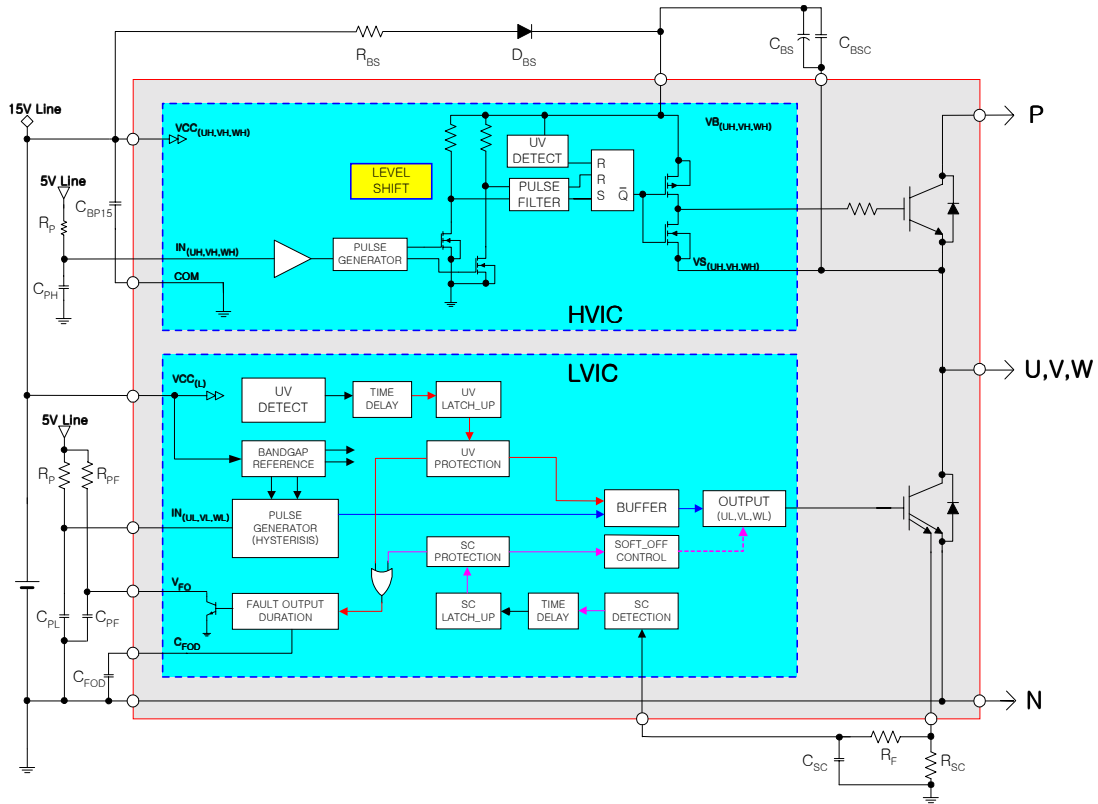


Fig. 10. Mounting Screws Torque Order (1 → 2 → 3 → 4)

Recommended Operating Conditions

| Item | Symbol | Condition | Value | | | Unit |
|--|---------------|---|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| Supply Voltage | V_{PN} | Applied between P - N | - | 300 | 400 | V |
| Control Supply Voltage | V_{CC} | Applied between $V_{CC(H)}$ - COM, $V_{CC(L)}$ - COM | 13.5 | 15 | 16.5 | V |
| High-side Bias Voltage | V_{BS} | Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$ | 13.5 | 15 | 16.5 | V |
| Blanking Time for Preventing Arm-short | t_{dead} | For Each Input Signal | 3 | - | - | us |
| PWM Input Signal | f_{PWM} | $T_C \leq 100^\circ C$, $T_J \leq 125^\circ C$ | - | 3 | - | kHz |
| Input ON Threshold Voltage | $V_{IN(ON)}$ | Applied between U_{IN} , V_{IN} , W_{IN} - COM | 0 ~ 0.65 | | | V |
| Input OFF Threshold Voltage | $V_{IN(OFF)}$ | Applied between U_{IN} , V_{IN} , W_{IN} - COM | 4 ~ 5.5 | | | V |

ICs Internal Structure and Input/Output Conditions

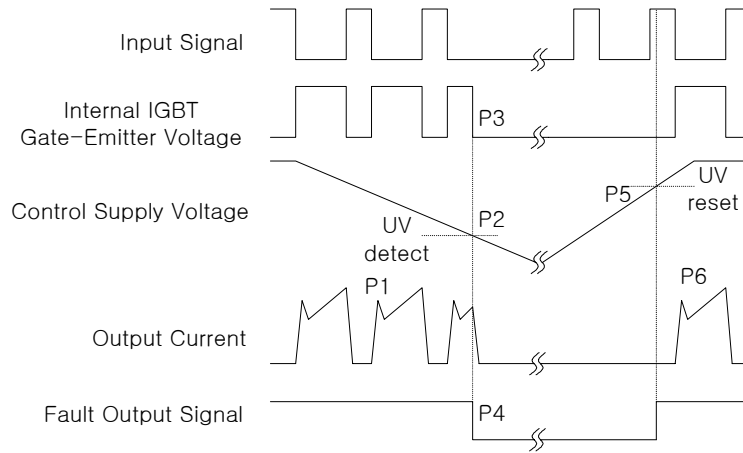


Note

1. One LVIC drives three Sense-IGBTs and can do short-circuit current protection also. Three sense emitters are commonly connected to R_{SC} terminal to detect short-circuit current. Low-side part of the inverter consists of three sense-IGBTs
2. One HVIC drives one normal-IGBT. High-side part of the inverter consists of three normal-IGBTs
3. Each IC has under voltage detection and protection function.
4. The logic input is compatible with standard CMOS or LSTTL outputs.
5. $R_P C_P$ coupling at each input/output is recommended in order to prevent the gating input/output signals oscillation and it should be as close as possible to each SPM gating input pin.
6. It would be recommended that the bootstrap diode, D_{BS} , has soft and fast recovery characteristics.

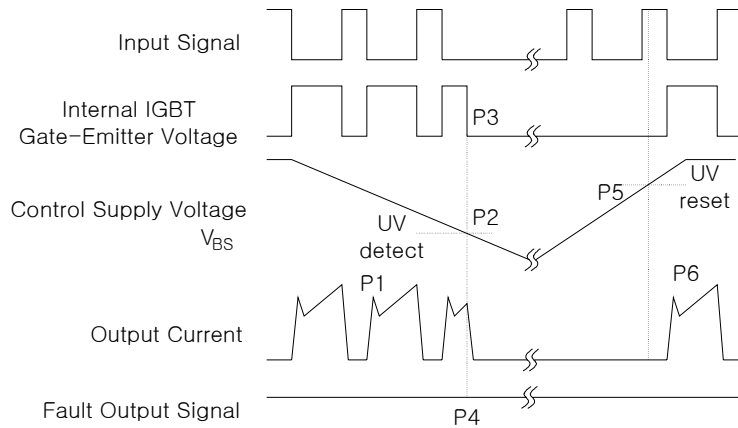
Fig. 11.

Time Charts of SPMs Protective Function



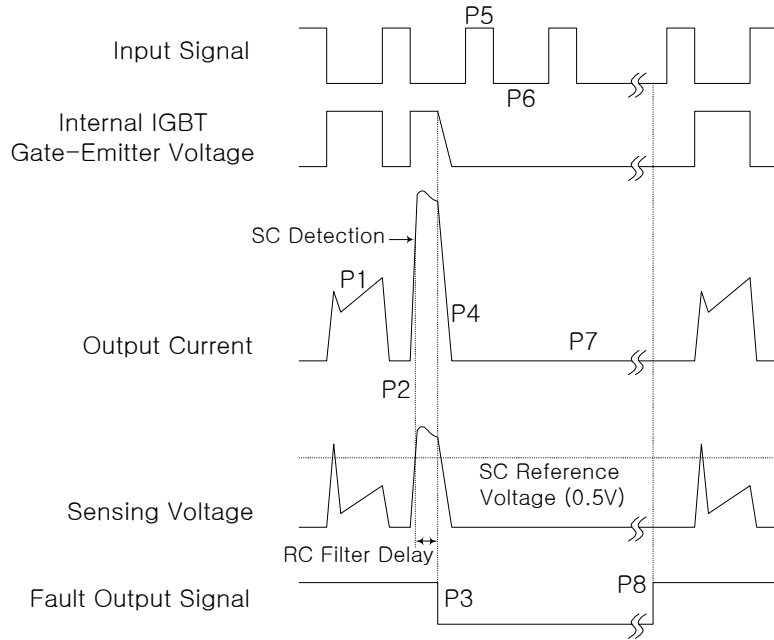
- P1 : Normal operation - IGBT ON and conducting current
- P2 : Under voltage detection
- P3 : IGBT gate interrupt
- P4 : Fault signal generation
- P5 : Under voltage reset
- P6 : Normal operation - IGBT ON and conducting current

Fig. 12. Under-Voltage Protection (Low-side)



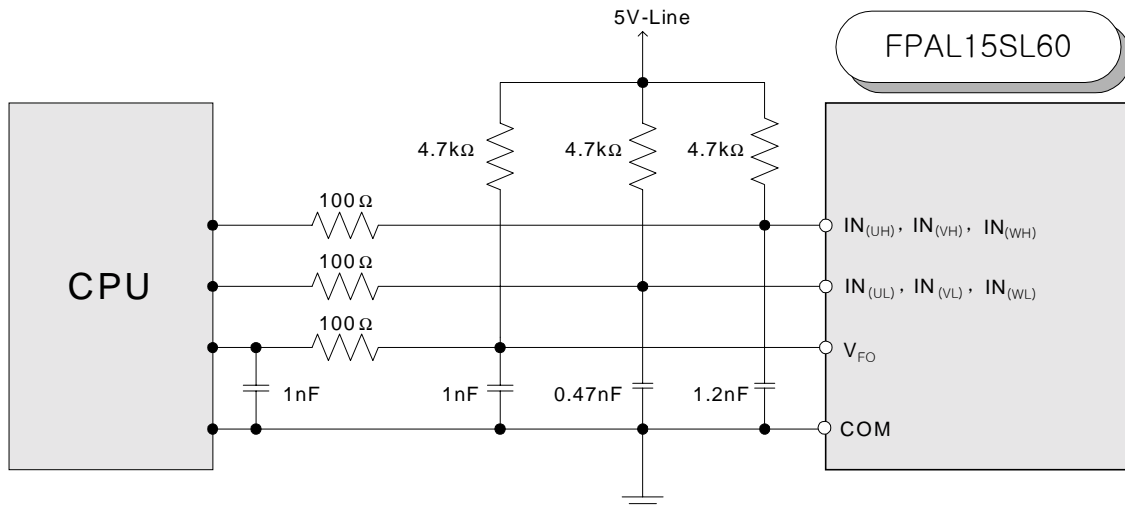
- P1 : Normal operation - IGBT ON and conducting current
- P2 : Under voltage detection
- P3 : IGBT gate interrupt
- P4 : No fault signal
- P5 : Under voltage reset
- P6 : Normal operation - IGBT ON and conducting current

Fig. 13. Under-Voltage Protection (High-side)



- P1 : Normal operation - IGBT ON and conducting currents
- P2 : Short-circuit current detection
- P3 : IGBT gate interrupt / Fault signal generation
- P4 : IGBT is slowly turned off
- P5 : IGBT OFF signal
- P6 : IGBT ON signal - but IGBT cannot be turned on during the fault-output activation
- P7 : IGBT OFF state
- P8 : Fault-output reset and normal operation start

Fig. 14. Short-circuit Current Protection (Low-side Operation only)



Note

It would be recommended that by-pass capacitors for the gating input signals, $IN_{(XX)}$ should be placed on the SPM pins and on the both sides of CPU and SPM for the fault output signal, V_{FO} , as close as possible.

Fig. 15. Recommended CPU I/O Interface Circuit

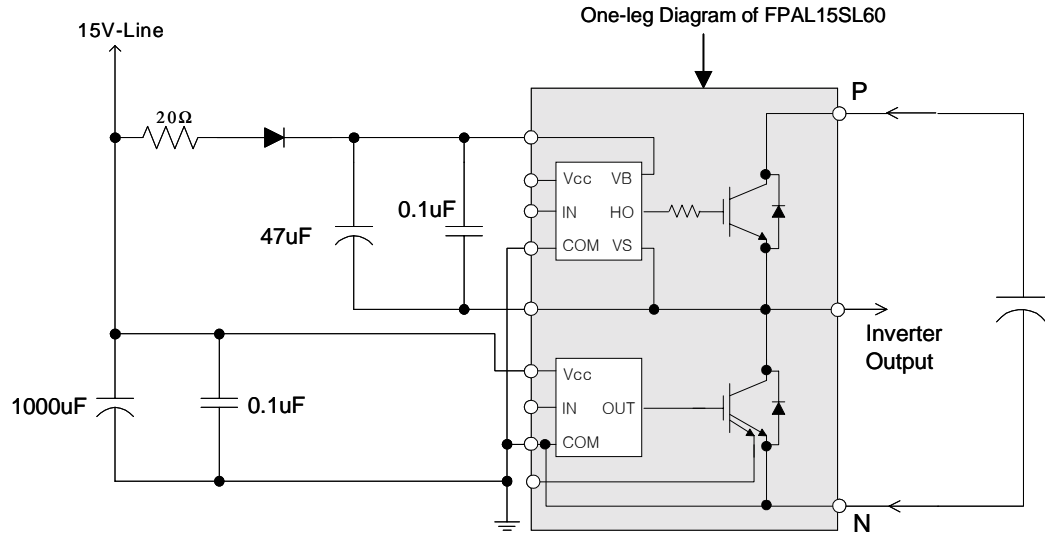
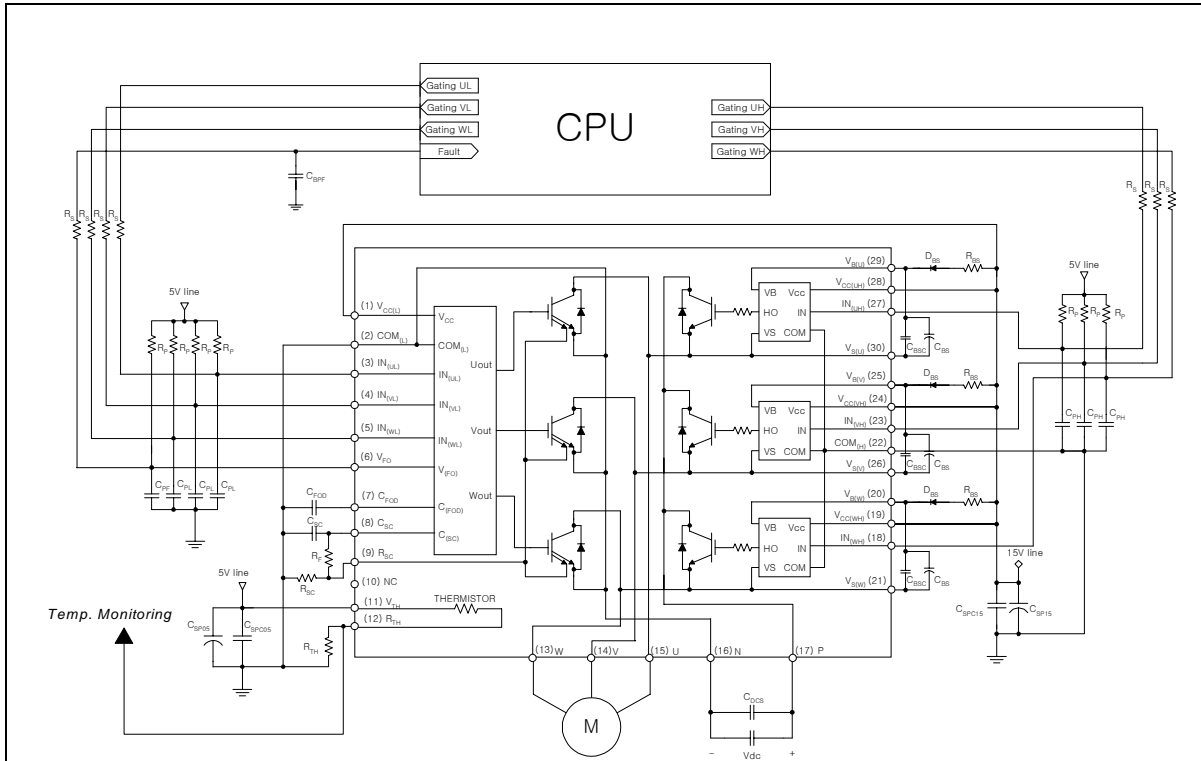


Fig. 16. Recommended Bootstrap Operation Circuit and Parameters

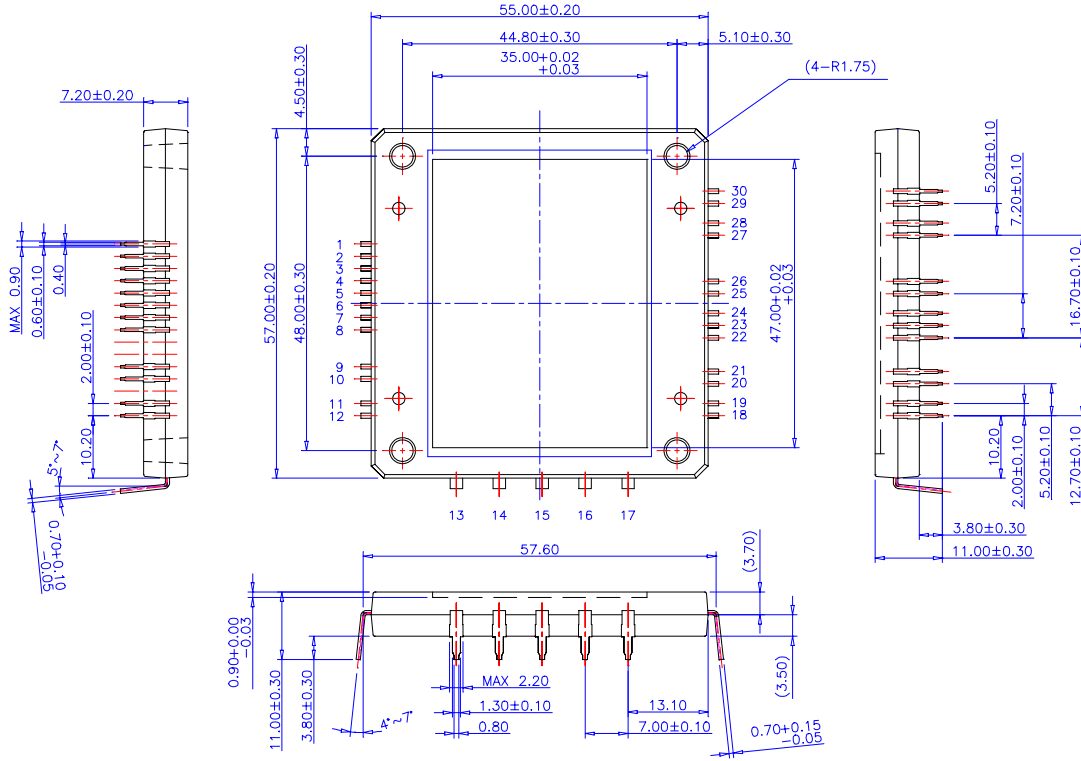


Note

1. $R_P C_{PL}/R_P C_{PH}$ coupling at each SPM input is recommended in order to prevent input signals' oscillation and it should be as close as possible to each SPM input pin.
2. By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3. V_{FO} output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7k Ω resistance. Please refer to Fig. 15.
4. C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.
5. V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD} (pin7) and $COM_{(L)}$ (pin2). (Example : if $C_{FOD} = 5.6$ nF, then $t_{FO} = 300$ μ s (typ.)) Please refer to the note 5 for calculation method.
6. Each input signal line should be pulled up to the 5V power supply with approximately 4.7k Ω resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedance of the system's printed circuit board). Approximately a 0.22-2nF by-pass capacitor should be used across each power supply connection terminals.
7. To prevent errors of the protection function, the wiring around R_{SC} , R_F and C_{SC} should be as short as possible.
8. In the short-circuit protection circuit, please select the $R_F C_{SC}$ time constant in the range 3-4 μ s. R_F should be at least 30 times larger than R_{SC} . (Recommended Example: $R_{SC} = 56$ Ω , $R_F = 3.9$ k Ω and $C_{SC} = 1$ nF)
9. Each capacitor should be mounted as close to the pins of the SPM as possible.
10. To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1-0.22 μ F between the P&N pins is recommended.
11. Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays. It is recommended that the distance be 5cm at least

Fig. 17. Application Circuit

Detailed Package Outline Drawings



FPAL15SL60

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