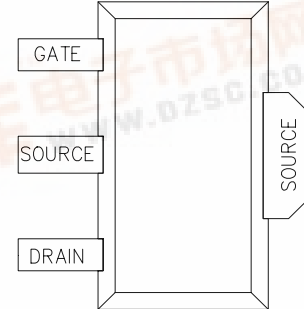




FPD3000SOT89

LOW NOISE, HIGH LINEARITY PACKAGED PHEMT

- PERFORMANCE (1850 MHz)
 - ◆ 30 dBm Output Power (P_{1dB})
 - ◆ 13 dB Small-Signal Gain (SSG)
 - ◆ 1.3 dB Noise Figure
 - ◆ 45 dBm Output IP3
 - ◆ 45% Power-Added Efficiency
 - ◆ Evaluation Boards Available
 - ◆ Available in Lead Free Finish: FPD3000SOT89E



DESCRIPTION AND APPLICATIONS

The FPD3000SOT89 is a packaged depletion mode AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT). It utilizes a $0.25 \times 3000 \mu\text{m}$ Schottky barrier Gate, defined by high-resolution stepper-based photolithography. The recessed and offset Gate structure minimizes parasitics to optimize performance, with an epitaxial structure designed for improved linearity over a range of bias conditions and input power levels. The FPD3000 is available in die form and in other packages.

Typical applications include drivers or output stages in PCS/Cellular base station high-intercept-point LNAs, WLL and WLAN systems, and other types of wireless infrastructure systems.

ELECTRICAL SPECIFICATIONS AT 22°C

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|--|--------------|---|------|-----|------|---------------|
| RF SPECIFICATIONS MEASURED AT $f = 1850 \text{ MHz}$ USING CW SIGNAL | | | | | | |
| Power at 1dB Gain Compression | P_{1dB} | $V_{DS} = 5 \text{ V}; I_{DS} = 50\% I_{DSS}$ | 29.5 | 30 | | dBm |
| Small-Signal Gain | SSG | $V_{DS} = 5 \text{ V}; I_{DS} = 50\% I_{DSS}$ | 11.5 | 13 | | dB |
| Power-Added Efficiency | PAE | $V_{DS} = 5 \text{ V}; I_{DS} = 50\% I_{DSS};$ $P_{OUT} = P_{1dB}$ | | 45 | | % |
| Noise Figure | NF | $V_{DS} = 5 \text{ V}; I_{DS} = 50\% I_{DSS}$ | | 1.3 | | dB |
| | | $V_{DS} = 5 \text{ V}; I_{DS} = 25\% I_{DSS}$ | | 0.9 | | |
| Output Third-Order Intercept Point (from 15 to 5 dB below P_{1dB}) | IP3 | $V_{DS} = 5 \text{ V}; I_{DS} = 50\% I_{DSS}$ | | 42 | | dBm |
| | | Matched for optimal power Matched for best IP3 | | 45 | | |
| Saturated Drain-Source Current | I_{DSS} | $V_{DS} = 1.3 \text{ V}; V_{GS} = 0 \text{ V}$ | 750 | 930 | 1100 | mA |
| Maximum Drain-Source Current | I_{MAX} | $V_{DS} = 1.3 \text{ V}; V_{GS} \cong +1 \text{ V}$ | | 1.5 | | A |
| Transconductance | G_M | $V_{DS} = 1.3 \text{ V}; V_{GS} = 0 \text{ V}$ | | 800 | | mS |
| Gate-Source Leakage Current | I_{GSO} | $V_{GS} = -5 \text{ V}$ | | 2 | 20 | μA |
| Pinch-Off Voltage | $ V_P $ | $V_{DS} = 1.3 \text{ V}; I_{DS} = 3 \text{ mA}$ | 0.7 | 1.0 | 1.3 | V |
| Gate-Source Breakdown Voltage | $ V_{BDGS} $ | $I_{GS} = 3 \text{ mA}$ | 12 | 16 | | V |
| Gate-Drain Breakdown Voltage | $ V_{BDGD} $ | $I_{GD} = 3 \text{ mA}$ | 12 | 16 | | V |



• ABSOLUTE MAXIMUM RATINGS¹

| Parameter | Symbol | Test Conditions | Min | Max | Units |
|---|-----------|---------------------------------|-----|-----------|-------|
| Drain-Source Voltage | V_{DS} | $-3V < V_{GS} < +0V$ | | 8 | V |
| Gate-Source Voltage | V_{GS} | $0V < V_{DS} < +8V$ | | -3 | V |
| Drain-Source Current | I_{DS} | For $V_{DS} > 2V$ | | I_{DSS} | mA |
| Gate Current | I_G | Forward or reverse current | | 30 | mA |
| RF Input Power ² | P_{IN} | Under any acceptable bias state | | 600 | mW |
| Channel Operating Temperature | T_{CH} | Under any acceptable bias state | | 175 | °C |
| Storage Temperature | T_{STG} | Non-Operating Storage | -40 | 150 | °C |
| Total Power Dissipation | P_{TOT} | See De-Rating Note below | | 3.5 | W |
| Gain Compression | Comp. | Under any bias conditions | | 5 | dB |
| Simultaneous Combination of Limits ³ | | 2 or more Max. Limits | | 80 | % |

¹ $T_{Ambient} = 22^{\circ}C$ unless otherwise noted ²Max. RF Input Limit must be further limited if input VSWR > 2.5:1

³Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.

- Total Power Dissipation defined as: $P_{TOT} \equiv (P_{DC} + P_{IN}) - P_{OUT}$, where:

P_{DC} : DC Bias Power

P_{IN} : RF Input Power

P_{OUT} : RF Output Power

- Total Power Dissipation to be de-rated as follows above $22^{\circ}C$:

$$P_{TOT} = 3.5W - (0.025W/^{\circ}C) \times T_{PACK}$$

where T_{PACK} = source tab lead temperature above $22^{\circ}C$

(coefficient of de-rating formula is the Thermal Conductivity)

Example: For a $65^{\circ}C$ source lead temperature: $P_{TOT} = 3.5W - (0.025 \times (65 - 22)) = 2.43W$

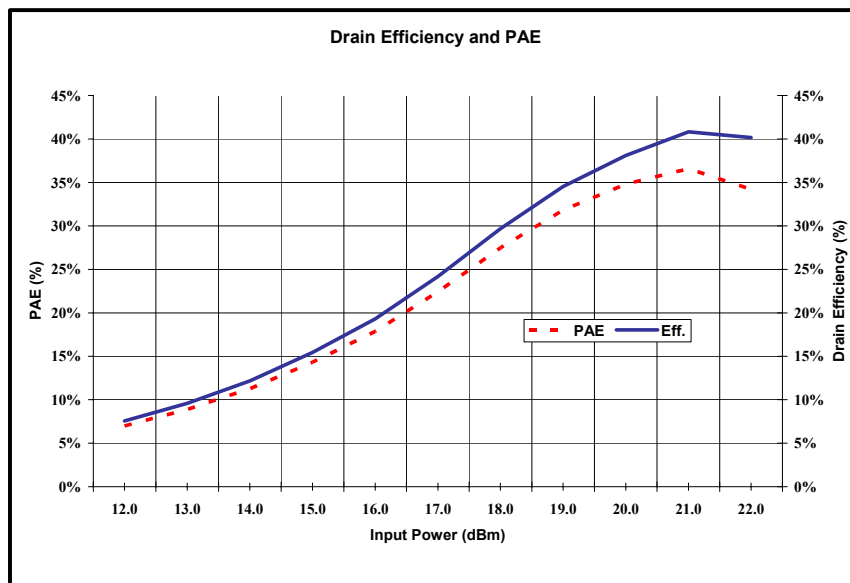
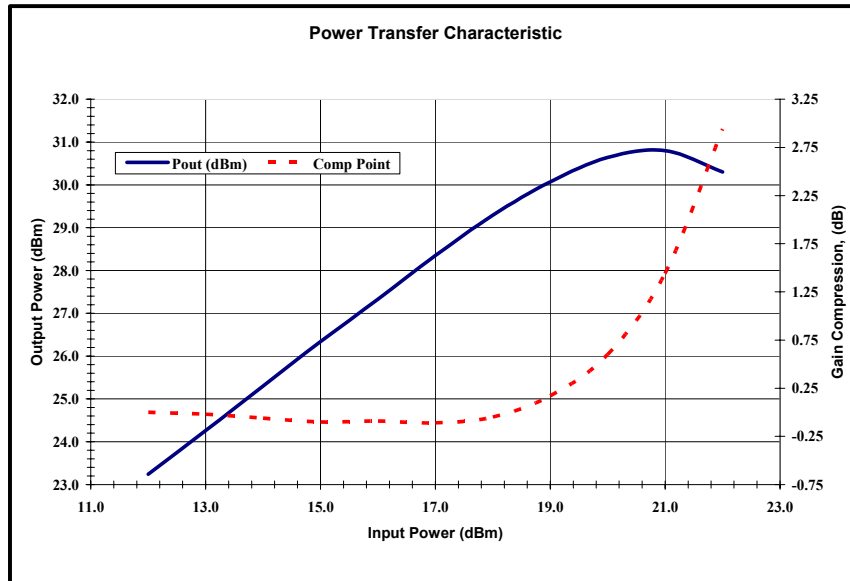
• HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. These devices should be treated as Class 1A per ESD-STM5.1-1998, Human Body Model. Further information on ESD control measures can be found in MIL-STD-1686 and MIL-HDBK-263.

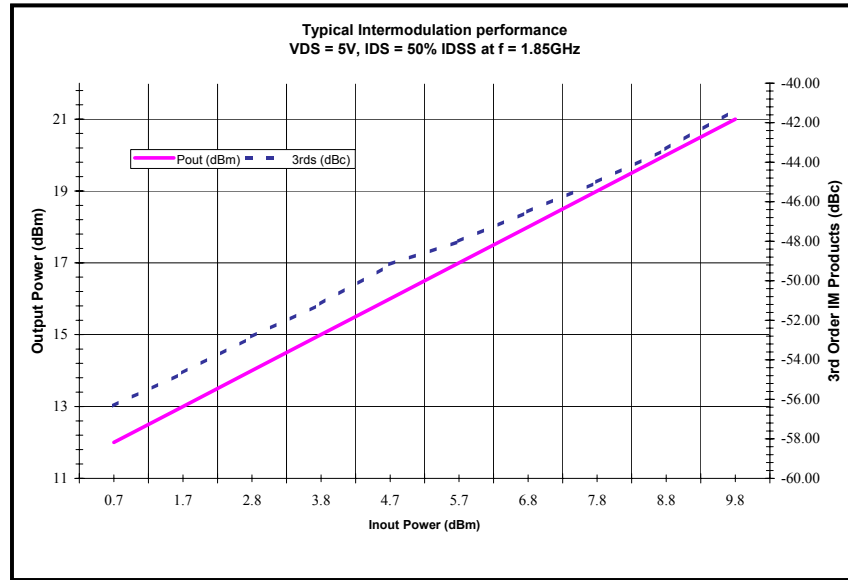
• APPLICATIONS NOTES & DESIGN DATA

Applications Notes are available from your local Filtronic Sales Representative or directly from the factory. Complete design data, including S-parameters, noise data, and large-signal models are available on the Filtronic web site. Evaluation Boards available upon request.

- TYPICAL TUNED RF PERFORMANCE

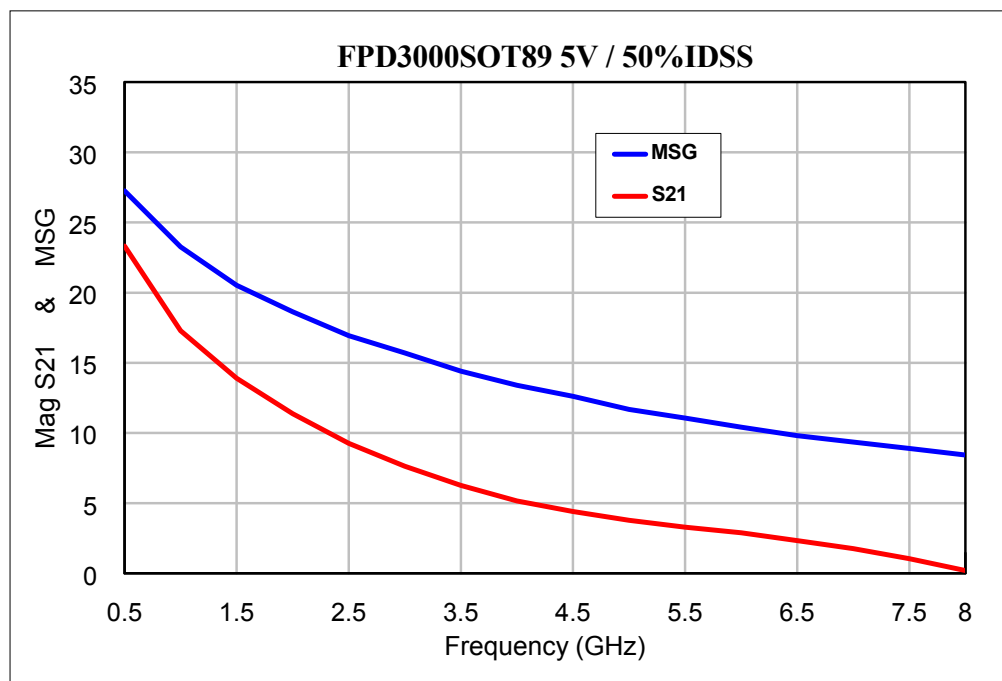


Typical power and efficiency is shown above. The devices were biased nominally at $V_{DS} = 5V$, $I_{DS} = 50\%$ of I_{DSS} , at a test frequency of 1.85 GHz. The test devices were tuned (input and output tuning) for maximum output power at 1dB gain compression.

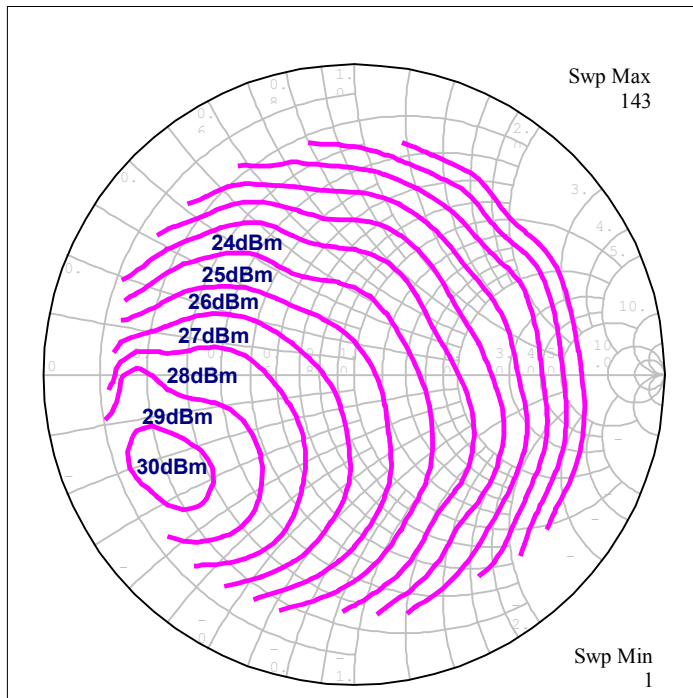


Note: pHEMT devices exhibit non-classical intermodulation performance, with equivalent IP3 values exceeding 14 dB above P_{1dB} . This IMD enhancement is affected by the quiescent bias current, the Drain-Source voltage, and the tuning or matching applied to the device.

Maximum Stable Gain & S_{21}



- TYPICAL OUTPUT PLANE POWER CONTOURS (VDS = 5V, IDS = 50% IDSS)



1850 MHz

Contours swept with a constant input power, set so that nominal P_{1dB} is achieved at the point of optimum output match.

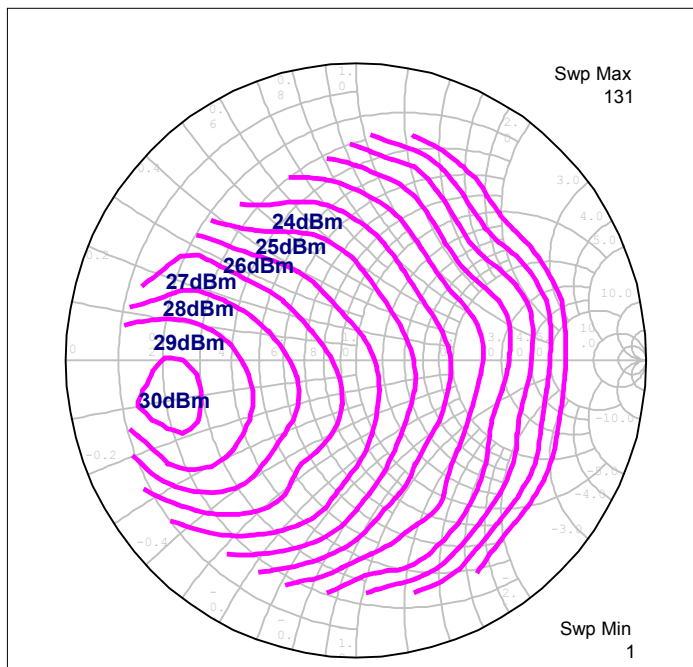
Input (Source plane) Γ_s :

$$0.70 \angle -165.5^\circ$$

$$0.17 - j0.12 \text{ (normalized)}$$

$$8.5 - j6.0 \Omega$$

Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.



900 MHz

Contours swept with a constant input power, set so that nominal P_{1dB} is achieved at the point of optimum output match.

Input (Source plane) Γ_s :

$$0.78 \angle -147.4^\circ$$

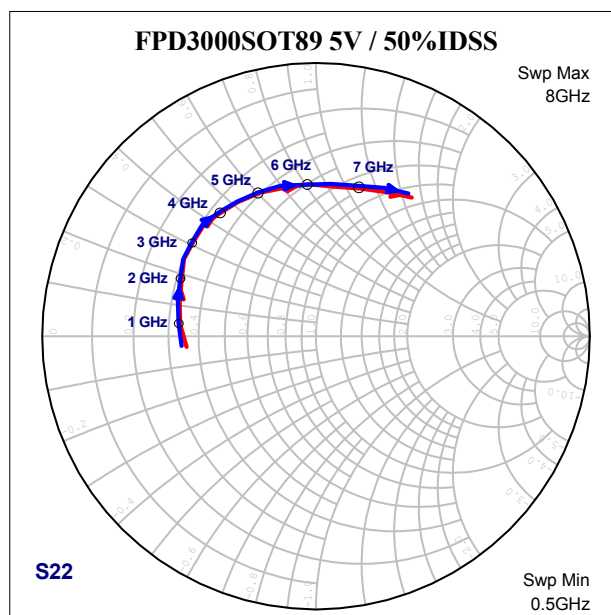
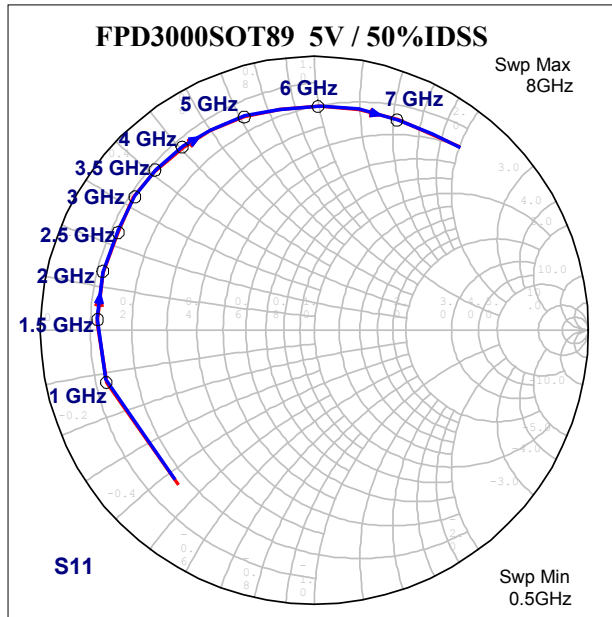
$$0.13 - j0.29 \text{ (normalized)}$$

$$6.5 - j14.5 \Omega$$

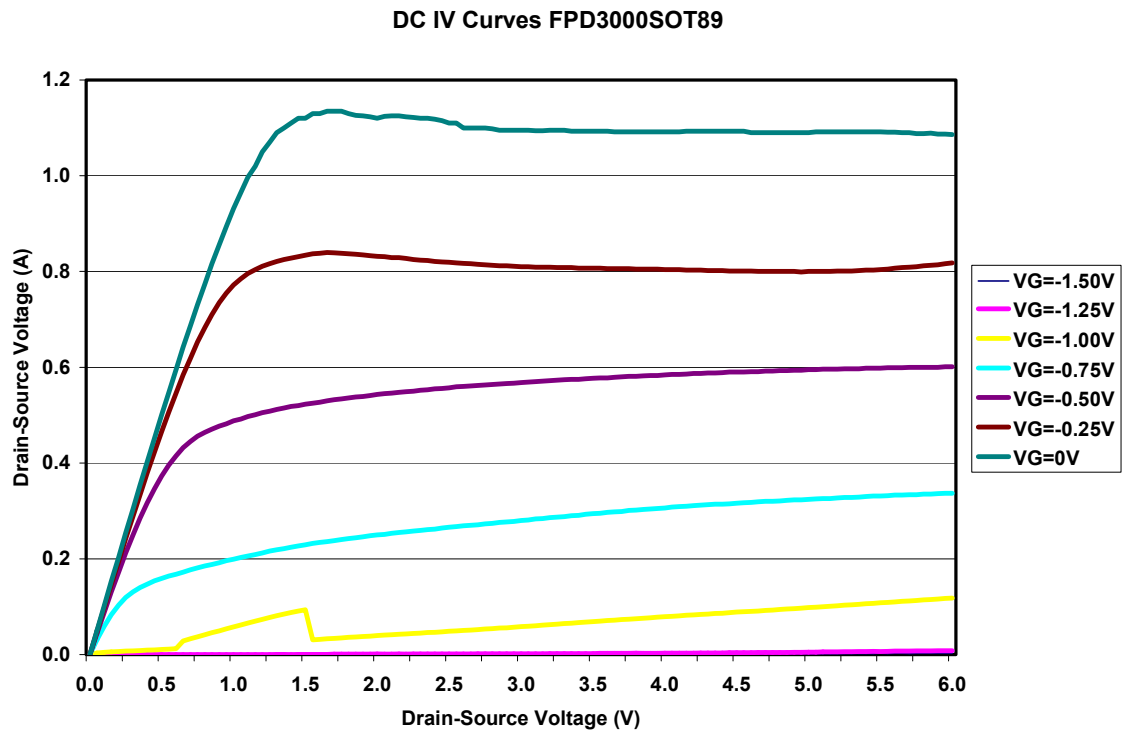
Nominal IP3 performance is obtained with this input plane match, and the output plane match as shown.

- TYPICAL SCATTERING PARAMETERS (50Ω SYSTEM)

See Website “More Info” for S-parameter design files.



- TYPICAL I-V CHARACTERISTICS



Note: The recommended method for measuring I_{DSS} , or any particular I_{DS} , is to set the Drain-Source voltage (V_{DS}) at 1.3V. This measurement point avoids the onset of spurious self-oscillation which would normally distort the current measurement (this effect has been filtered from the I-V curves presented above). Setting the $V_{DS} > 1.3V$ will generally cause errors in the current measurements, even in stabilized circuits.

Recommendation: Traditionally a device's I_{DSS} rating (I_{DS} at $V_{GS} = 0V$) was used as a predictor of RF power, and for MESFETs there is a correlation between I_{DSS} and P_{1dB} (power at 1dB gain compression). For pHEMTs it can be shown that there is *no* meaningful statistical correlation between I_{DSS} and P_{1dB} ; specifically a linear regression analysis shows $r^2 < 0.7$, and the regression fails the F-statistic test. I_{DSS} is sometimes useful as a guide to circuit tuning, since the S_{22} does vary with the quiescent operating point I_{DS} .