PD - 94630

International
IOR Rectifier

SMPS MOSFET IRFPS38N60L

HEXFET® Power MOSFET

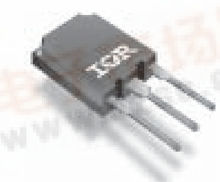
Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications

V_{DSS}	$R_{DS(on)}$ typ.	Trr typ.	I_D
600V	120mΩ	170ns	38A

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.



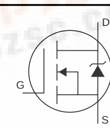
SUPER TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	38	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	24	
I_{DM}	Pulsed Drain Current ①	150	
P_D @T_C = 25°C	Power Dissipation	540	W
	Linear Derating Factor	4.3	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
dv/dt	Peak Diode Recovery dv/dt ②	13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	1.1(10)	N•m (lbf•in)

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	38	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	150		
V_{SD}	Diode Forward Voltage	——	——	1.5	V	T_J = 25°C, I_S = 38A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	170	250	ns	T_J = 25°C, I_F = 38A
		——	420	630		T_J = 125°C, di/dt = 100A/μs ④
Q_{rr}	Reverse Recovery Charge	——	830	1240	nC	T_J = 25°C, I_S = 38A, V_{GS} = 0V ④
		——	2600	3900		T_J = 125°C, di/dt = 100A/μs ④
I_{RRM}	Reverse Recovery Current	——	9.1	14	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



02/12/03

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	600	—–	—–	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—–	0.41	—–	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—–	120	150	mΩ	V_{GS} = 10V, I_D = 23A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—–	5.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	—–	—–	50	μA	V_{DS} = 600V, V_{GS} = 0V
		—–	—–	2.0	mA	V_{DS} = 480V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—–	—–	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—–	—–	-100		V_{GS} = -30V
R_G	Internal Gate Resistance	—–	1.2	—–	Ω	f = 1MHz, open drain

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	20	—–	—–	S	V_{DS} = 50V, I_D = 23A
Q_g	Total Gate Charge	—–	—–	320		I_D = 38A
Q_{gs}	Gate-to-Source Charge	—–	—–	85	nC	V_{DS} = 480V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—–	—–	160		V_{GS} = 10V, See Fig. 7 & 15 ④
$t_{d(on)}$	Turn-On Delay Time	—–	44	—–		V_{DD} = 300V
t_r	Rise Time	—–	130	—–	ns	I_D = 38A
$t_{d(off)}$	Turn-Off Delay Time	—–	92	—–		R_G = 4.3Ω
t_f	Fall Time	—–	69	—–		V_{GS} = 10V, See Fig. 11a & 11b ④
C_{iss}	Input Capacitance	—–	7990	—–		V_{GS} = 0V
C_{oss}	Output Capacitance	—–	740	—–		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—–	72	—–	pF	*ƒ* = 1.0MHz, See Fig. 5
C_{oss} eff.	Effective Output Capacitance	—–	350	—–		V_{GS} = 0V,V_{DS} = 0V to 480V ⑤
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—–	260	—–		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—–	680	mJ
I_{AR}	Avalanche Current ①	—–	38	A
E_{AR}	Repetitive Avalanche Energy ①	—–	54	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—–	0.22	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—–	°C/W
$R_{\theta JA}$	Junction-to-Ambient	—–	40	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)

② Starting T_J = 25°C, L = 0.91mH, R_G = 25Ω, I_{AS} = 38A, dv/dt = 13V/ns. (See Figure 12a)

③ $I_{SD} \leq$ 38A, di/dt ≤ 630A/μs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 150°C.

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
C_{oss} eff.(ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

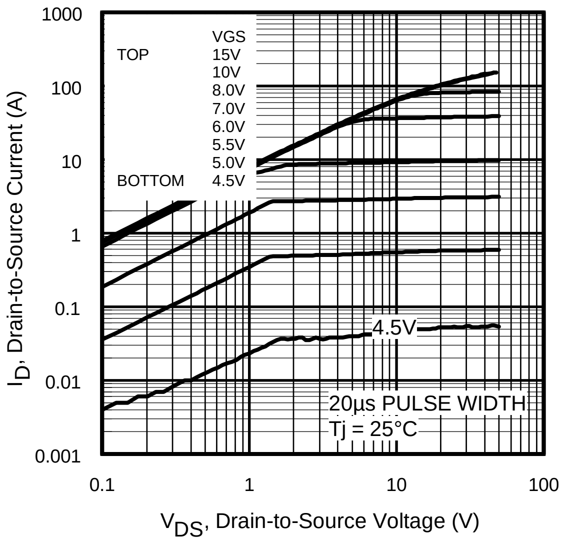


Fig 1. Typical Output Characteristics

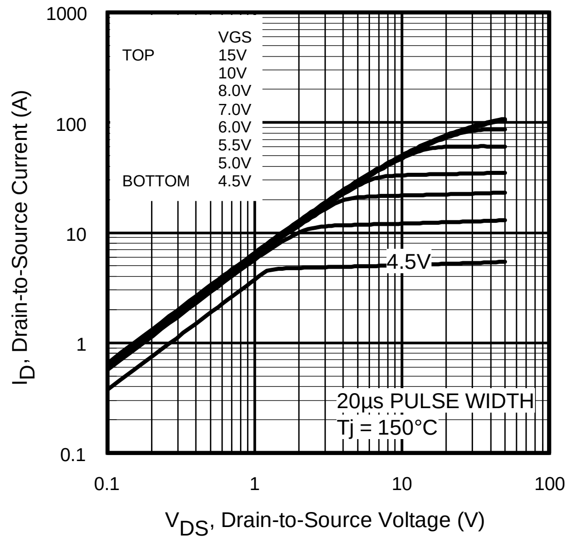


Fig 2. Typical Output Characteristics

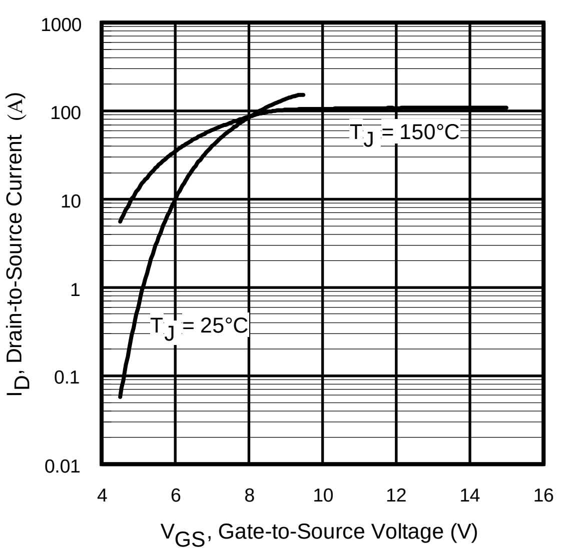


Fig 3. Typical Transfer Characteristics

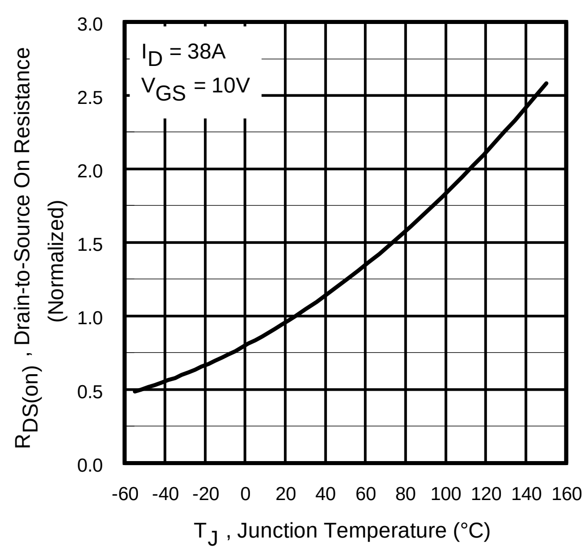


Fig 4. Normalized On-Resistance vs. Temperature

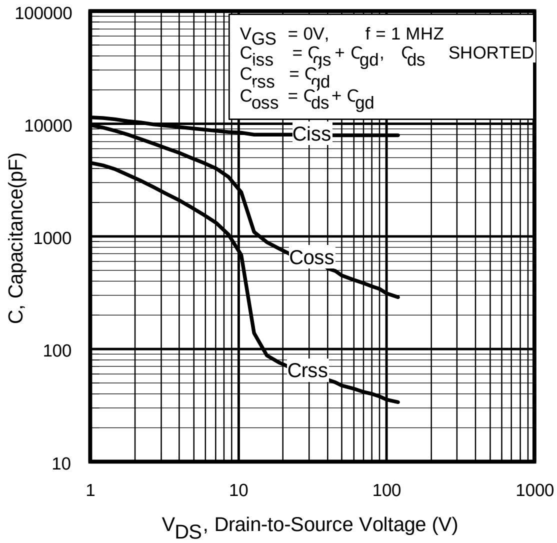


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

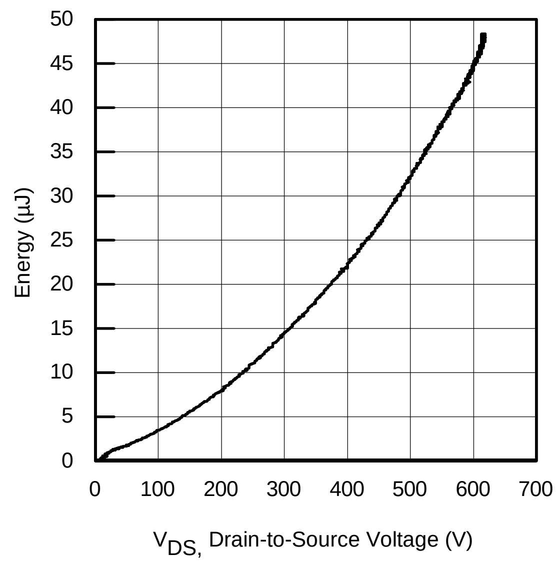


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

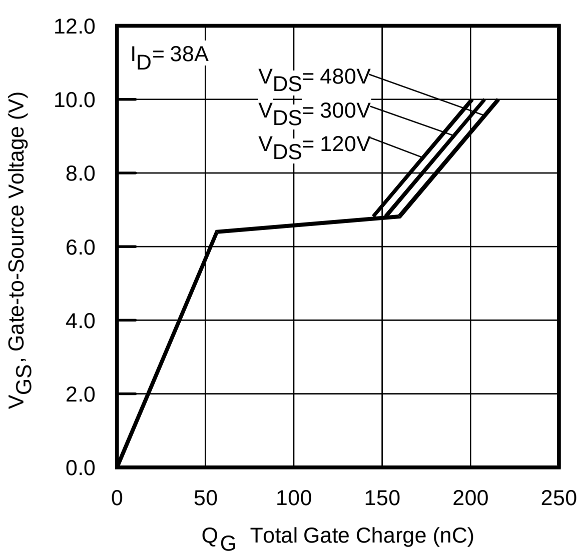


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

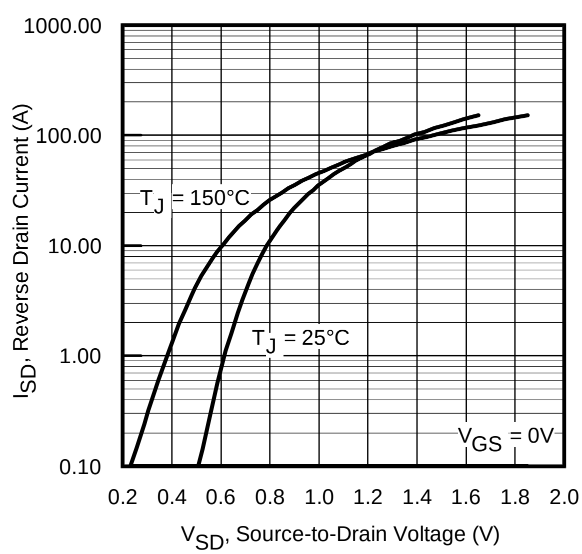


Fig 8. Typical Source-Drain Diode Forward Voltage

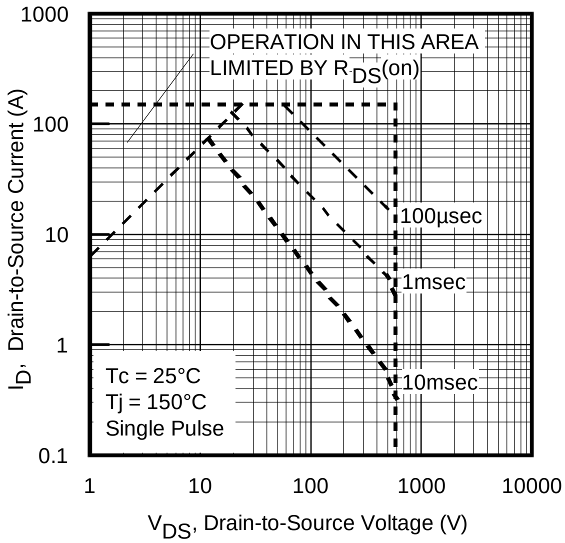


Fig 9. Maximum Safe Operating Area

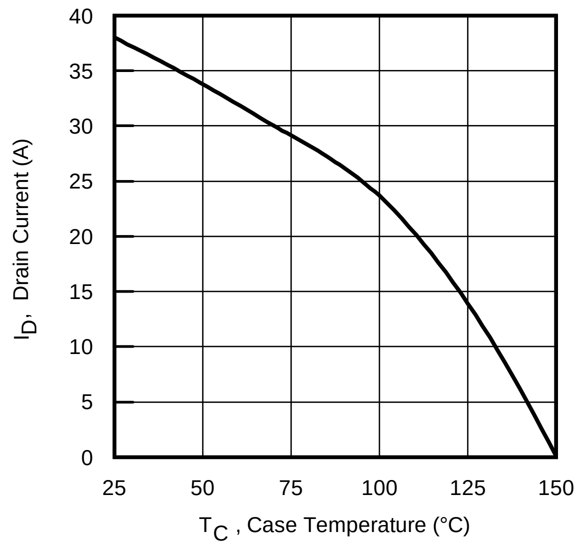


Fig 10. Maximum Drain Current vs. Case Temperature

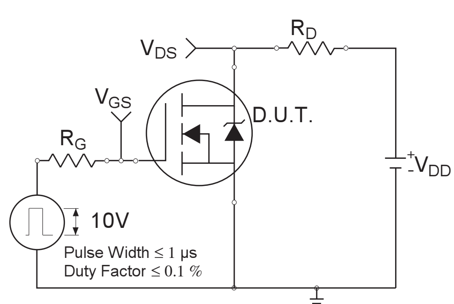


Fig 11a. Switching Time Test Circuit

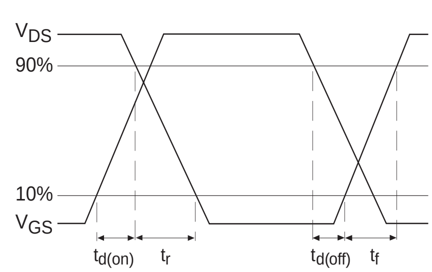


Fig 11b. Switching Time Waveforms

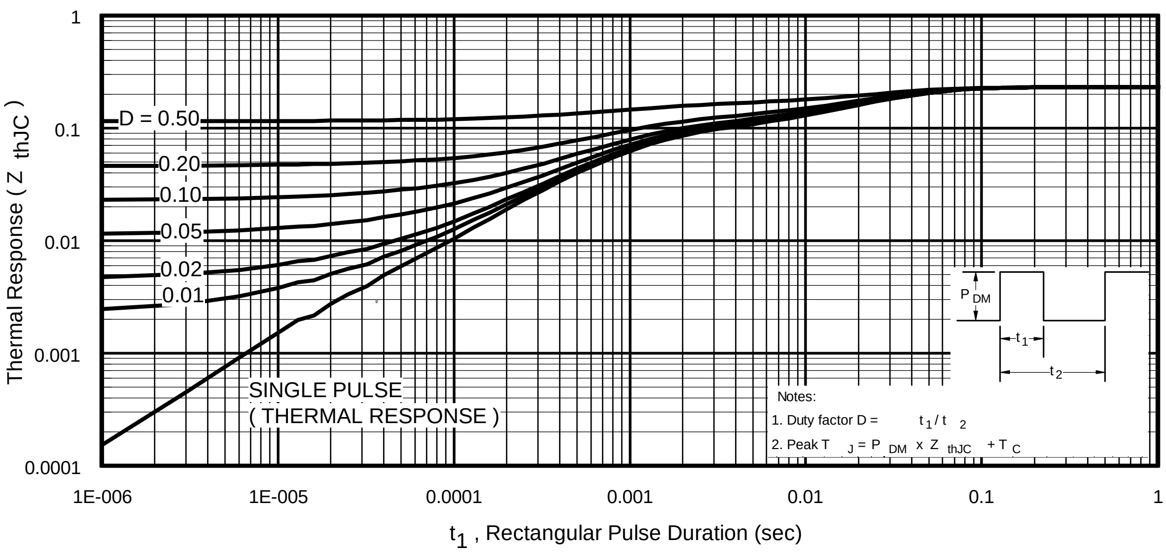


Fig 12. Maximum Effective Transient Thermal Impedance, Junction-to-Case

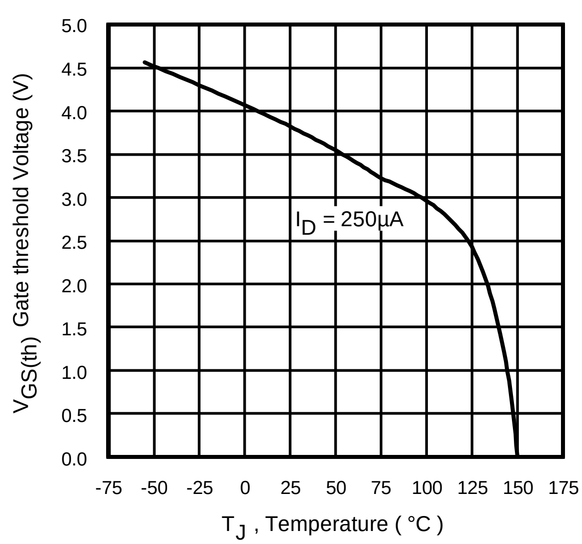


Fig 13. Threshold Voltage vs. Temperature

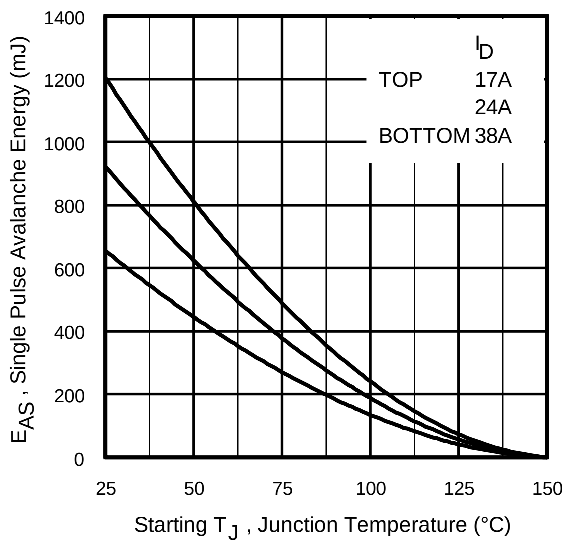


Fig 14a. Maximum Avalanche Energy vs. Drain Current

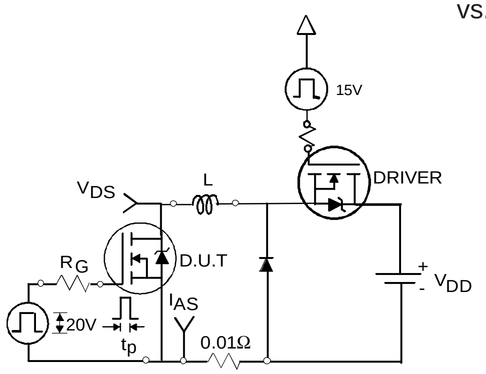


Fig 14b. Unclamped Inductive Test Circuit

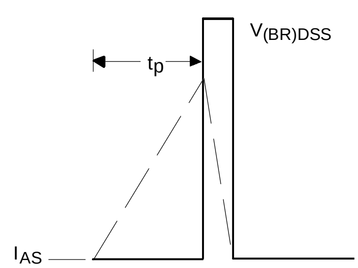


Fig 14c. Unclamped Inductive Waveforms

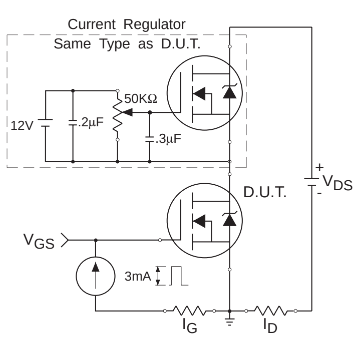


Fig 15a. Gate Charge Test Circuit

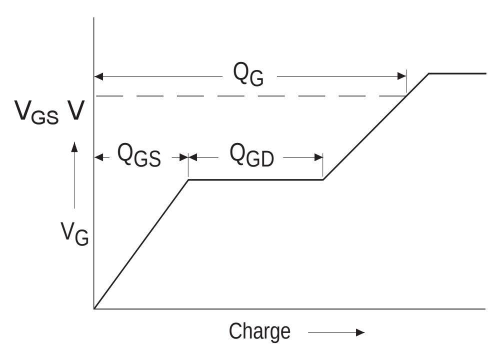
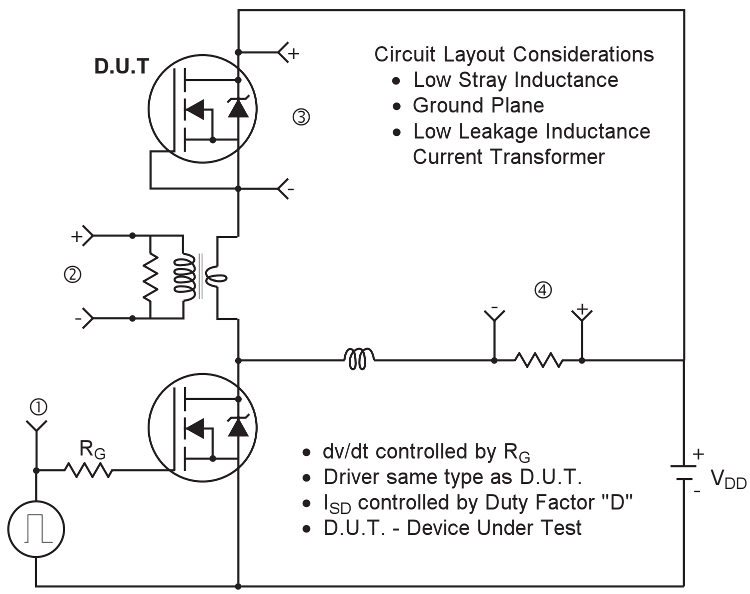
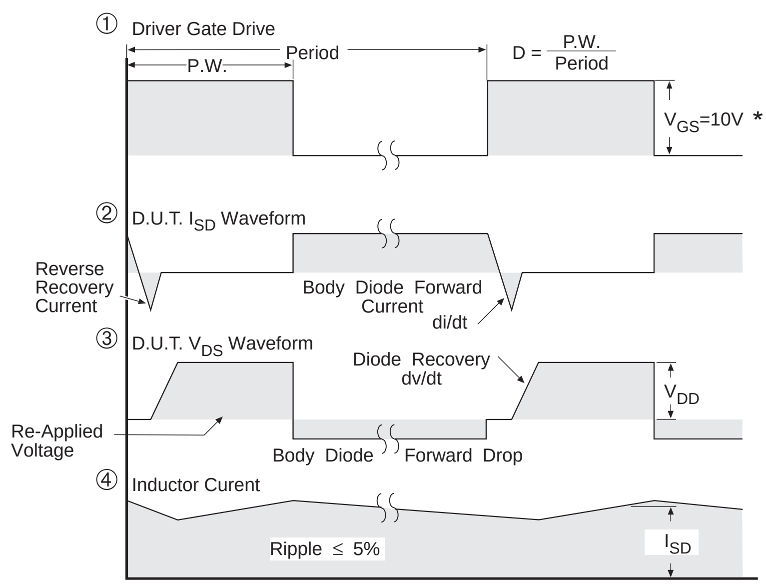


Fig 15b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



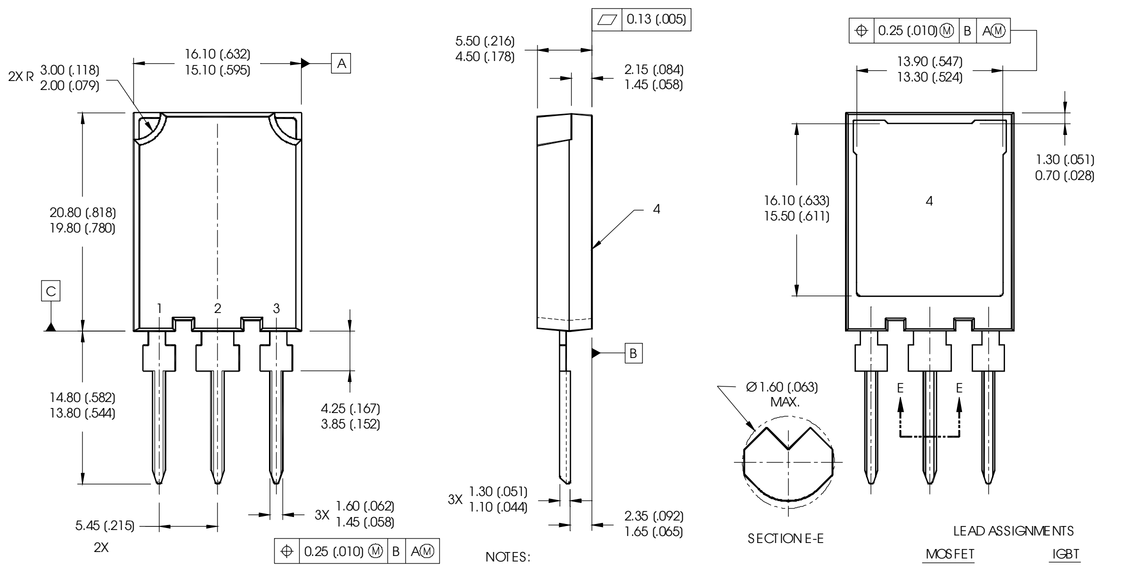


* V_{GS} = 5V for Logic Level Devices

Fig 16. For N-Channel HEXFET® Power MOSFETs

SUPER TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES)
3. CONTROLLING DIMENSION: MILLIMETER
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-274AA

LEAD ASSIGNMENTS

MOSFET	IGBT
1 - GATE	1 - GATE
2 - DRAIN	2 - COLLECTOR
3 - SOURCE	3 - EMITTER
4 - DRAIN	4 - COLLECTOR

Super TO-247AC package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

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