

# International IR Rectifier

PD- 93923B

## SMPS MOSFET IRFPS40N50L

HEXFET® Power MOSFET

### Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- ZVS and High Frequency Circuit
- PWM Inverters

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> typ.</b>	<b>I<sub>D</sub></b>
<b>500V</b>	<b>0.087Ω</b>	<b>46A</b>

### Benefits

- Low Gate Charge Q<sub>g</sub> results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low T<sub>rr</sub> and Soft Diode Recovery
- High Performance Optimised Anti-parallel Diode



### Absolute Maximum Ratings

	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	46	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	29	
I <sub>DM</sub>	Pulsed Drain Current ①	180	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	540	W
	Linear Derating Factor	4.3	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
	dv/dt Peak Diode Recovery dv/dt ③	25	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

### Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	46	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	180		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.5	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 46A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	170	250	ns	T <sub>J</sub> = 25°C I <sub>F</sub> = 46A
		—	220	330		T <sub>J</sub> = 125°C di/dt = 100A/μs ④
Q <sub>rr</sub>	Reverse Recovery Charge	—	705	1060	nC	T <sub>J</sub> = 25°C
		—	1.3	2.0		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	9.0	—	A	
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

### Typical SMPS Topologies

- Bridge Converters
- All Zero Voltage Switching

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$ Ⓞ
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.087	0.100	$\Omega$	$V_{GS} = 10V, I_D = 28A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	50	$\mu A$	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	2.0	mA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -30V$

## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	21	—	—	S	$V_{DS} = 50V, I_D = 46A$
$Q_g$	Total Gate Charge	—	—	380	nC	$I_D = 46A$
$Q_{gs}$	Gate-to-Source Charge	—	—	80		$V_{DS} = 400V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	190		$V_{GS} = 10V$ , See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	$V_{DD} = 250V$
$t_r$	Rise Time	—	170	—		$I_D = 46A$
$t_{d(off)}$	Turn-Off Delay Time	—	50	—		$R_G = 0.85\Omega$
$t_f$	Fall Time	—	69	—		$V_{GS} = 10V$ , See Fig. 10 ④
$C_{iss}$	Input Capacitance	—	8110	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	960	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	130	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	11200	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	240	—		$V_{GS} = 0V, V_{DS} = 400V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	420	—		$V_{GS} = 0V, V_{DS} = 0V$ to $400V$ ⑤

## Avalanche Characteristics

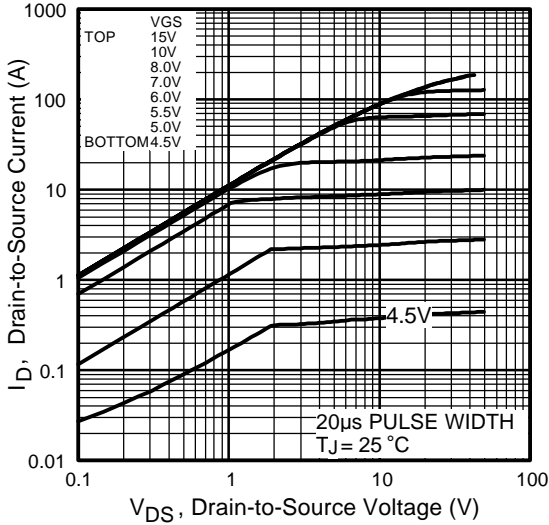
Symbol	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	920	mJ
$I_{AR}$	Avalanche Current①	—	46	A
$E_{AR}$	Repetitive Avalanche Energy①	—	54	mJ

## Thermal Resistance

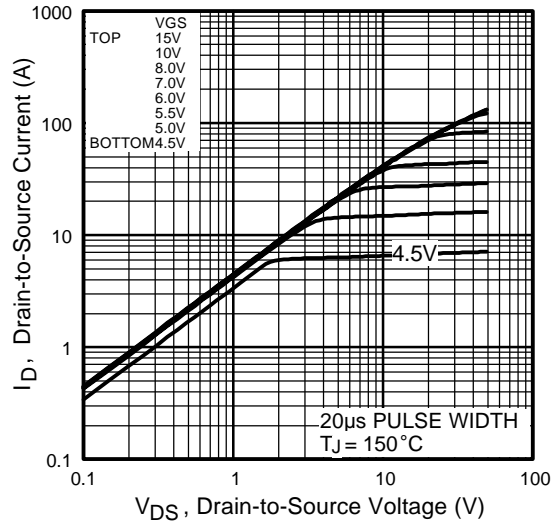
Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.23	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

### Notes:

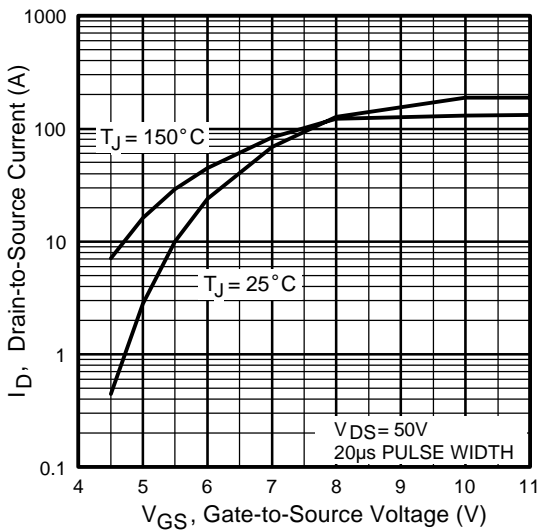
- ① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11)
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.86\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 46A$  (See Figure 12a)
- ③  $I_{SD} \leq 46A$ ,  $di/dt \leq 367A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$



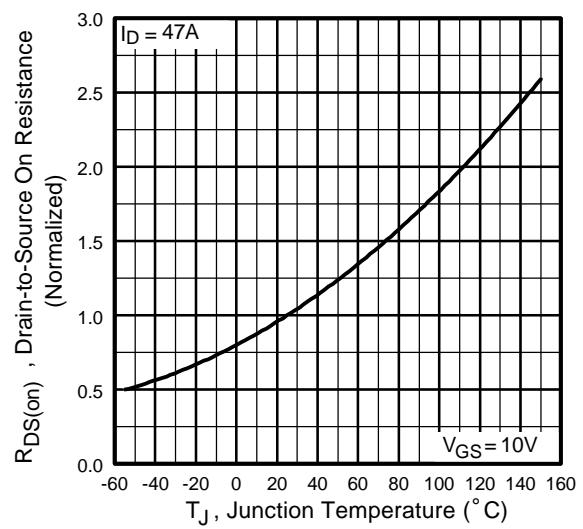
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



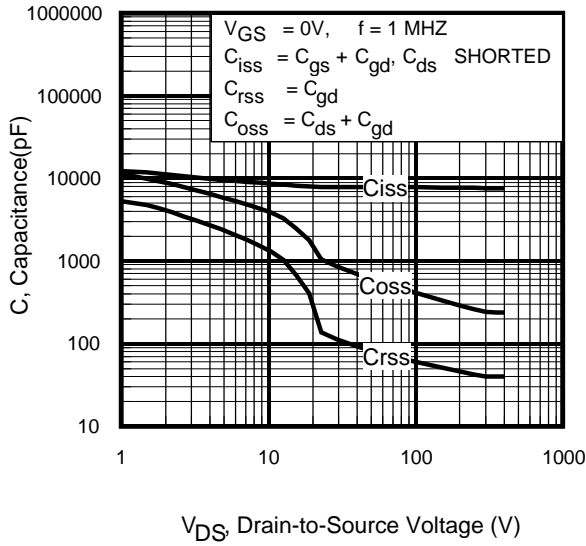
**Fig 3.** Typical Transfer Characteristics



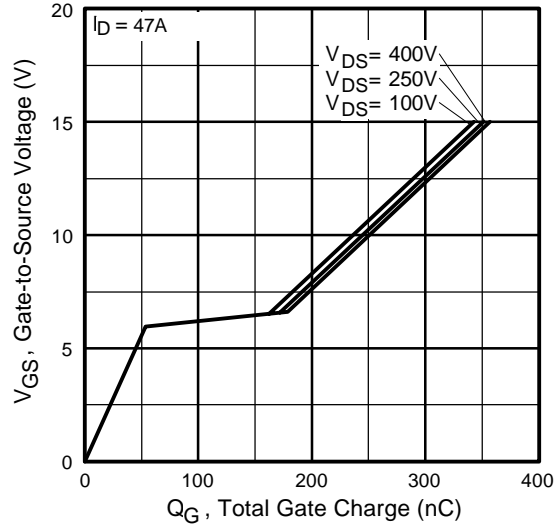
**Fig 4.** Normalized On-Resistance Vs. Temperature

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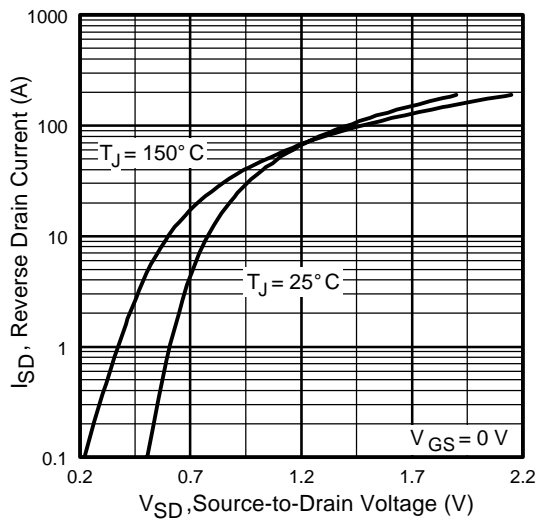
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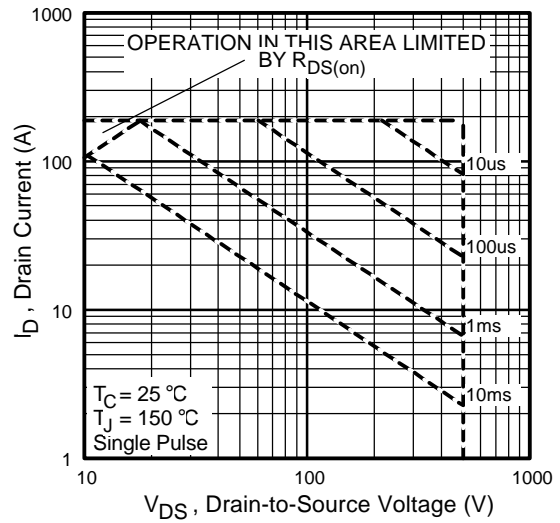
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



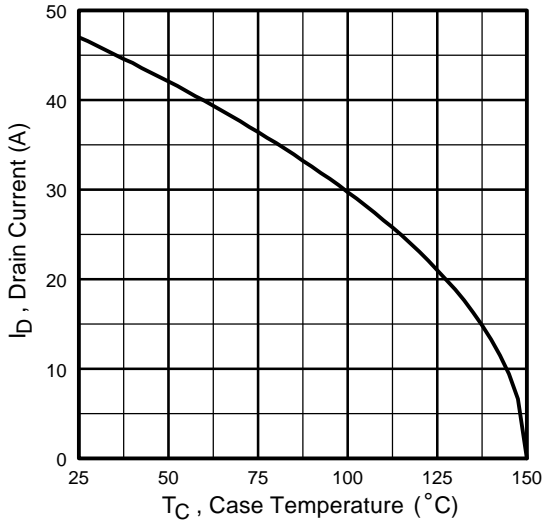
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



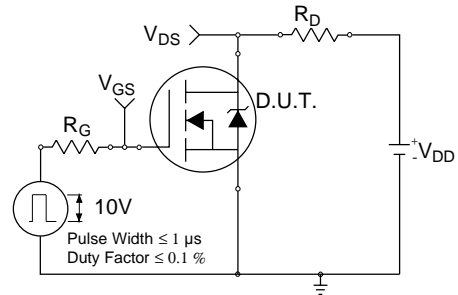
**Fig 7.** Typical Source-Drain Diode Forward Voltage



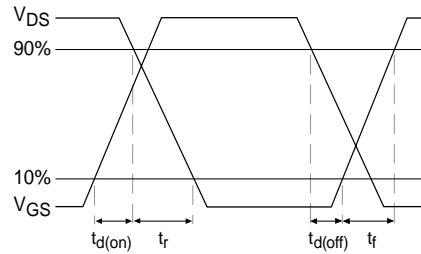
**Fig 8.** Maximum Safe Operating Area



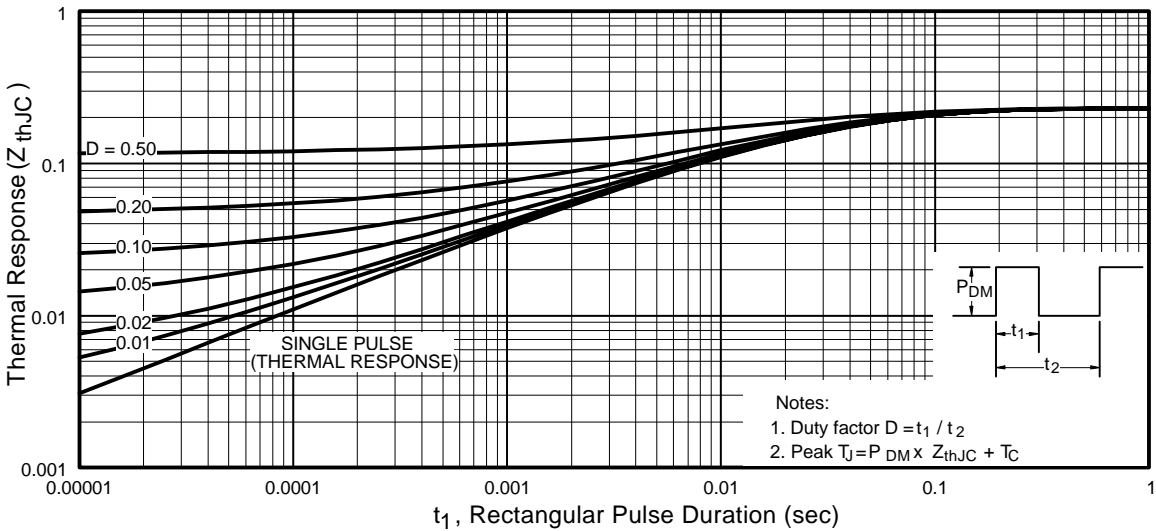
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



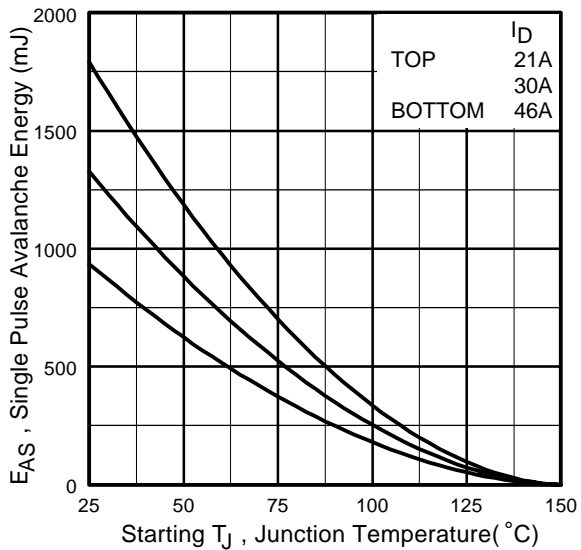
**Fig 10b.** Switching Time Waveforms



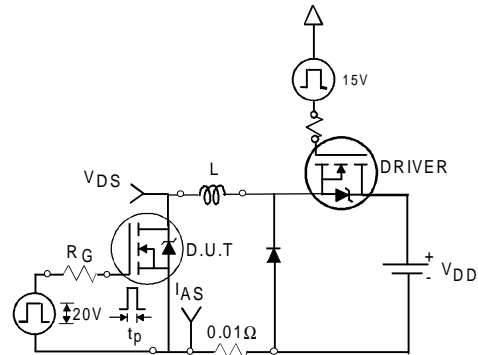
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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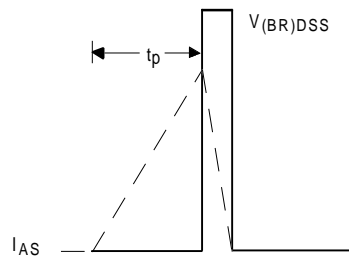
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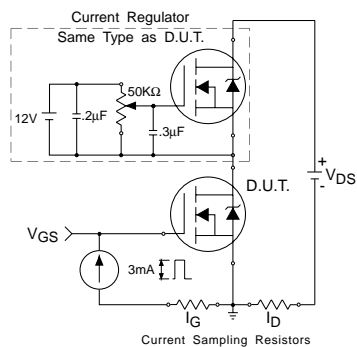
**Fig 12a.** Maximum Avalanche Energy Vs. Drain Current



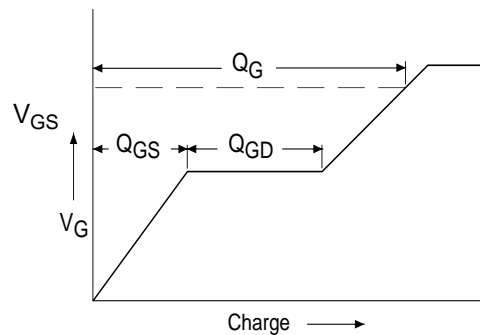
**Fig 12c.** Unclamped Inductive Test Circuit



**Fig 12d.** Unclamped Inductive Waveforms

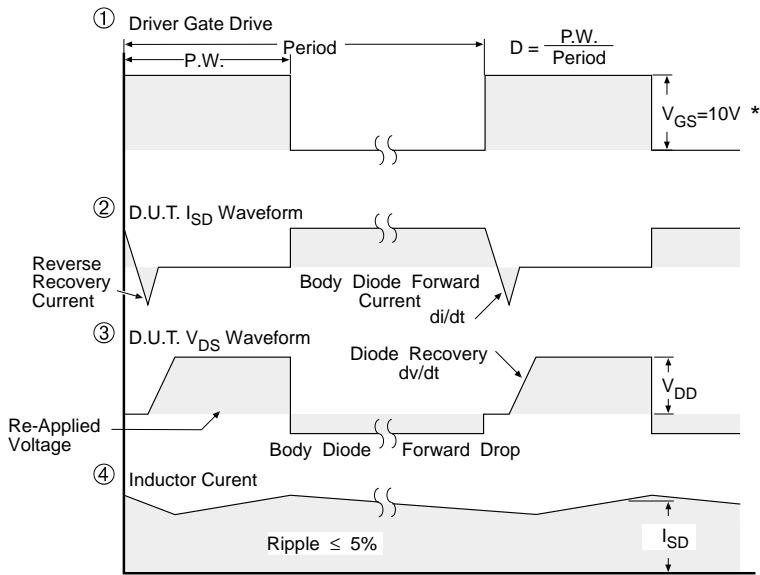
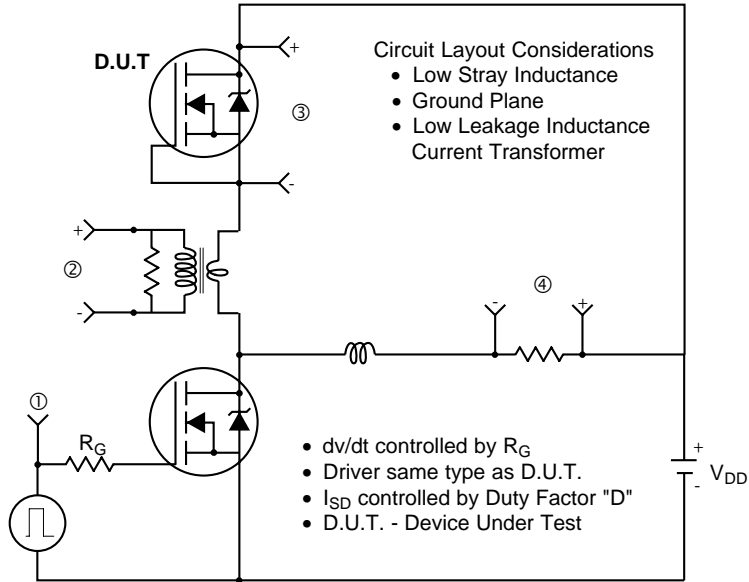


**Fig 13a.** Gate Charge Test Circuit



**Fig 13b.** Basic Gate Charge Waveform

**Peak Diode Recovery dv/dt Test Circuit**



\*  $V_{GS} = 5V$  for Logic Level Devices

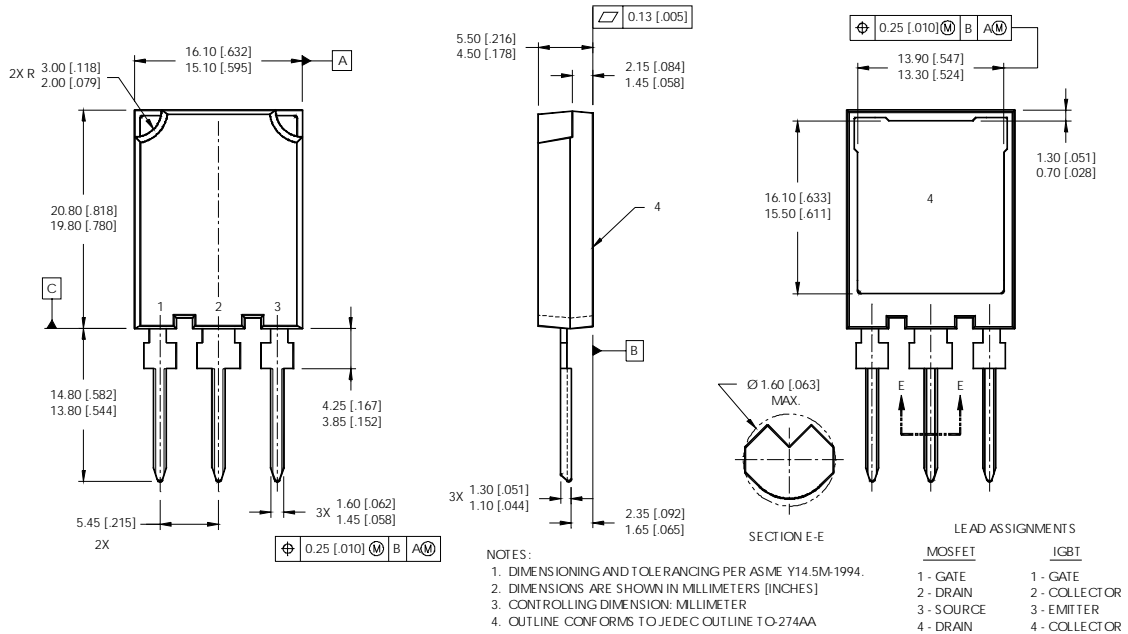
**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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## SUPER TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



Data and specifications subject to change without notice.  
This product has been designed and qualified for the industrial market.  
Qualification Standards can be found on IR's Web site.

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