



March 2001

QFET™

## FQB13N50 / FQI13N50

### 500V N-Channel MOSFET

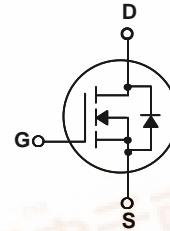
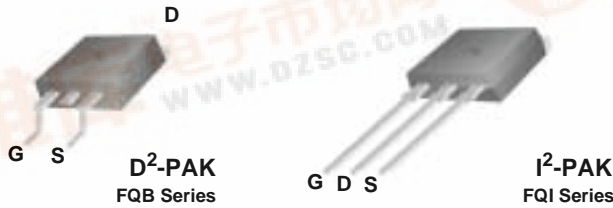
#### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, and electronic lamp ballast based on half bridge.

#### Features

- 12.5A, 500V.  $R_{DS(on)} = 0.43\Omega$  @  $V_{GS} = 10V$
- Low gate charge ( typical 45 nC).
- Low  $C_{rss}$  ( typical 25 pF).
- Fast switching.
- 100% avalanche tested.
- Improved dv/dt capability.



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB13N50 / FQI13N50	Units
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	12.5	A
		7.9	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	50	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	810	mJ
$I_{AR}$	Avalanche Current (Note 1)	12.5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	17	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	170	W
	- Derate above $25^\circ\text{C}$	1.35	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.74	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)



## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.48	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 6.25\text{ A}$	--	0.33	0.43	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 6.25\text{ A}$ (Note 4)	--	10	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1800	2300	pF
$C_{oss}$	Output Capacitance		--	245	320	pF
$C_{rss}$	Reverse Transfer Capacitance		--	25	35	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 13.4\text{ A},$ $R_G = 25\ \Omega$  (Note 4, 5)	--	40	90	ns
$t_r$	Turn-On Rise Time		--	140	290	ns
$t_{d(off)}$	Turn-Off Delay Time		--	100	210	ns
$t_f$	Turn-Off Fall Time		--	85	180	ns
$Q_g$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 13.4\text{ A},$ $V_{GS} = 10\text{ V}$  (Note 4, 5)	--	45	60	nC
$Q_{gs}$	Gate-Source Charge		--	11	--	nC
$Q_{gd}$	Gate-Drain Charge		--	22	--	nC
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	12.5	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	50	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 12.5\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 13.4\text{ A},$ $dI_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	290	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	2.6	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 9.3\text{mH}, I_{AS} = 12.5\text{A}, V_{DD} = 50\text{V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 13.4\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

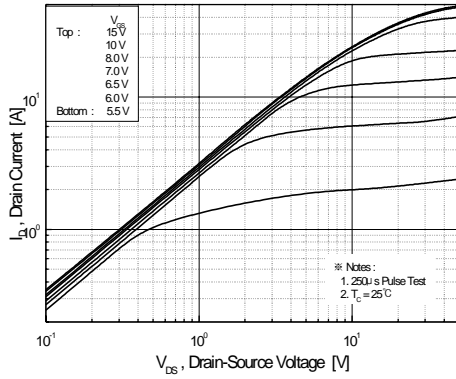


Figure 1. On-Region Characteristics

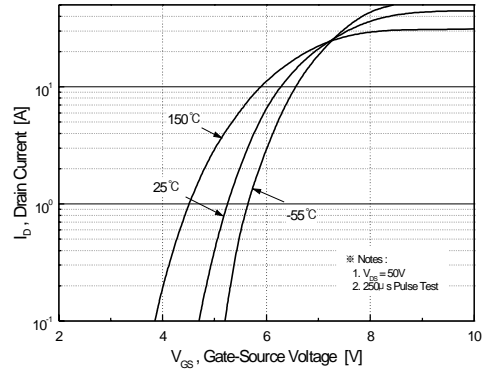


Figure 2. Transfer Characteristics

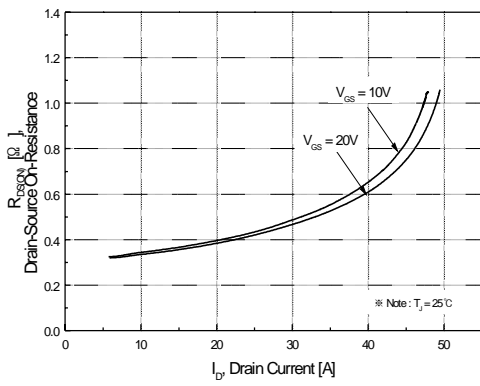


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

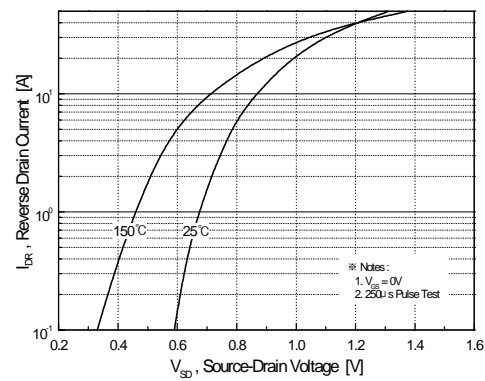


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

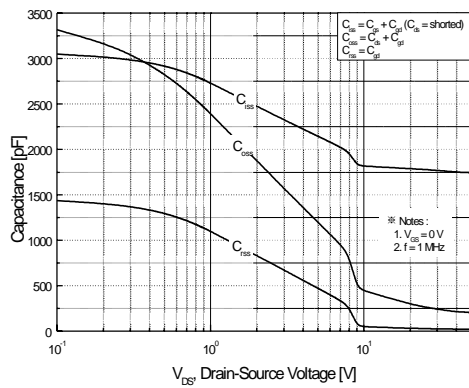


Figure 5. Capacitance Characteristics

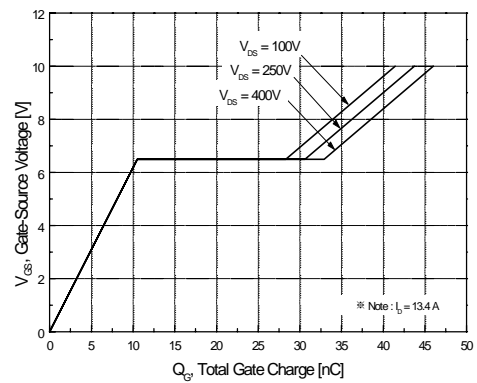
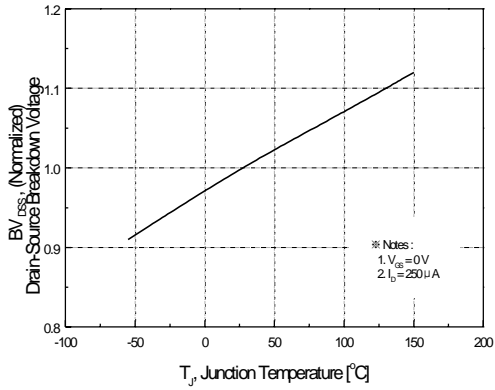
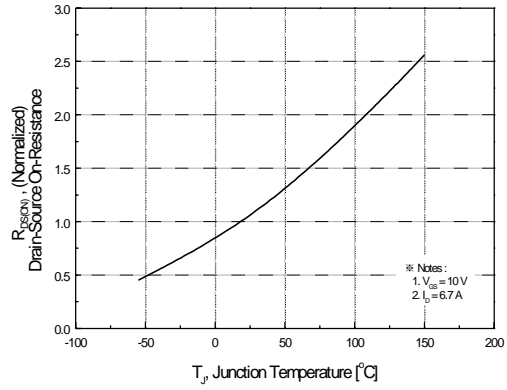


Figure 6. Gate Charge Characteristics

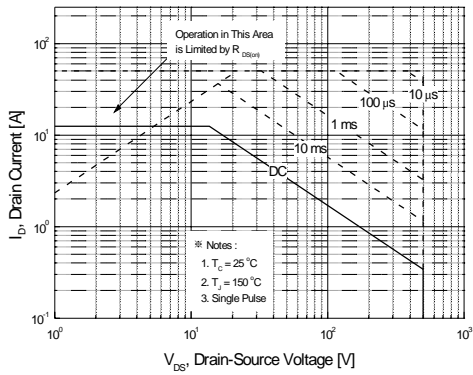
**Typical Characteristics** (Continued)



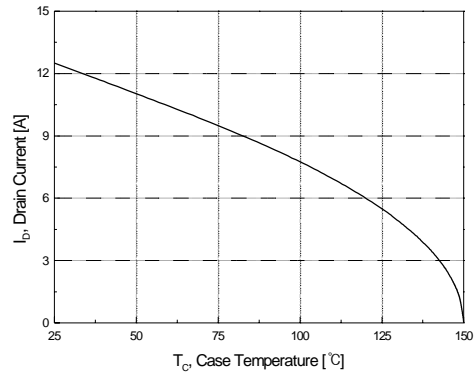
**Figure 7. Breakdown Voltage Variation vs. Temperature**



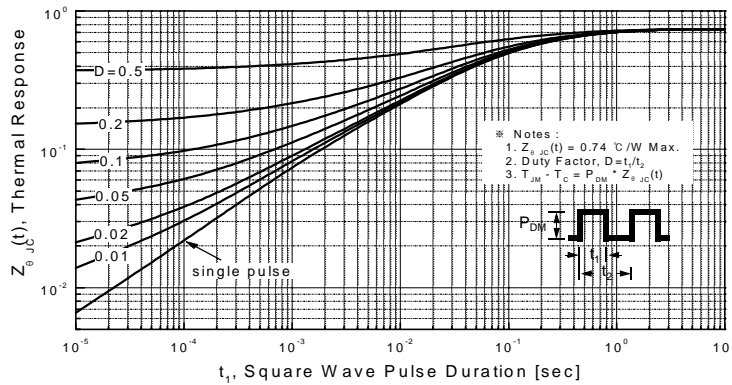
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

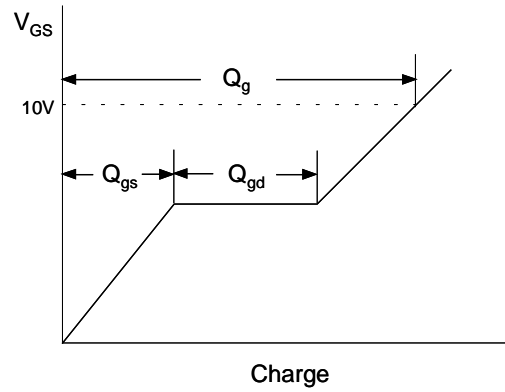
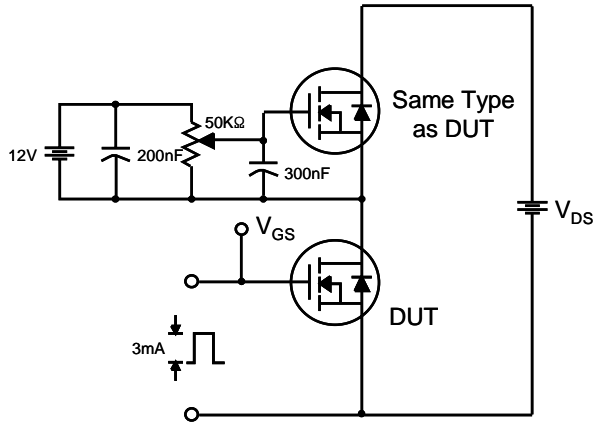


**Figure 10. Maximum Drain Current vs. Case Temperature**

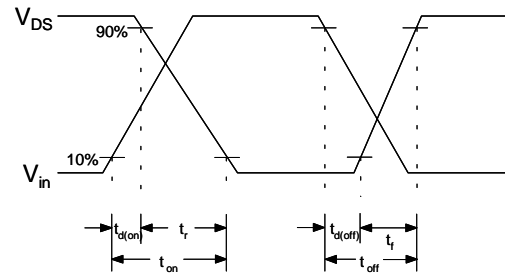
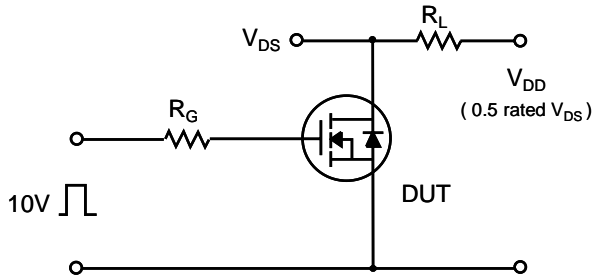


**Figure 11. Transient Thermal Response Curve**

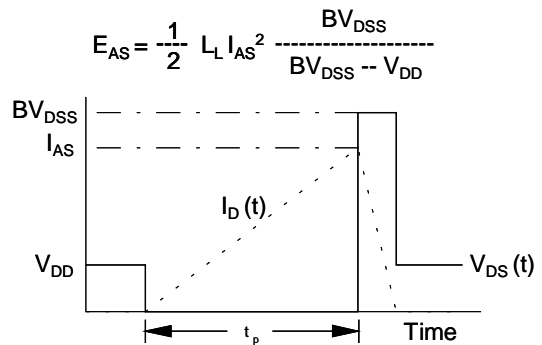
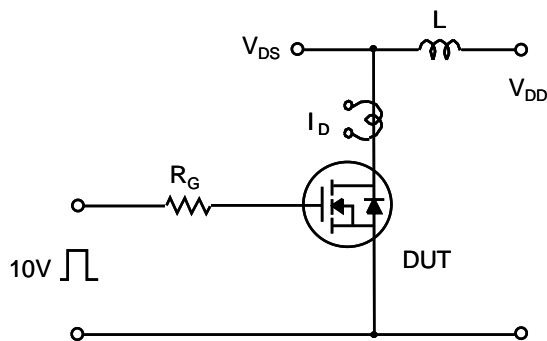
**Gate Charge Test Circuit & Waveform**



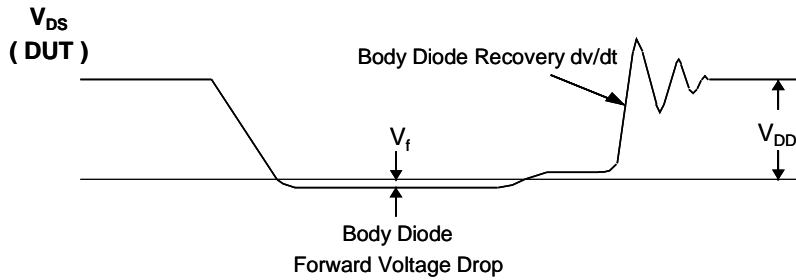
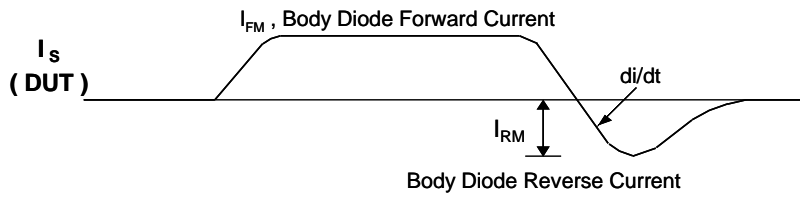
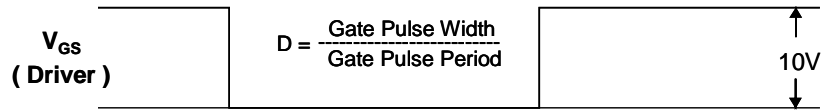
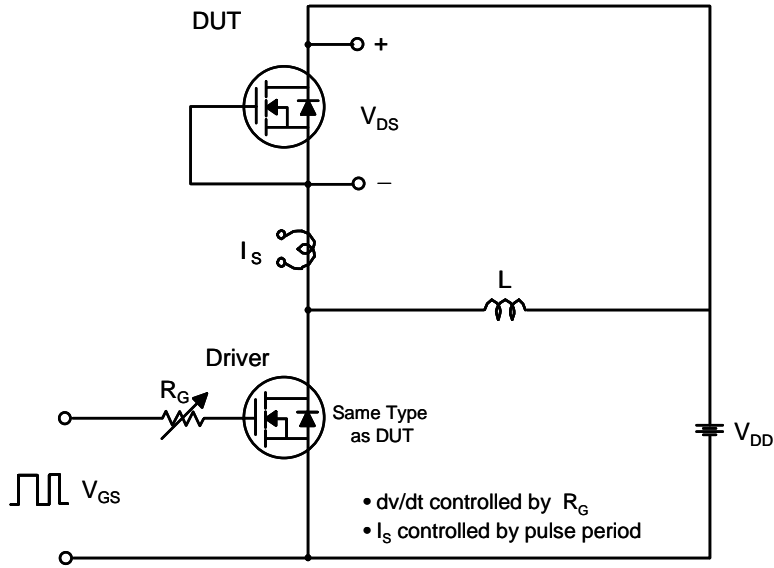
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

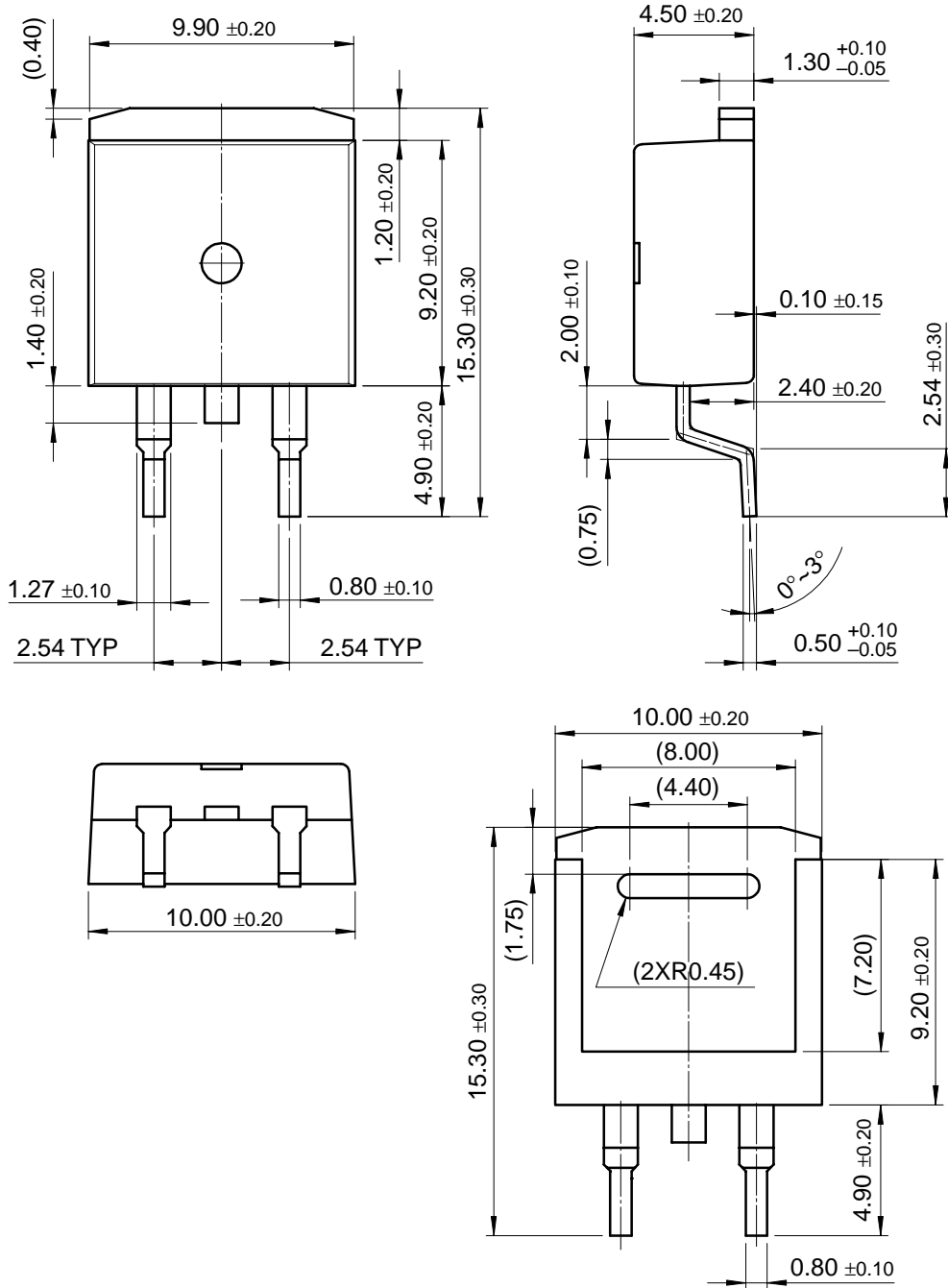


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

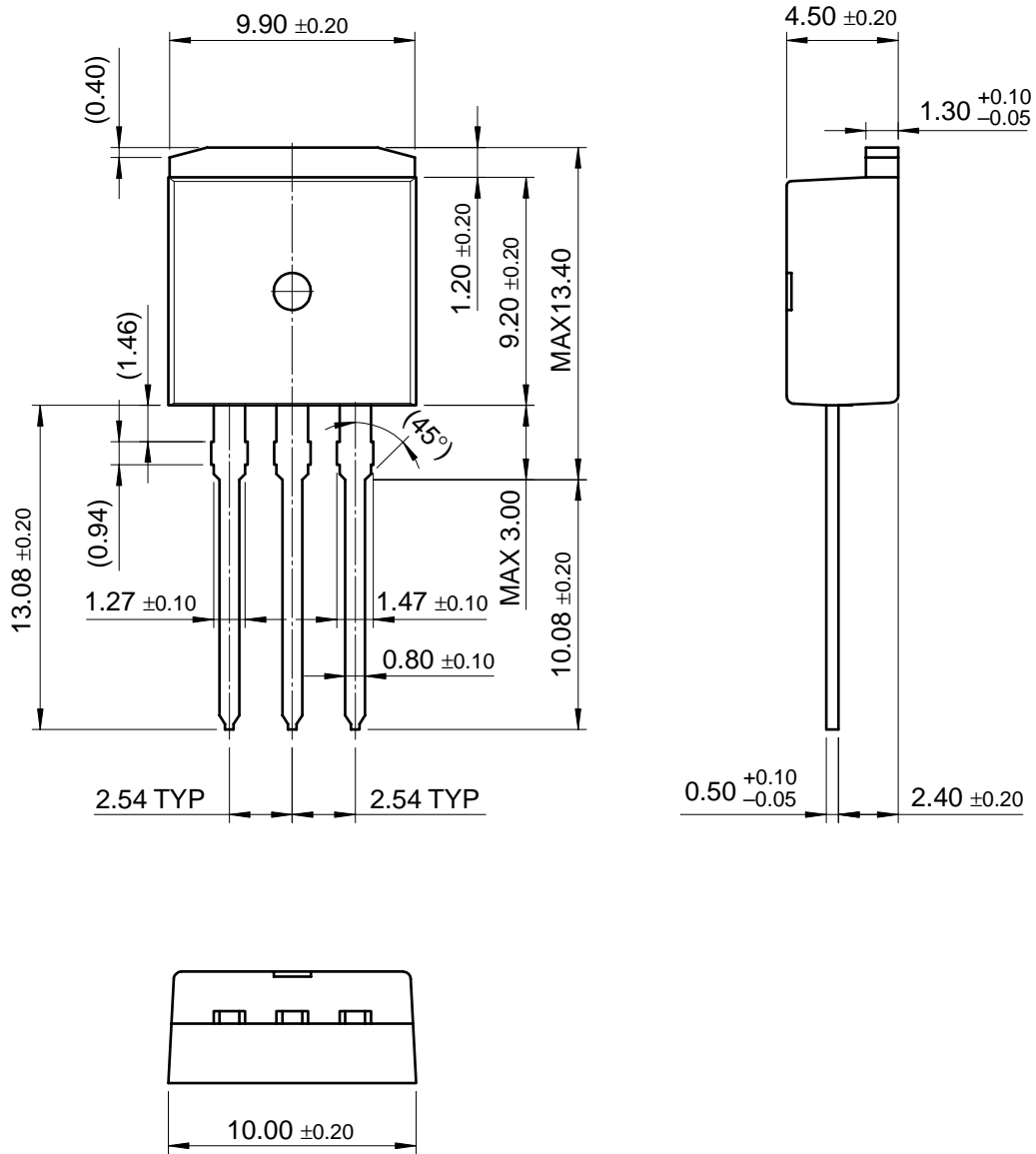
D<sup>2</sup>PAK



FQB13N50 / FQI13N50

Package Dimensions (Continued)

# I<sup>2</sup>PAK





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