

FQB9N08L / FQI9N08L



June 2000

QFET™

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### 80V LOGIC N-Channel MOSFET

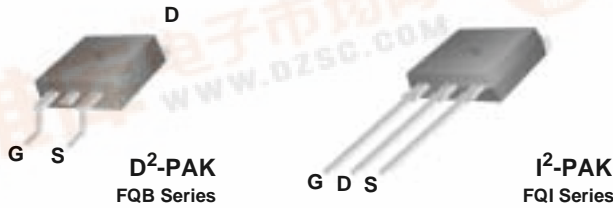
#### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, high efficiency switching for DC/DC converters, and DC motor control.

#### Features

- 9.3A, 80V,  $R_{DS(on)} = 0.21\Omega$  @  $V_{GS} = 10V$
- Low gate charge ( typical 4.7 nC)
- Low  $C_{rss}$  ( typical 16 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating
- Low level gate drive requirements allowing direct operation from logic drives



#### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB9N08L / FQI9N08L	Units
$V_{DSS}$	Drain-Source Voltage	80	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	9.3	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	6.57	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	37.2	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	55	mJ
$I_{AR}$	Avalanche Current (Note 1)	9.3	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	4.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.75	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	40	W
	- Derate above $25^\circ\text{C}$	0.27	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	3.75	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	40	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)



## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	80	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.08	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 64\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

## On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 4.65\text{ A}$	--	0.15	0.21	$\Omega$
		$V_{GS} = 5\text{ V}, I_D = 4.65\text{ A}$	--	0.17	0.23	
$g_{FS}$	Forward Transconductance	$V_{DS} = 25\text{ V}, I_D = 4.65\text{ A}$ (Note 4)	--	4.9	--	S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	215	280	pF
$C_{oss}$	Output Capacitance		--	70	90	pF
$C_{riss}$	Reverse Transfer Capacitance		--	16	20	pF

## Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}, I_D = 9.3\text{ A},$ $R_G = 25\ \Omega$	--	6.5	23	ns	
$t_r$	Turn-On Rise Time		--	180	370	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4, 5)	--	13	35	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	30	70	ns
$Q_g$	Total Gate Charge	$V_{DS} = 64\text{ V}, I_D = 9.3\text{ A},$ $V_{GS} = 5\text{ V}$	--	4.7	6.1	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4, 5)	--	1.2	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	2.8	--	nC

## Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	9.3	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	37.2	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 9.3\text{ A}$	--	--	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 9.3\text{ A},$	--	54	--	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	80	--	nC

### Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 0.87\text{ mH}, I_{AS} = 9.3\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 9.3\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

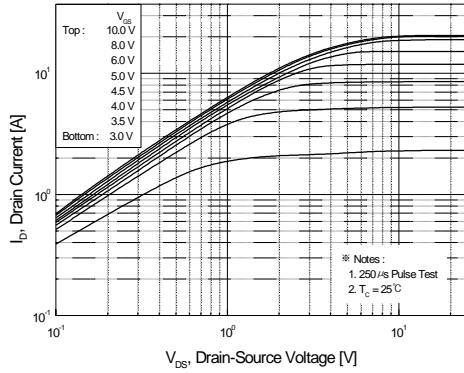


Figure 1. On-Region Characteristics

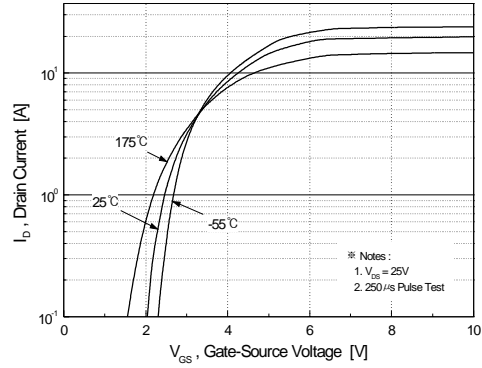


Figure 2. Transfer Characteristics

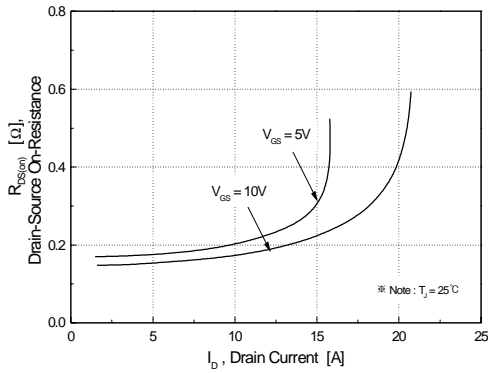


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

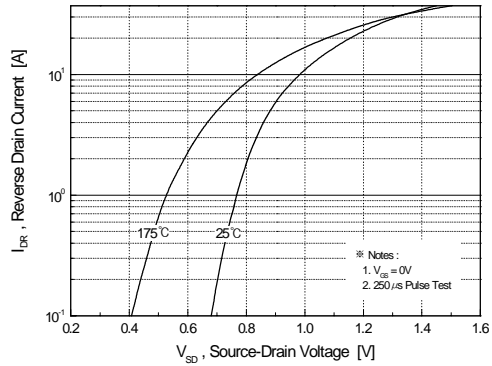


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

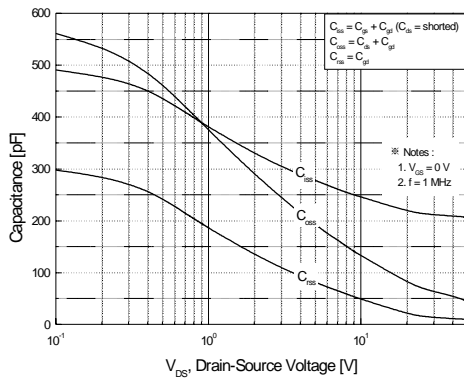


Figure 5. Capacitance Characteristics

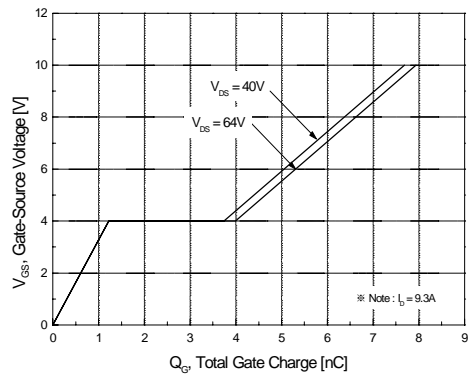
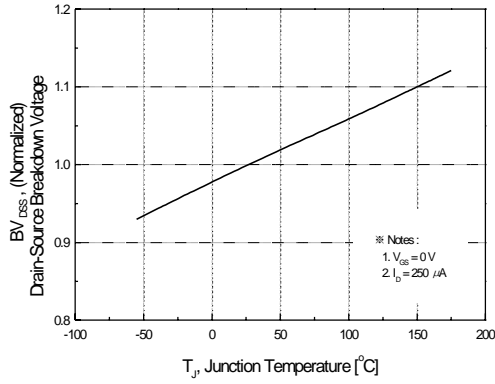
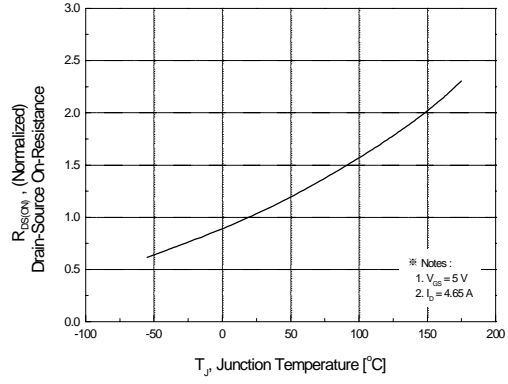


Figure 6. Gate Charge Characteristics

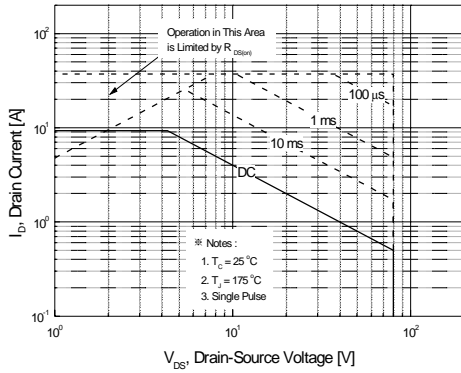
**Typical Characteristics** (Continued)



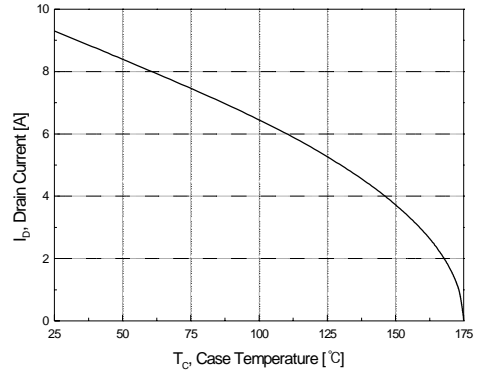
**Figure 7. Breakdown Voltage Variation vs. Temperature**



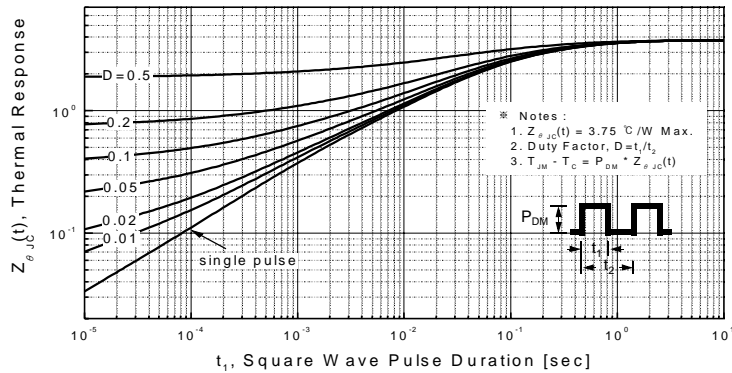
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

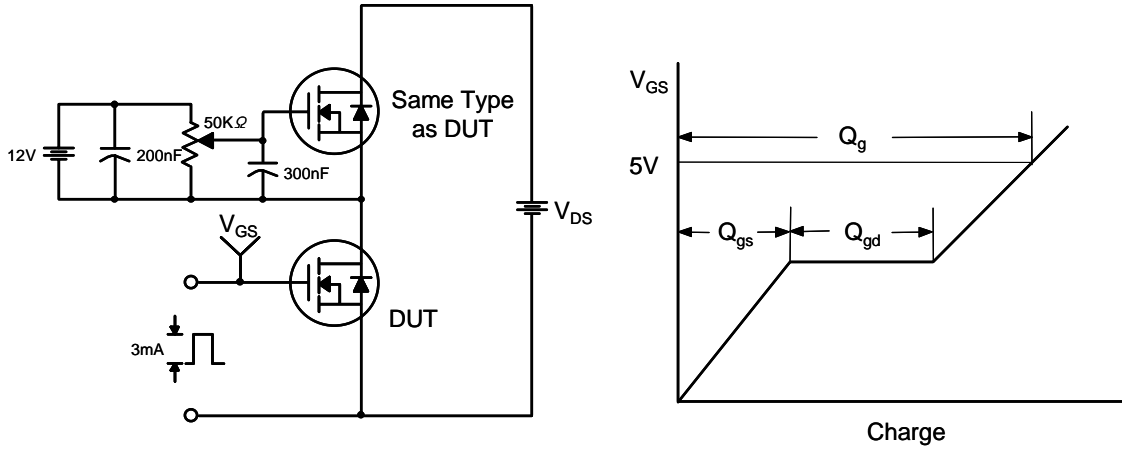


**Figure 10. Maximum Drain Current vs. Case Temperature**

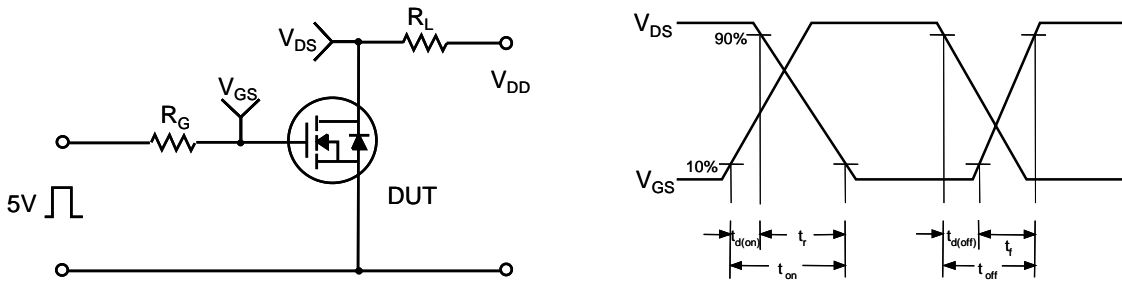


**Figure 11. Transient Thermal Response Curve**

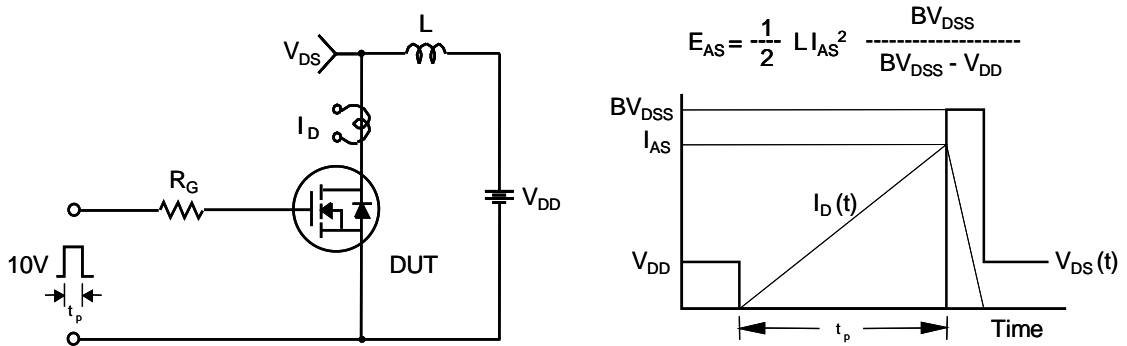
Gate Charge Test Circuit & Waveform



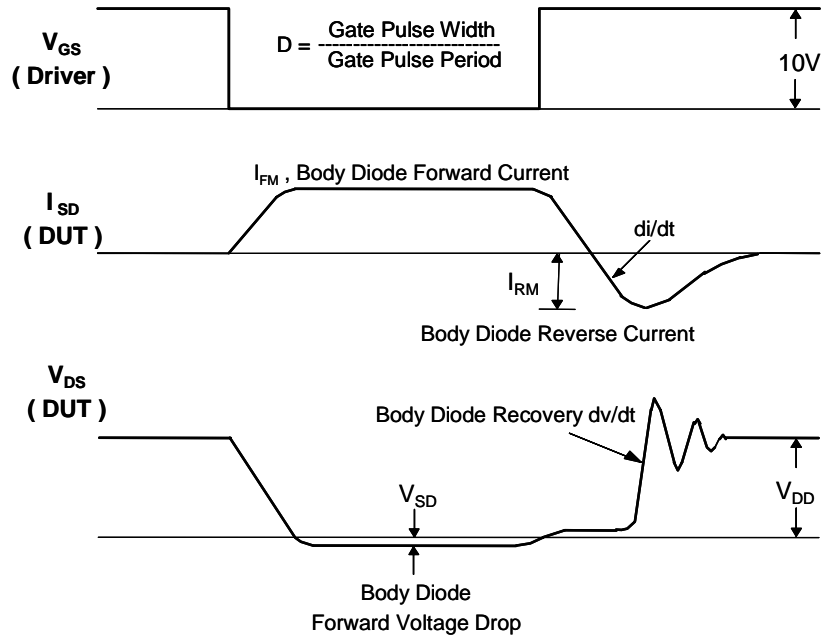
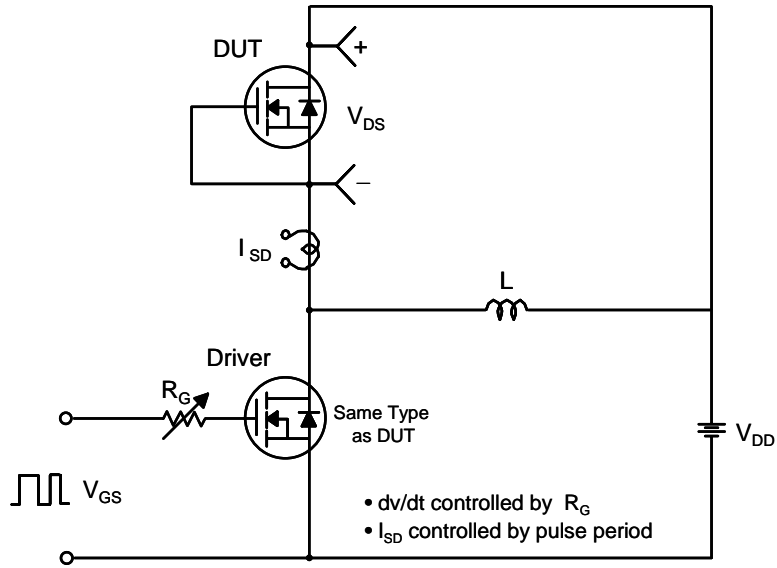
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

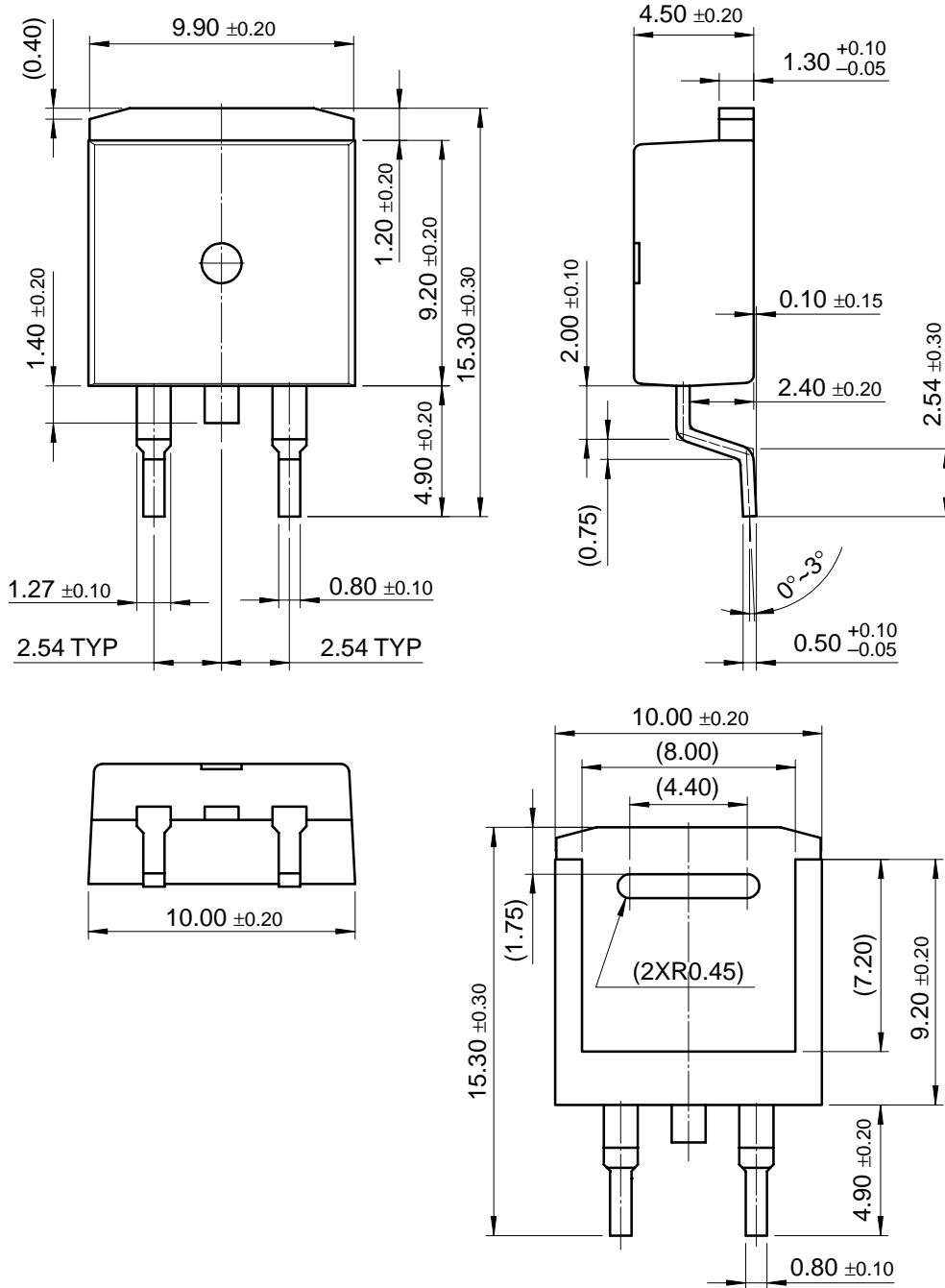


Peak Diode Recovery dv/dt Test Circuit & Waveforms



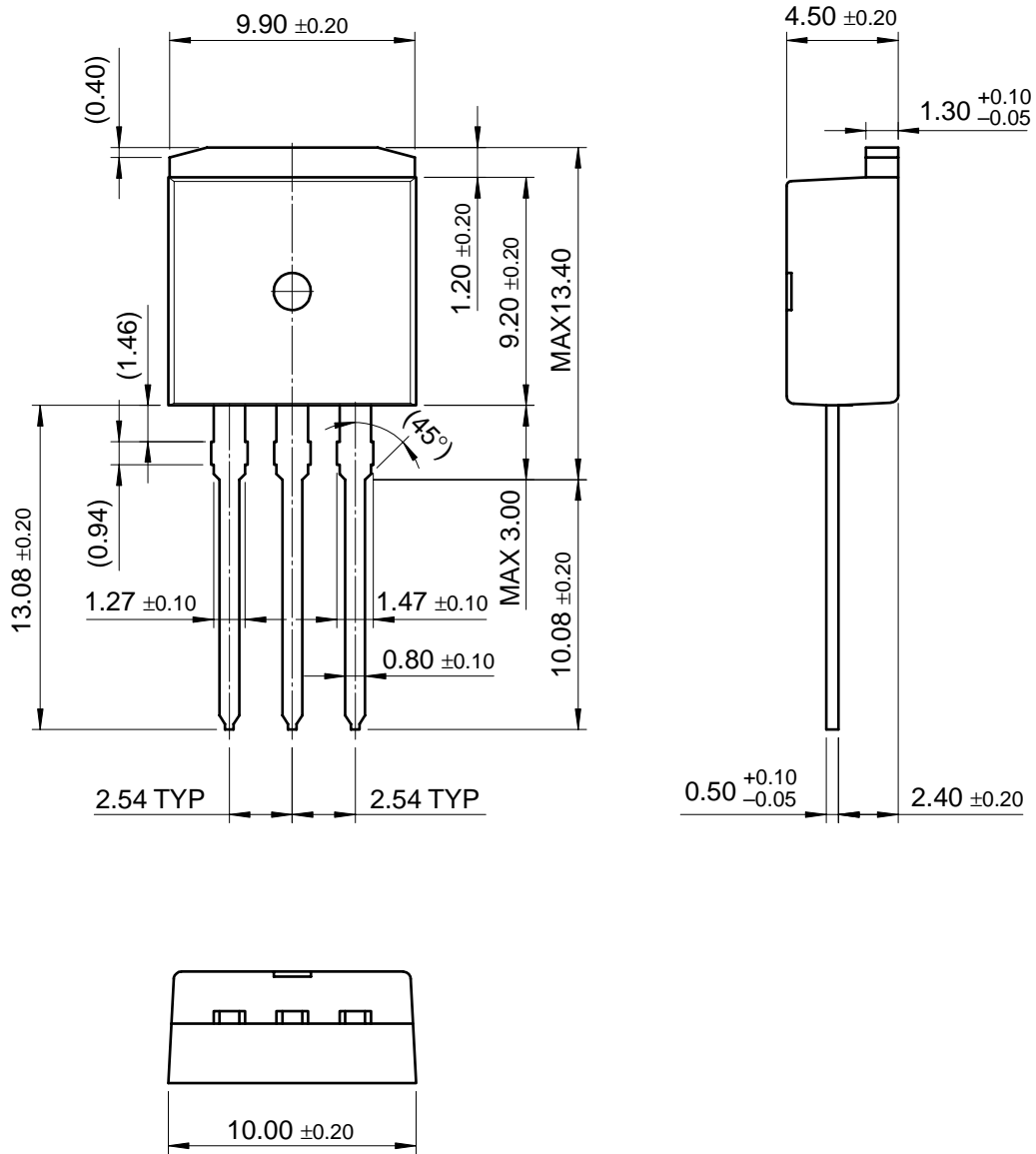
Package Dimensions

D<sup>2</sup>PAK



Package Dimensions (Continued)

# I<sup>2</sup>PAK



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