

May 2001



# FQP60N03L

## 30V LOGIC N-Channel MOSFET

## **General Description**

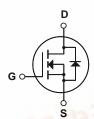
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters, high efficiency switching for power management in portable and battery operated products.

## **Features**

- 60A, 30V.  $R_{DS(on)} = 0.0135\Omega @V_{GS} = 10 V$
- Low gate charge (typical 18.5 nC)
- Low Crss (typical 155 pF)
- Fast switching
- 100% avalanche tested
- · Improved dv/dt capability
- 175°C maximum junction temperature rating





# Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	07\//g =	FQP60N03L	Units	
$V_{DSS}$	Drain-Source Voltage		30	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)		60	А	
			42.5	А	
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	240	А	
V <sub>GSS</sub>	Gate-Source Voltage		± 20	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	220	mJ	
I <sub>AR</sub>	Avalanche Current	(Note 1)	60	Α	
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	10.0	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)		7.0	V/ns	
$P_{D}$	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C		100	W	
			0.67	W/°C	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +175	°C	
TL	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C	

# **Thermal Characteristics**

Symbol	Parameter	Тур	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		1.50	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.5		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		62.5	°C/W

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$				V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 μA, Referenced to 25°C		0.02		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V			1	μΑ
		V <sub>DS</sub> = 24 V, T <sub>C</sub> = 150°C			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V			-100	nA
On Cha	racteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	1.0		2.5	V
R <sub>DS(on)</sub>	Static Drain-Source	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		0.011	0.0135	
D3(0H)	On-Resistance	V <sub>GS</sub> =5 V, I <sub>D</sub> =30 A		0.015	0.019	Ω
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 15 \text{ V}, I_{D} = 30 \text{ A}$ (Note	4)	33		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz		875 570 155	740 200	pF pF
	ing Characteristics			133	200	рі
t <sub>d(on)</sub>	Turn-On Delay Time	V 45.V L 00.A		17	45	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{DD} = 15 \text{ V}, I_{D} = 30 \text{ A},$ $R_{G} = 25 \Omega$		155	320	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	NG = 23 22		10	30	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4,	5)	75	160	ns
Qg	Total Gate Charge	$V_{DS} = 24 \text{ V}, I_{D} = 60 \text{ A},$		18.5	24	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 5 V		7		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4,	5)	9.5		nC
	ource Diode Characteristics ar	nd Maximum Ratings			1	
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				60	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode F	de Forward Current			240	Α
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V, } I_{S} = 60 \text{ A}$			1.5	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_{S} = 60 \text{ A},$		40		ns
٩rr	,	$dI_F / dt = 100 A/\mu s$ (Note				

**Notes:**1. Repetitive Rating : Pulse width limited by maximum junction temperature 2. L = 60μH, I<sub>AS</sub> = 60A, V<sub>DD</sub> = 15V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C 3. I<sub>SD</sub> ≤ 60A, di/dt ≤ 300A/μs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, Starting T<sub>J</sub> = 25°C 4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2% 5. Essentially independent of operating temperature

# **Typical Characteristics**

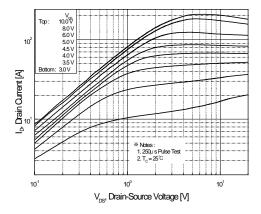


Figure 1. On-Region Characteristics

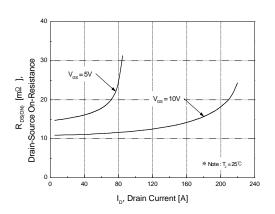


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

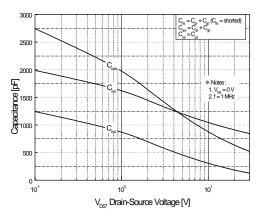


Figure 5. Capacitance Characteristics

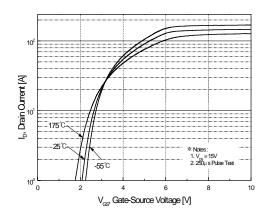


Figure 2. Transfer Characteristics

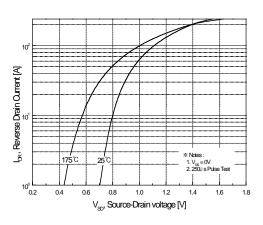


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

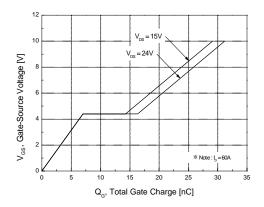


Figure 6. Gate Charge Characteristics

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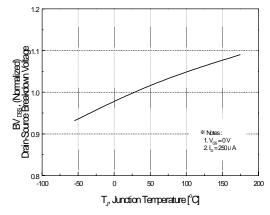


Figure 7. Breakdown Voltage Variation vs. Temperature

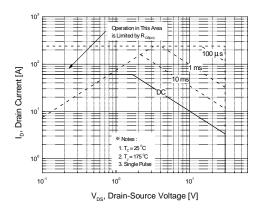


Figure 9. Maximum Safe Operating Area

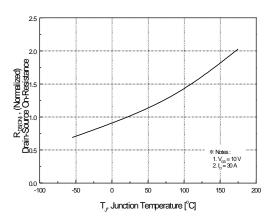


Figure 8. On-Resistance Variation vs. Temperature

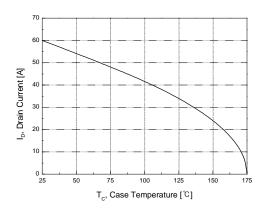


Figure 10. Maximum Drain Current vs. Case Temperature

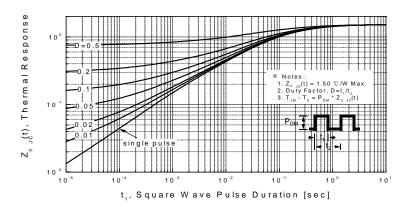
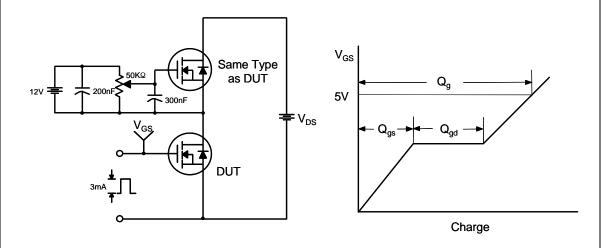


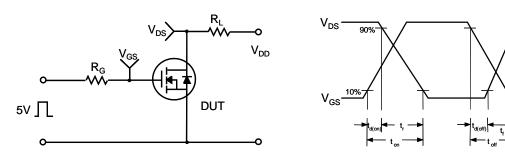
Figure 11. Transient Thermal Response Curve

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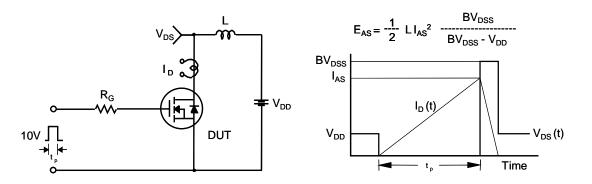
#### **Gate Charge Test Circuit & Waveform**



#### **Resistive Switching Test Circuit & Waveforms**

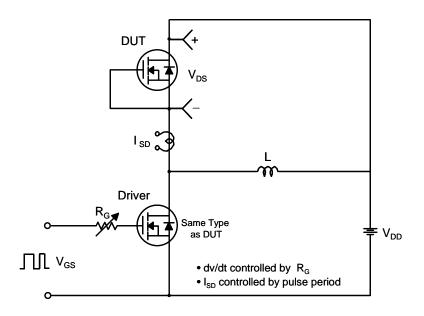


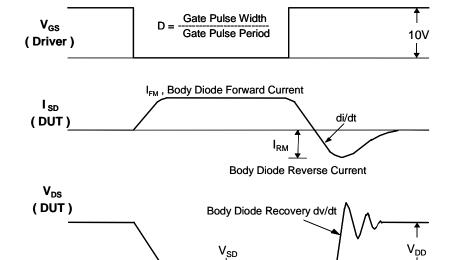
# **Unclamped Inductive Switching Test Circuit & Waveforms**



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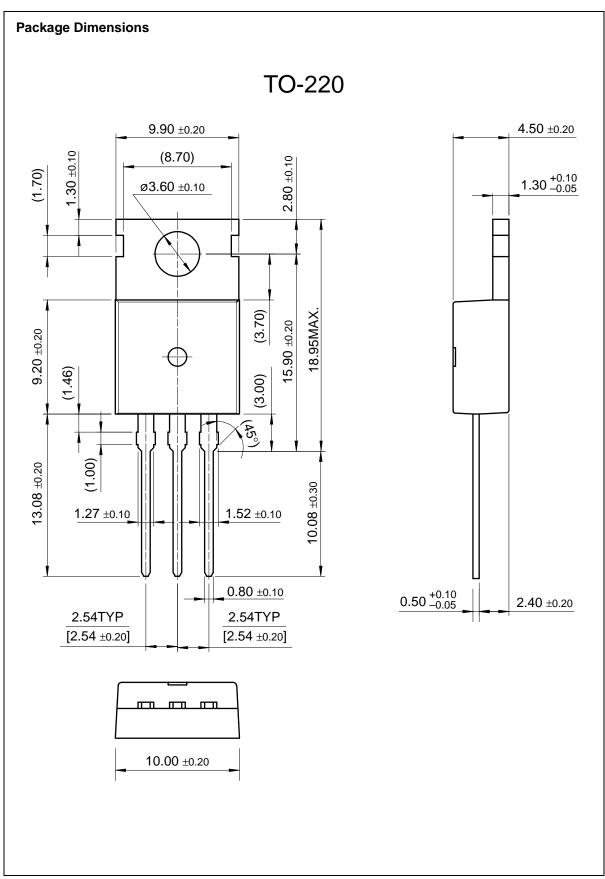
#### Peak Diode Recovery dv/dt Test Circuit & Waveforms





Body Diode Forward Voltage Drop

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