

March 1992 Revised August 1999

# 74FR74 • 74FR1074 Dual D-Type Flip-Flop

### **General Description**

The 74FR74 and 74FR1074 are dual D-type flip-flops with true and complement ( $Q/\overline{Q}$ ) outputs. On the 74FR74, data at the D inputs is transferred to the outputs on the rising edge of the clock input (CP<sub>n</sub>). The 74FR1074 is the negative edge triggered version of this device. Both parts feature asynchronous clear (C<sub>Dn</sub>) and set (S<sub>Dn</sub>) inputs which are low level enabled.

### **Features**

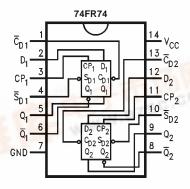
- 74FR74 is pin-for-pin compatible with the 74F74
- True 150 MHz f<sub>MAX</sub> capability on 74FR74
- Outputs sink 24 mA and source 24 mA
- Guaranteed pin-to-pin skew specifications

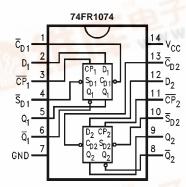
### **Ordering Code:**

Order Number	Package Number	Package Description
74FR74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74FR74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74FR1074SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
74FR1074PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

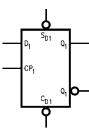
### **Connection Diagrams**

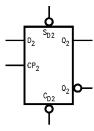




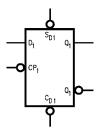
# **Logic Symbols**

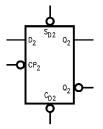






74FR1074





# **Pin Descriptions**

Pin Names	Description
D <sub>n</sub>	Data Inputs
CP <sub>n</sub>	Clock Inputs
S <sub>Dn</sub>	Asynchronous Set Inputs
C <sub>Dn</sub>	Asynchronous Clear Inputs
Q <sub>n</sub>	True Output
$\overline{Q}_n$	Complementary Output

## **Truth Tables**

### 74FR74

	Inp	Out	puts		
SD	SD CD CP D				Q
L	Н	Х	Х	Н	L
Н	L	X	X	L	Н
L	L	X	X	Н	Н
Н	Н	~	Н	Н	L
Н	Н	~	L	L	Н
Н	Н	L	Χ	$Q_0$	$\overline{Q}_0$

- H = HIGH Voltage Level
  L = LOW Voltage Level
  Z = High Impedance
  X = Immaterial

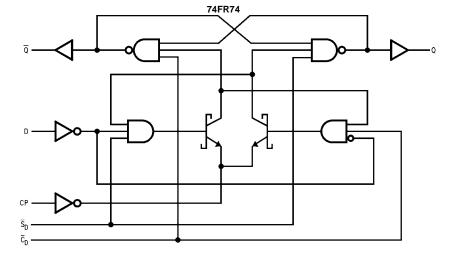
  → = Rising Edge
  Q<sub>0</sub> = Previous Q(\overline{Q}) before LOW-to-HIGH Clock Transition

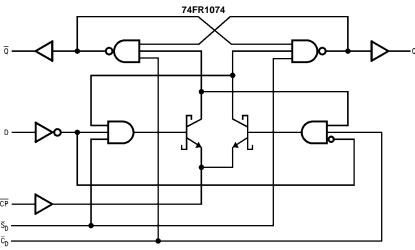
#### 74FR1074

	Inp	Out	puts		
SD	CD	СР	D	Q	Q
L	Н	Х	Х	Н	L
Н	L	X	X	L	Н
L	L	X	Χ	Н	Н
Н	Н	$\sim$	Н	Н	L
Н	Н	$\sim$	L	L	Н
Н	Н	L	Χ	$Q_0$	$\overline{Q}_0$

- $H = HIGH \ Voltage \ Level \\ L = LOW \ Voltage \ Level \\ Z = High \ Impedance \\ X = Immaterial \\ \sim = Falling \ Edge \\ Q_0 = Previous \ Q(\overline{Q}) \ before \ HIGH-to-LOW \ Clock \ Transition$

# **Logic Diagrams**





Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

### **Absolute Maximum Ratings**(Note 1)

 $\begin{array}{ll} \mbox{Storage Temperature} & -65\mbox{°C to } +150\mbox{°C} \\ \mbox{Ambient Temperature under Bias} & -55\mbox{°C to } +125\mbox{°C} \\ \end{array}$ 

Junction Temperature under Bias  $-55^{\circ}$ C to +150 $^{\circ}$ C V<sub>CC</sub> Pin Potential to Ground Pin -0.5V to +7.0V Input Voltage (Note 2) -0.5V to +7.0V

Input Current (Note 2) –30 mA to +5.0 mA

Voltage Applied to Output

in HIGH State (with  $V_{CC} = 0V$ )

Standard Output -0.5V to  $V_{CC}$ 

Current Applied to Output

in LOW State (Max) twice the rated  $I_{OL}$  (mA) ESD Last Passing Voltage (Min) 2000V

# Recommended Operating Conditions

Free Air Ambient Temperature  $0^{\circ}$ C to  $+70^{\circ}$ C Supply Voltage +4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

### **DC Electrical Characteristics**

Symbol	Parameter	Min	Тур	Max	Units	v <sub>cc</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
<sub>′он</sub>	Output HIGH	2.5			V	Min	I <sub>OH</sub> = -1 mA
	Voltage	2.4			V	Min	$I_{OH} = -3 \text{ mA}$
		2.0			V	Min	I <sub>OH</sub> = -24 mA
/ <sub>OL</sub>	Output LOW Voltage			0.5	V	Min	I <sub>OL</sub> = 24 mA
IH	Input HIGH Current			5	μΑ	Max	V <sub>IN</sub> = 2.7V
BVI	Input HIGH Current			7	μА	Max	V <sub>IN</sub> = 7.0V
	Breakdown Test			,	μΑ	IVIAX	VIN = 7.0V
IL	Input LOW Current			-150	μΑ	Max	$V_{IN} = 0.5V (D_n, CP_n)$
				-1.8	mA	Max	$V_{IN} = 0.5V (C_{Dn}, S_{Dn})$
/ <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9 \mu A$ ,
							All Other Pins Grounded
OD	Output Circuit			3.75	V	0.0	$V_{IOD} = 150 \text{ mV},$
	Leakage Test						All Other Pins Grounded
os	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
CEX	Output HIGH			50	μΑ	Max	V <sub>OUT</sub> = V <sub>CC</sub>
	Leakage Current						
Icc	Power Supply Current			24	mA	Max	

### **AC Electrical Characteristics 74FR74**

Symbol	Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$			$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$	
		Min	Тур	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	150	190		150		MHz
t <sub>PLH</sub>	Propagation Delay	2.5	3.5	5.0	2.5	5.0	
t <sub>PHL</sub>	$CP_n$ to $Q_n$ or $\overline{Q}_n$	2.5	4.5	6.0	2.5	6.0	ns
t <sub>PLH</sub>	Propagation Delay	1.5	3.5	5.5	1.5	5.5	ns
t <sub>PHL</sub>	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$	2.0	5.5	7.0	2.0	7.0	
toshl	Pin to Pin Skew					1.0	ns
(Note 3)	for HL Transitions					1.0	115
toslh	Pin to Pin Skew					1.0	ns
(Note 3)	for LH Transitions					1.0	115
t <sub>OST</sub>	Pin to Pin Skew					3.0	ns
(Note 3)	for HL/LH Transitions					3.0	115
t <sub>Q/Q</sub>	True/Complement					1.8	no
(Note 3)	Output Skew					1.0	ns
t <sub>PS</sub>	Pin (Signal)					1.8	ns
(Note 3)	Transition Variation					1.0	IIS

Note 3: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>) or in opposite directions both HL and LH (t<sub>OST</sub>). t<sub>OST</sub> is guaranteed by design.

## **AC Operating Requirements** 74FR74

Symbol	Parameter		$T_A = +25$ °C $V_{CC} = +5.0V$ $C_L = 50$ pF		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50$ pF	
		Min	Max	Min	Max	1
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	2.5		2.5		ns
t <sub>S</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	2.5		2.5		115
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0		0		ns
t <sub>H</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	0		0		115
t <sub>W</sub> (H)	CP <sub>n</sub> Pulse Width	3.3		3.3		ns
$t_W(L)$	HIGH or LOW	3.3		3.3		115
(Note 4)						
t <sub>W</sub> (L)	$\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ Pulse Width	4.0		4.0		ns
t <sub>REC</sub>	Recovery Time	2.0		2.0		ns
	$\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ to $CP_n$					

Note 4: This specification is guaranteed by design.

### **AC Electrical Characteristics** 74FR1074

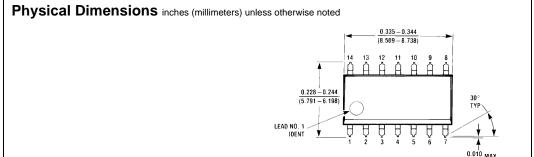
Symbol	Parameter		$T_A = +25^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		$T_A = 0$ °C to +70°C $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
		Min	Тур	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	120	160		120		MHz
t <sub>PLH</sub>	Propagation Delay	2.5	4.0	5.5	2.5	5.5	no
t <sub>PHL</sub>	$CP_n$ to $Q_n$ or $\overline{Q}_n$	3.0	5.0	6.5	3.0	6.5	ns
t <sub>PLH</sub>	Propagation Delay	1.5	3.5	5.5	1.5	5.5	ns
t <sub>PHL</sub>	$\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$	2.0	5.5	7.0	2.0	7.0	
t <sub>OSHL</sub>	Pin to Pin Skew					1.5	ns
(Note 5)	for HL Transitions					1.5	115
toslh	Pin to Pin Skew					1.5	ns
(Note 5)	for LH Transitions					1.5	113
t <sub>OST</sub>	Pin to Pin Skew					3.5	ns
(Note 5)	for HL/LH Transitions					5.5	113
t <sub>Q/Q</sub>	True/Complement					2.0	ns
(Note 5)	Output Skew					2.0	115
t <sub>PS</sub>	Pin (Signal)					2.0	ns
(Note 5)	Transition Variation					2.0	113

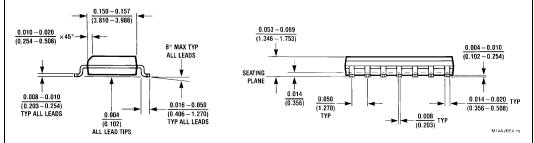
Note 5: Pin-to-Pin Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>) or in opposite directions both HL and LH (t<sub>OST</sub>). t<sub>OST</sub> is guaranteed by design.

## **AC Operating Requirements** 74FR1074

Symbol	Parameter	$T_A = +25$ °C $V_{CC} = +5.0$ V $C_L = 50$ pF		$T_A = 0^{\circ}C = +70^{\circ}C$ $V_{CC} = +5.0V$ $C_L = 50 \text{ pF}$		Units
		Min	Max	Min	Max	
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	2.0		2.0		ns
t <sub>S</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	2.0		2.0		115
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0		0		ns
t <sub>H</sub> (L)	D <sub>n</sub> to CP <sub>n</sub>	0		0		115
t <sub>W</sub> (H)	CP <sub>n</sub> Pulse Width	3.3		3.3		ns
t <sub>W</sub> (L)	HIGH or LOW	3.3		3.3		115
(Note 6)						
t <sub>W</sub> (L)	$\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ Pulse Width	4.0		4.0		ns
t <sub>REC</sub>	Recovery Time $\overline{S}_{Dn}$ or $\overline{C}_{Dn}$ to $\operatorname{CP}_n$	2.0		2.0		ns

Note 6: This specification is guaranteed by design.





14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow Package Number M14A

#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770 (18.80 - 19.56)ก กฤก (2.286) 14 13 12 11 10 9 8 14 13 12 INDEX AREA $0.250 \pm 0.010$ (6.350 ± 0.254) PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 0.030 MAX $\frac{332}{(2.337)} \text{ DIA}$ (0.762) DEPTH OPTION 1 OPTION 02 $0.135 \pm 0.005$ 0.300 - 0.320 $(3.429 \pm 0.127)$ (7.620 - 8.128)0.145 - 0.200 0.060 4° TYP (1.651) (3.683 - 5.080)¥ $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 95° ± 5° 0.020 (0.508)0.125 - 0.150 $0.075 \pm 0.015$ 0.280 0.014-0.023 TYP (7.112) MIN $\frac{0.100 \pm 0.010}{(2.540 \pm 0.254)} \text{ TYP}$ (0.356 - 0.584) $\frac{0.050 \pm 0.010}{(1.270 - 0.254)}$ TYP 0.325 +0.040 -0.015 8.255 + 1.016 - 0.381

14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

N14A (REV F)