FAIRCHILD SEMICONDUCTOR™

April 1991
Revised August 1999

74FR9244
9-Bit Buffer/Line Driver with 3-STATE Outputs

General Description

The 74FR9244 is a non-inverting 9-bit buffer and line driver designed to be employed as memory and address driver, clock driver and bus-oriented transmitter/receiver.

Features

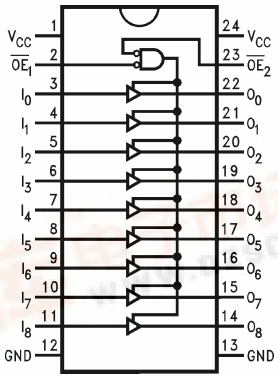
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA and source 15 mA
- Guaranteed multiple output switching, 250 pf delays and pin-to-pin skew
- Guaranteed 4000V minimum ESD protection
- 9-Bit architecture for systems carrying parity

Ordering Code:

Order Number	Package Number	Package Description
74FR9244SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74FR9244SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Pin Descriptions

Pin Names	Description
$\overline{OE}_1$,–$\overline{OE}_2$	Output Enable Input (Active-LOW)
I_0–I_8	Inputs
O_0–O_8	Outputs

Truth Table

$\overline{OE}_1$	$\overline{OE}_2$	I_n	O_n
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings(Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
Junction Temperature Under Bias	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
3-STATE Output	−0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	Twice The Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4			V	Min	I_{OH} = −3 mA
		2.0			V	Min	I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input HIGH Current			5	µA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	µA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−150	µA	Max	V_{IN} = 0.5V
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 µA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Current			3.75	µA	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
I_{OZH}	Output Leakage Current			20	µA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	µA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current			50	µA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test			100	µA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		30	40	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current		60	75	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current		35	45	mA	Max	Outputs 3-STATED
C_{IN}	Input Capacitance		8.0		pF	5.0	

AC Electrical Characteristics

Symbol	Parameter	$T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0	2.6	4.1	1.0	4.1	ns
t_{PHL}		1.0	1.8	4.1	1.0	4.1	
t_{PZH}	Output Enable Time	2.6	4.8	7.0	2.6	7.0	ns
t_{PZL}		2.6	3.9	7.0	2.6	7.0	
t_{PHZ}	Output Disable Time	1.6	3.7	6.1	1.6	6.1	ns
t_{PLZ}		1.6	3.6	6.1	1.6	6.1	

Extended AC Characteristics

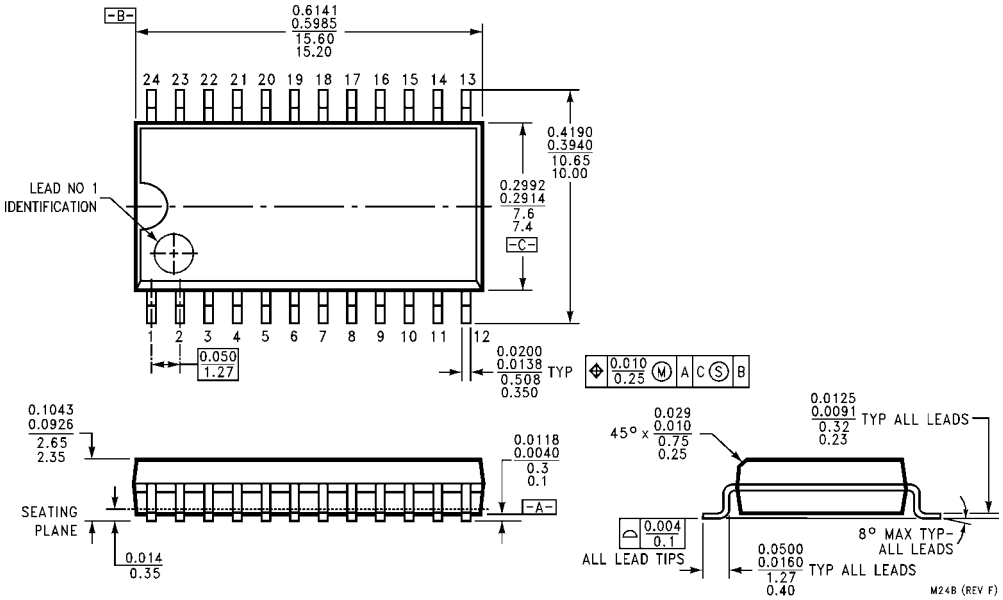
Symbol	Parameter	$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF, Eight Outputs Switching (Note 3)		$T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V$, $C_L = 250$ pF (Note 4)		Units
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.0	6.0	2.3	8.0	ns
t_{PHL}		1.0	6.0	2.3	8.0	
t_{PZH}	Output Enable Time	2.6	8.5			ns
t_{PZL}		2.6	8.5			
t_{PHZ}	Output Disable Time	1.6	6.5			ns
t_{PLZ}		1.6	6.5			
t_{OSHL}	Pin-to-Pin Skew for HL Transitions (Note 5)		1.3			ns
t_{OSLH}	Pin-to-Pin Skew for LH Transitions (Note 5)		1.7			ns
t_{OST}	Pin-to-Pin Skew for HL/LH Transitions (Note 5)		3.0			ns

Note 3: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all LOW-to-HIGH, HIGH-to-LOW, 3-STATE-to-HIGH, etc.

Note 4: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

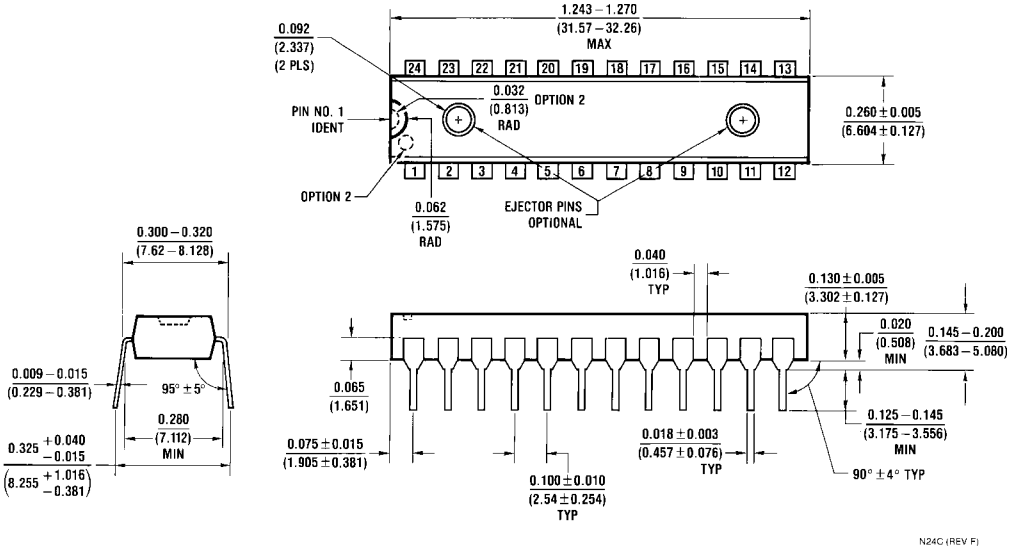
Note 5: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW, (t_{OSHL}), LOW-to-HIGH, (t_{OSLH}), or HIGH-to-LOW and/or LOW-to-HIGH, (t_{OST}). Specification guaranteed with all outputs switching in phase.

Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-100, 0.300 Wide
Package Number N24C