AMERICAN MICROSYSTEMS, INC.

FS612509-01/-02

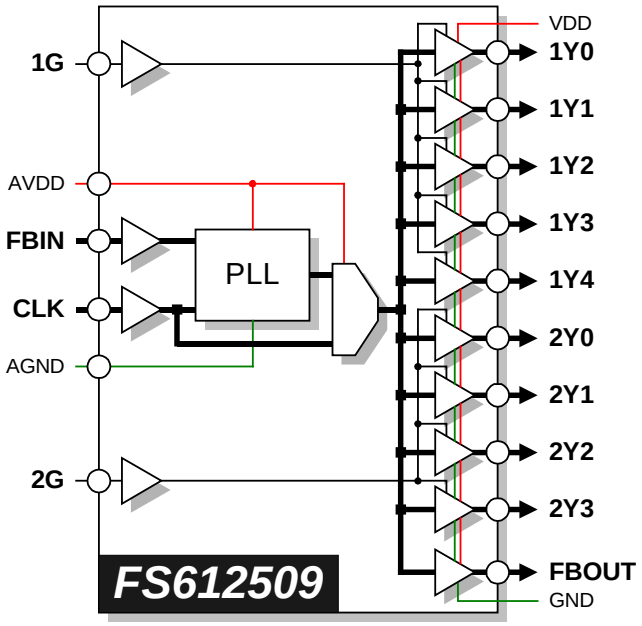
1:9 Zero-Delay Clock Buffer IC

November 2000

1.0 Features

- Generates one bank of five outputs (1Y0 to 1Y4) and one bank of four outputs (2Y0 to 2Y3) from one reference clock input (CLK)
- Designed to meet the PLL Component Specifications as noted in the PC133 SDRAM Registered DIMM Design Specification
- External feedback input (FBIN) to synchronize all clock outputs to the clock input
- Operating frequency: 25MHz to 140MHz
- Tight tracking skew (spread-spectrum tolerant)
- On-chip 25Ω series damping resistors for driving point-to-point loads
- Separate bank controls:
  - Signal 1G enables or disables outputs 1Y0 - 1Y4
  - Signal 2G enables or disables outputs 2Y0 - 2Y3
- Available with an auto power-down option that turns off the PLL and forces all outputs low when the reference clock stops (*FS612509-02*)
- Packaged in a 24-pin TSSOP

Figure 1: Block Diagram



2.0 Description

The FS612509 is a low skew, low jitter CMOS zero-delay phase-lock loop (PLL) clock buffer IC designed for high-speed motherboard applications, such as those using 133MHz SDRAM.

Nine buffered clock outputs are derived from an onboard open-loop PLL. The PLL aligns the frequency and phase of all output clocks to the input clock CLK, including an FBOUT clock that feeds back to FBIN to close the loop.

One group of five outputs 1Y0 to 1Y4 are enabled and disabled low by the active-high 1G signal. A second group of four outputs 2Y0 to 2Y3 are enabled and disabled low by the active-high 2G signal. The PLL may be bypassed by pulling AVDD to ground.

Figure 2: Pin Configuration

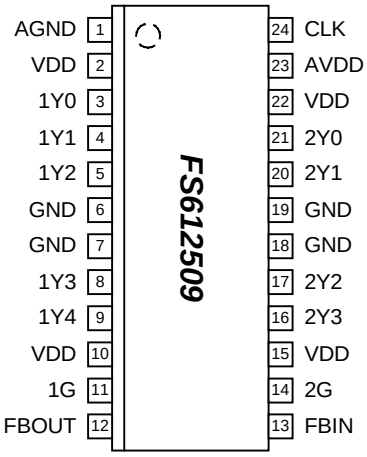


Table 1: Function Table

PLL	INPUT				OUTPUT		
	AVDD	1G	2G	CLK	1Y0-1Y4	2Y0-2Y3	FBOUT
Zero-Delay	H	L	L	H	L	L	H
	H	L	H	H	L	H	H
	H	H	L	H	H	L	H
	H	H	H	H	H	H	H
	H	H	H	L	L	L	L
PLL Bypass	L	L	L	H	L	L	H
	L	L	H	H	L	H	H
	L	H	L	H	H	L	H
	L	H	H	H	H	H	H
	L	H	H	L	L	L	L

Table 2: Pin Descriptions

Key: AI = Analog Input; AO = Analog Output; DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DI-3 = Three-Level Digital Input, DO = Digital Output; P = Power/Ground; # = Active Low pin

PIN	TYPE	NAME	DESCRIPTION	
11	DI	1G	Output enable stops Bank 1 clocks (1Y0 – 1Y4) in a low state when this pin is low	
14	DI	2G	Output enable stops Bank 2 clocks (2Y0 – 2Y3) in a low state when this pin is low	
3	DO	1Y0	Clock output	Bank 1 Enabled by 1G
4	DO	1Y1	Clock output	
5	DO	1Y2	Clock output	
8	DO	1Y3	Clock output	
9	DO	1Y4	Clock output	
21	DO	2Y0	Clock output	Bank 2 Enabled by 2G
20	DO	2Y1	Clock output	
17	DO	2Y2	Clock output	
16	DO	2Y3	Clock output	
23	P	AVDD	Power Supply / Test mode enable. This pin provides the power supply to the internal PLL. When the pin is pulled low, the PLL is bypassed and the output clocks directly follow the input clock	
1	P	AGND	PLL supply ground	
24	DI	CLK	Reference clock input (*Note: -02 version has a pull-down on this pin*)	
13	DI	FBIN	Feedback clock input, connected to FBOUT to complete the loop	
12	DO	FBOUT	Feedback output clock	
6, 7, 18, 19	P	GND	Ground for all clock outputs	
2, 10, 15, 22	P	VDD	Power supply for all clock outputs	

November 2000

3.0 Device Operation

The FS612509 is a zero-delay buffer intended for use on buffered PC133 SDRAM DIMMs.

The FS612509 precisely aligns the frequency and phase of the output clocks to the input CLK by use of an on-chip phase-lock loop (PLL). The PLL generates up to 9 low-skew, low-jitter copies of the CLK, with the outputs adjusted for 50% duty cycle.

The FBOUT clock must be hardwired to the FBIN pin to complete the loop. The PLL actively adjusts the output clocks so that there is no phase error between the reference clock (CLK) and the feedback clock (FBIN).

Since the device uses a PLL to lock the output clocks to the input clock, there is a power-up stabilization time that is required for the PLL to achieve phase lock.

Note that all inputs and outputs use LVCMOS signal levels.

3.1 PLL Bypass

When the AVDD pin is pulled low, the reference clock signal bypasses the PLL and is brought directly through to the outputs. The PLL is powered down, and device acts a fanout buffer.

Note that if AVDD is re-established, the PLL requires a power-up and stabilization time to lock to the input clock.

3.2 Power-Down

The FS612509-02 version provides an auto power-down feature that shuts off the PLL, drives all outputs low, and places the device into a low current state if the reference clock stops. The power-down circuit is level sensitive, and detects either a DC high or low on the CLK input.

3.3 Bank Output Enable/Disable

Two banks of clock outputs are available on this device. Each bank is independently enabled or disabled by the 1G or 2G enable signals.

The first bank consists of five outputs 1Y0 to 1Y4, and the clocks are enabled or disabled by the 1G signal. A logic-high on 1G enables the Bank 1 outputs to swing in phase with the reference clock CLK. A logic-low on 1G forces the Bank 1 to a logic-low state.

A second bank of four clock outputs consists of 2Y0 to 2Y3, and the clocks are enabled or disabled by the 2G signal. A logic-high on 2G enables the Bank 2 outputs to swing in phase with the reference clock CLK. A logic-low on 2G forces the Bank 2 to a logic-low state.

The function table Table 1 shows the effect of the 1G and 2G enable signals on the clock outputs.

4.0 Tracking Skew

PLL-based buffer ICs may be required to follow a spread-spectrum modulated reference clock for frequencies greater than 66MHz. Spread spectrum modulation limits peak EMI emissions by intentionally introducing jitter onto a clock signal, effectively spreading the peak energy over a range of frequencies.

A downstream PLL, contained in a clock buffer IC such as this one, must carefully track the modulated input reference clock. A measure of how closely the downstream PLL follows the modulated clock is called the tracking skew. To ensure a tight tracking skew, the loop bandwidth of a downstream PLL is increased and the loop phase angle is reduced over that of typical PLL-based clock generators.

The type of modulation profile used impacts tracking skew. The maximum frequency change occurs at the profile limits where the modulation changes the slew rate polarity. To track the sudden reversal in clock frequency, the downstream PLL must have a large loop bandwidth. The ability of the downstream PLL to catch up to the modulating clock is determined by the loop transfer function phase angle.

The spread-spectrum reference clock should be either a triangle-wave or a non-linear modulation profile, with a modulation frequency of 50kHz or less.

5.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage, dc, Clock Buffers (V_{SS} = ground)	AV_{DD}	V_{SS} - 0.5	7	V
Supply Voltage, dc, Core	V_{DD}	V_{SS} - 0.5	7	V
Input Voltage, dc	V_I	V_{SS} - 0.5	V_{DD} + 0.5	V
Output Voltage, dc	V_O	V_{SS} - 0.5	V_{DD} + 0.5	V
Input Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{IK}	-50	50	mA
Output Clamp Current, dc (V_I < 0 or V_I > V_{DD})	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage, Core and Outputs	V_{DD}	3.3V ± 10%	3.0	3.3	3.6	V
Ambient Operating Temperature Range	T_A		0		70	°C
Output Load Capacitance	C_L				15	pF
Input Frequency	f_{CLK}	CLK	50		140	MHz
Input Duty Cycle		CLK	40		60	%
Input Rise/Fall Time		CLK			3	ns

November 2000

Table 5: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic		f_{CLK} = 133.33MHz; V_{DD} = 3.3V		130		mA
Supply Current, Static	I_{DDL}	Outputs low; V_{DD} = 3.3V		3		mA
Output Enable Input (1G, 2G)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input Leakage Current	I_I		-5		5	µA
Clock Inputs (CLK, FBIN)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input Leakage Current	I_I	-01 version	-5		5	µA
		-02 version has a pull-down on CLK		28		
Input Loading Capacitance *	$C_{L(in)}$	As seen by an external clock driver		4		pF
Clock Outputs (1Y0:4, 2Y0:3, FBOUT)						
High-Level Output Source Current	I_{OH}	V_{DD} = 2.9V, V_O = 2.0V		-18	-12	mA
		V_{DD} = 3.7V, V_O = 2.0V		-35	-12	
Low-Level Output Sink Current	I_{OL}	V_{DD} = 2.9V, V_O = 0.8V	12	16		mA
		V_{DD} = 3.7V, V_O = 0.8V	12	17		
Output Impedance	z_O			33		Ω
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Source Current *	I_{OSH}	V_O = 0V; shorted for 30s, max.		-60		mA
Short Circuit Sink Current *	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		90		mA

Table 6: Clock Output Drive (1Y0:4, 2Y0:3, FBOUT)

Voltage	Low Drive Current (mA)		High Drive Current (mA)	
0.1 V	-47	-59	2	2
0.2 V	-45	-58	4	4
0.4 V	-43	-56	8	9
0.6 V	-40	-55	12	13
0.8 V	-38	-52	16	17
1.0 V	-35	-50	20	21
1.2 V	-32	-47	24	25
1.4 V	-29	-45	27	29
1.6 V	-26	-41	31	33
1.8 V	-22	-38	34	36
2.0 V	-18	-35	38	40
2.2 V	-15	-31	41	43
2.4 V	-10	-28	43	46
2.6 V	-6	-24	45	49
2.8 V	-2	-20	48	51
3.0 V	0	-15	49	53
3.3 V		-9		56
3.6 V		-2		59

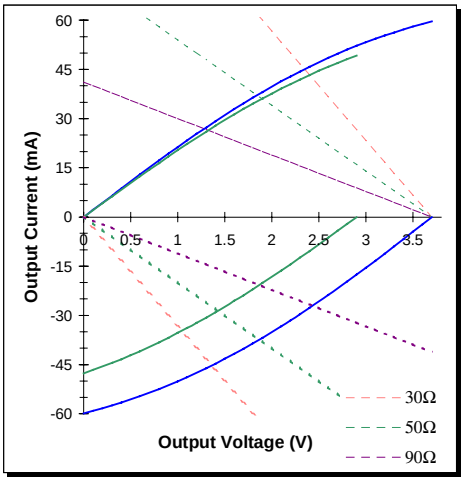


Table 7: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.3V, no load on any output, and ambient temperature T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ± 3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Skew, Output to Output *	$t_{sk(o)}$	Measured on the rising edge at 1.65V; C_L = 15pF			150	ps
Skew, Tracking *		Measured using a –0.5% 31.5kHz spread spectrum reference clock at 133.33MHz			150	ps
Static Phase Error *		From rising edge on CLK to rising edge on FBIN		-120		ps
Clock Stabilization Time *		Time required for the PLL to achieve phase lock			3	ms
Loop Bandwidth *		For calculation of Tracking Skew			1.2	MHz
Phase Angle *		For calculation of Tracking Skew			-0.031	°
Clock Outputs (1Y0:4, 2Y0:3, FBOUT)						
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at 1.65V	45		55	%
Jitter, Cycle-Cycle *	$t_{j(CC)}$	Adjacent cycles at 1.65V	-75		+75	ps
Jitter, Period (peak-peak) *	$t_{j(\Delta P)}$	From rising edge to next rising edge at 1.65V				
Rise Time *	t_r	V_O = 0.4V to 2.0V; C_L = 15pF		1.2		ns
Fall Time *	t_f	V_O = 2.0V to 0.4V; C_L = 15pF		1.4		ns
Enable Delay *	t_{DLH}	via 1G or 2G	1		10	ns
Disable Delay *	t_{DHL}	via 1G or 2G	1		10	ns

Figure 3: Clock Skew Measurement

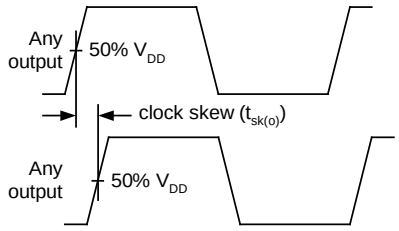


Figure 4: Phase Error Measurement

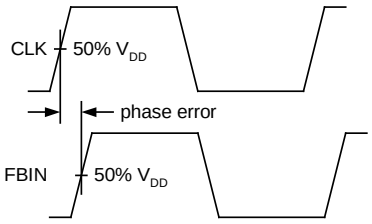


Figure 5: Timing Measurement Points

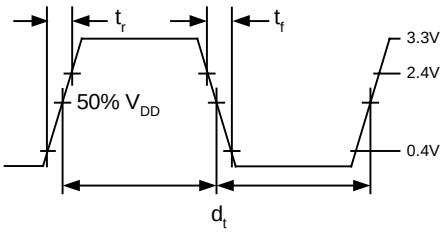
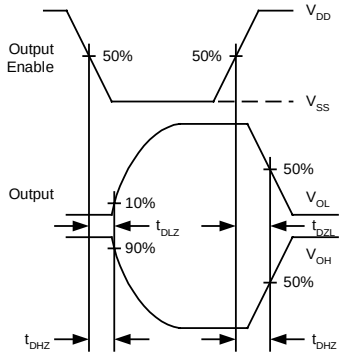


Figure 6: Output Enable Measurement



November 2000

6.0 Package Information

Table 8: 24-pin TSSOP Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.047	-	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.0315	0.0413	0.80	1.05
b	0.0075	0.0118	0.19	0.30
C	0.0035	0.0079	0.09	0.20
D	0.303	0.311	7.70	7.90
E_1	0.169	0.177	4.30	4.50
E	0.252		6.40 BSC	
e	0.0256		0.65 BSC	
L	0.0177	0.0295	0.45	0.75
S	0.0079	-	0.20	-
θ_1	0°	8°	0°	8°
θ_2	12 REF		12 REF	
θ_3	12 REF		12 REF	

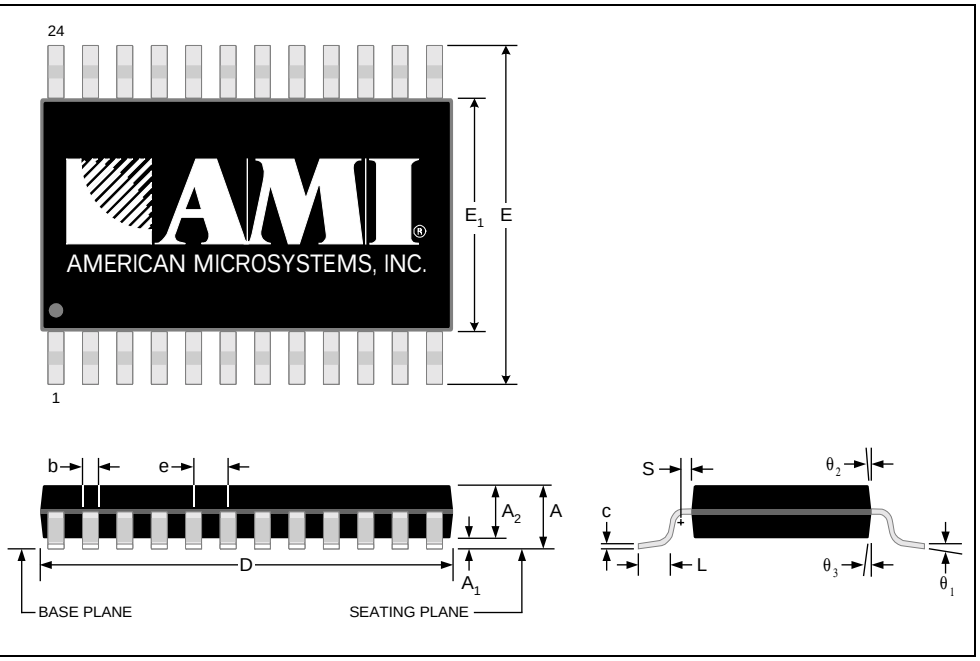


Table 9: 24-pin TSSOP Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	84	°C/W
Lead Inductance, Self	L_{11}	Longest lead	1.7	nH
Lead Inductance, Mutual	L_{12}	Longest lead to any 1st adjacent lead	0.6	nH
	L_{13}	Longest lead to any 2nd adjacent lead	0.24	
Lead Capacitance, Bulk	C_{11}	Longest lead to V_{SS}	0.3	pF
Lead Capacitance, Mutual	C_{12}	Longest lead to any 1st adjacent lead	0.1	pF
	C_{13}	Longest lead to any 2nd adjacent lead	0.007	

7.0 Ordering Information

Table 10: Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS612509-01	12055-802	24-pin TSSOP (Thin Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel
FS612509-02	12055-803	24-pin TSSOP (Thin Shrink Small Outline Package)	0°C to 70°C (Commercial)	Tape and Reel

American Microsystems, Inc., 2300 Buckskin Rd., Pocatello, ID 83201, (208) 233-4690, FAX (208) 234-6796, WWW Address: *http://www.amis.com* E-mail: *tgp@amis.com*