

International
IR Rectifier

SMPS MOSFET

PD - 91817A
IRFS9N60A

HEXFET® Power MOSFET

Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptable Power Supply
- High Speed Power Switching

V_{DSS}	R_{DS(on) max}	I_D
600V	0.75Ω	9.2A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current



Absolute Maximum Ratings

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V	9.2	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V	5.8	
I _{DM}	Pulsed Drain Current ①	37	
P _D @ T _C = 25°C	Power Dissipation	170	W
	Linear Derating Factor	1.3	W/°C
V _{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ②	5.0	V/ns
T _J	Operating Junction and	-55 to + 150	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Applicable Off Line SMPS Topologies:

- Active Clamped Forward
- Main Switch

Notes ① through ③ are on page 9
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Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	600	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.66	—	V/°C	Reference to 25°C, I _D = 1mA ^⑥
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.75	Ω	V _{GS} = 10V, I _D = 5.5A ^④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 600V, V _{GS} = 0V
		—	—	250		V _{DS} = 480V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -30V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g _{fs}	Forward Transconductance	5.5	—	—	S	V _{DS} = 25V, I _D = 3.1A
Q _g	Total Gate Charge	—	—	49	nC	I _D = 9.2A
Q _{gs}	Gate-to-Source Charge	—	—	13		V _{DS} = 400V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	20		V _{GS} = 10V, See Fig. 6 and 13 ^④
t _{d(on)}	Turn-On Delay Time	—	13	—		V _{DD} = 300V
t _r	Rise Time	—	25	—	ns	I _D = 9.2A
t _{d(off)}	Turn-Off Delay Time	—	30	—		R _G = 9.1Ω
t _f	Fall Time	—	22	—		R _D = 35.5Ω, See Fig. 10 ^④
C _{iss}	Input Capacitance	—	1400	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	180	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	7.1	—		f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	1957	—		V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz
C _{oss}	Output Capacitance	—	49	—		V _{GS} = 0V, V _{DS} = 480V, f = 1.0MHz
C _{oss eff.}	Effective Output Capacitance	—	96	—		V _{GS} = 0V, V _{DS} = 0V to 480V ^⑤

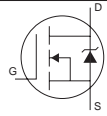
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E _{AS}	Single Pulse Avalanche Energy ^②	—	290	mJ
I _{AR}	Avalanche Current ^①	—	9.2	A
E _{AR}	Repetitive Avalanche Energy ^①	—	17	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	—	0.75	°C/W
R _{θJA}	Junction-to-Ambient (PCB Mounted, steady-state)	—	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	9.2	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ^①	—	—	37		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _J = 25°C, I _S = 9.2A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	530	800	ns	T _J = 25°C, I _F = 9.2A
Q _{rr}	Reverse Recovery Charge	—	3.0	4.4	μC	di/dt = 100A/μs ^④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

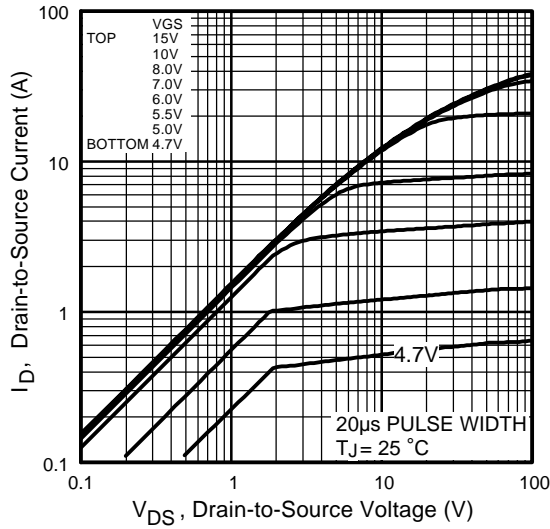


Fig 1. Typical Output Characteristics

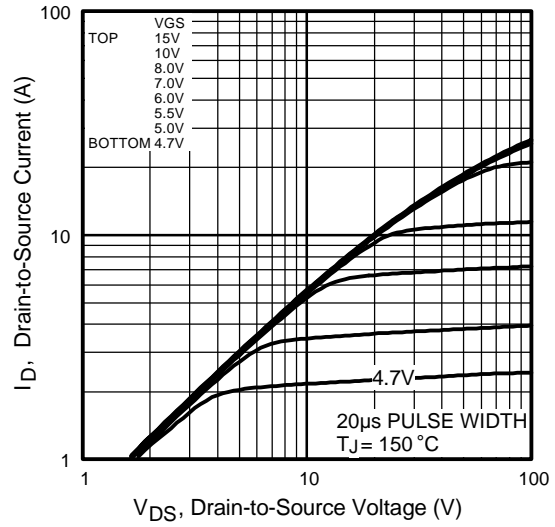


Fig 2. Typical Output Characteristics

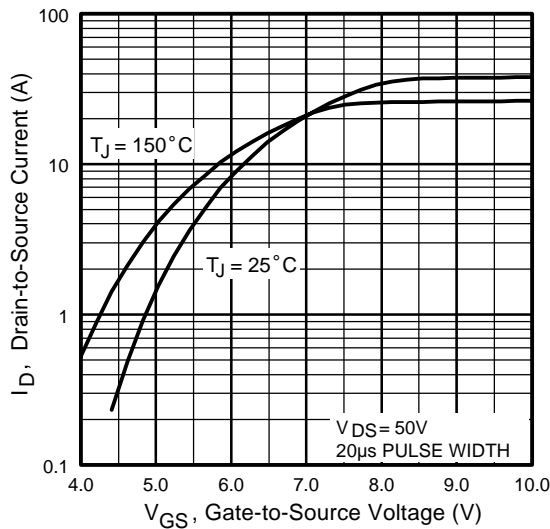


Fig 3. Typical Transfer Characteristics

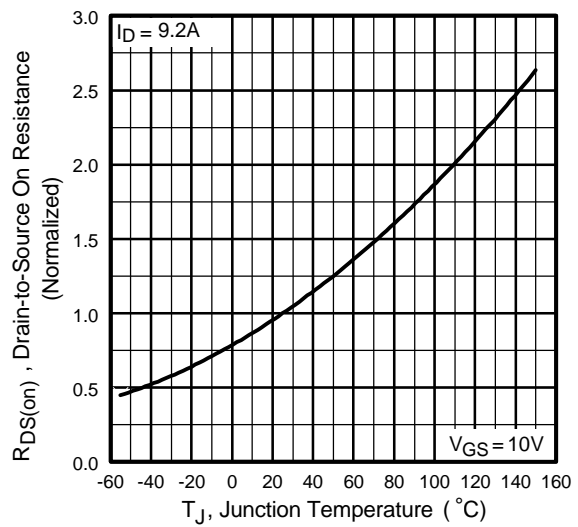


Fig 4. Normalized On-Resistance Vs. Temperature

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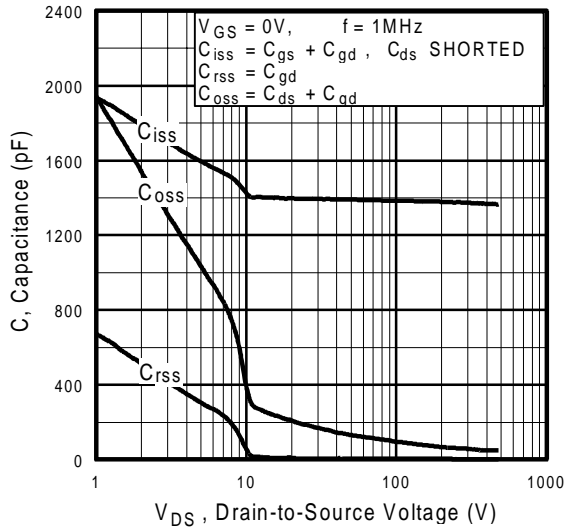


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

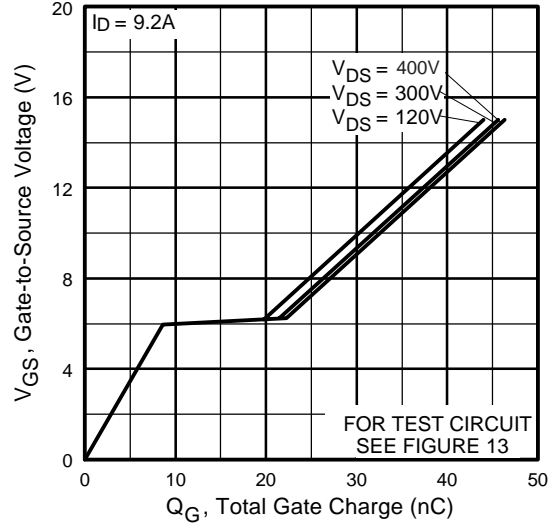


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

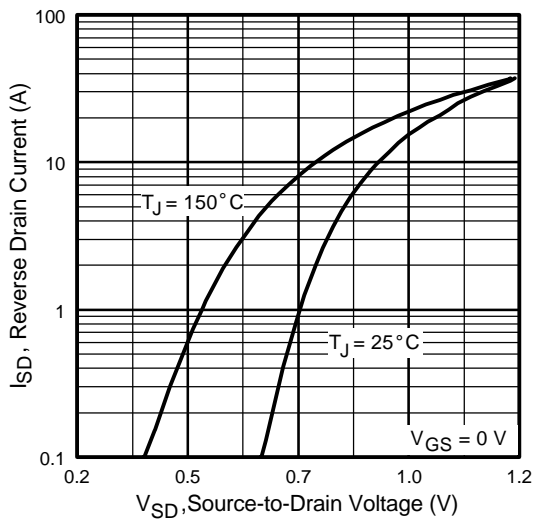


Fig 7. Typical Source-Drain Diode Forward Voltage

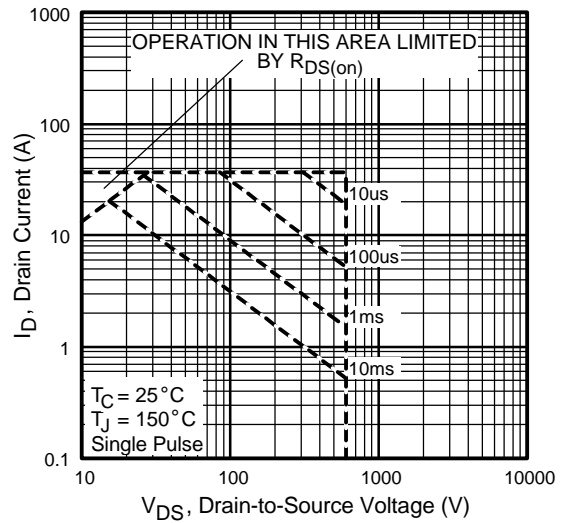


Fig 8. Maximum Safe Operating Area

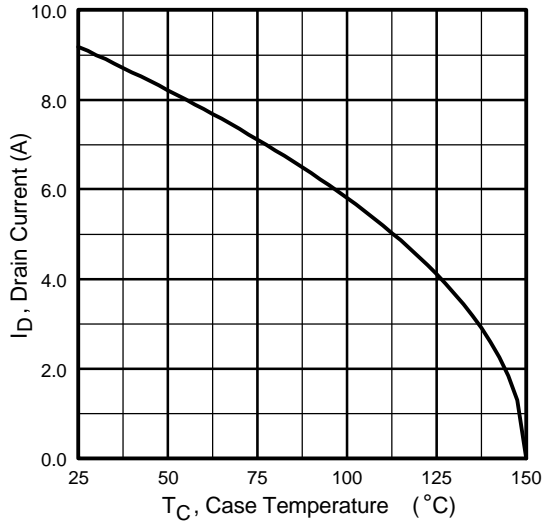


Fig 9. Maximum Drain Current Vs. Case Temperature

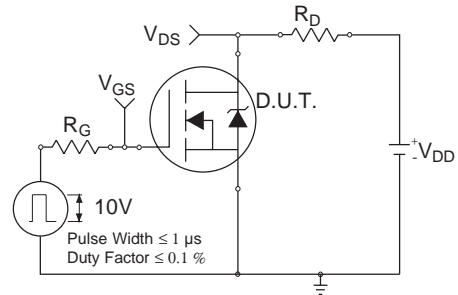


Fig 10a. Switching Time Test Circuit

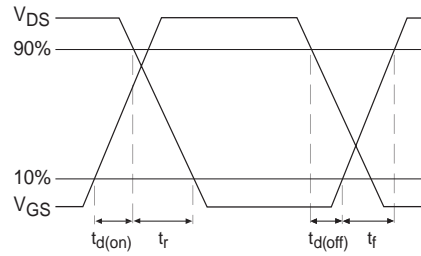


Fig 10b. Switching Time Waveforms

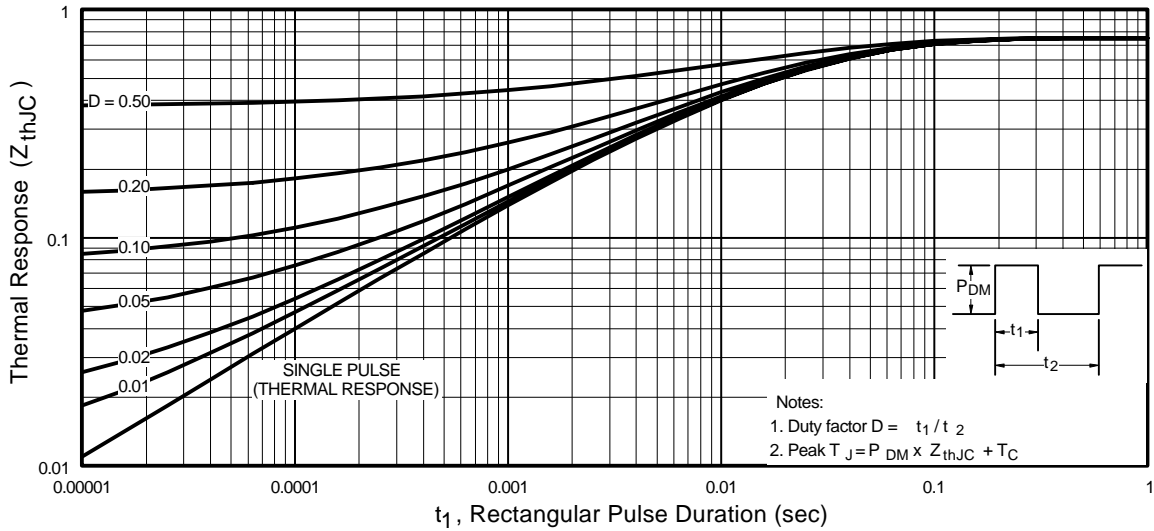


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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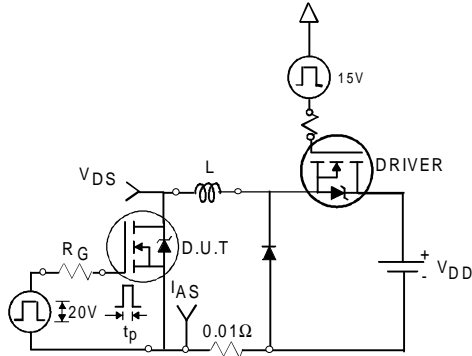


Fig 12a. Unclamped Inductive Test Circuit

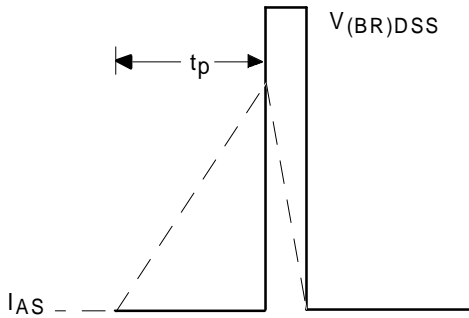


Fig 12b. Unclamped Inductive Waveforms

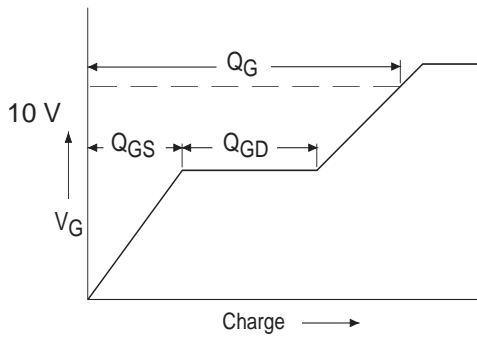


Fig 13a. Basic Gate Charge Waveform

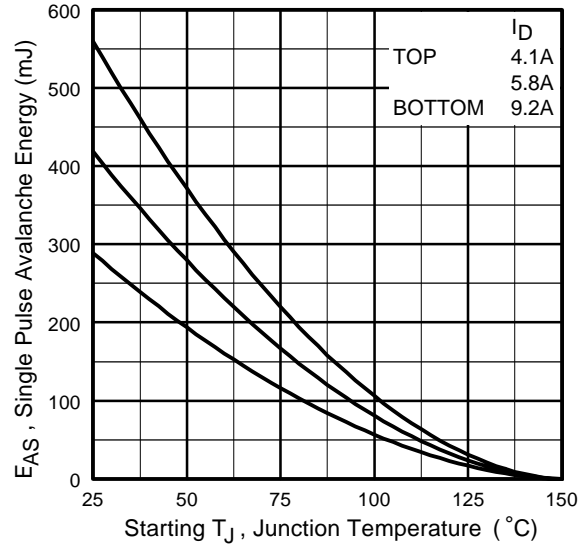


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

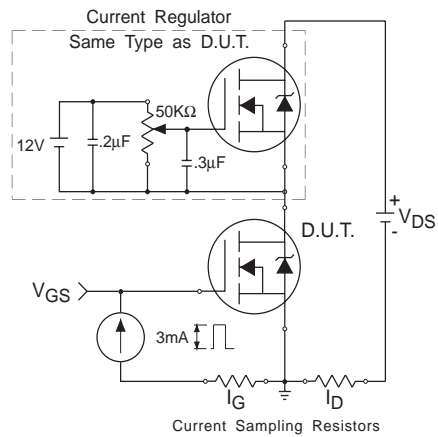
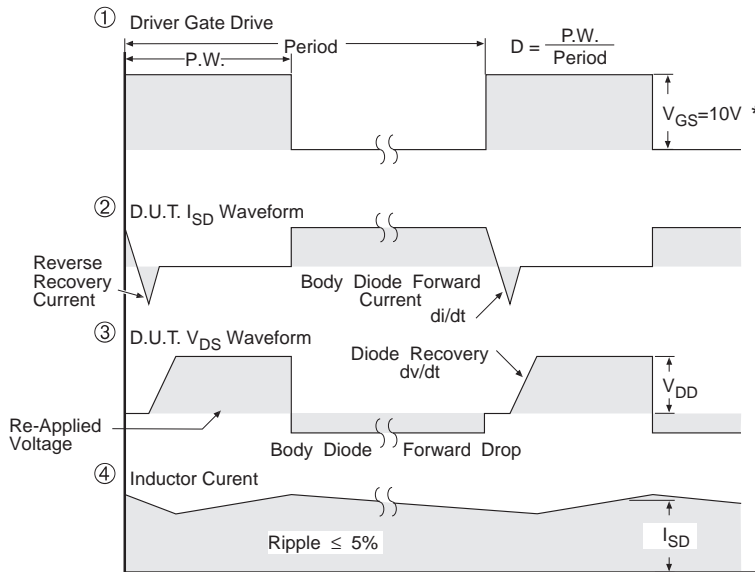
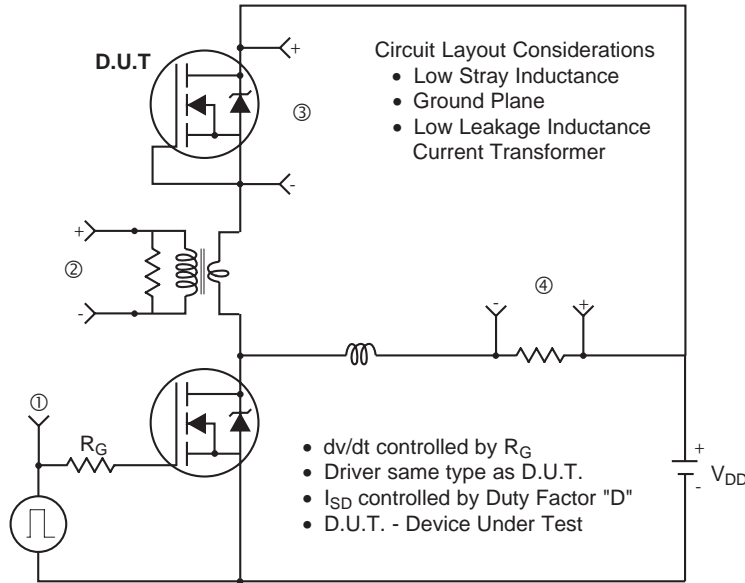


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



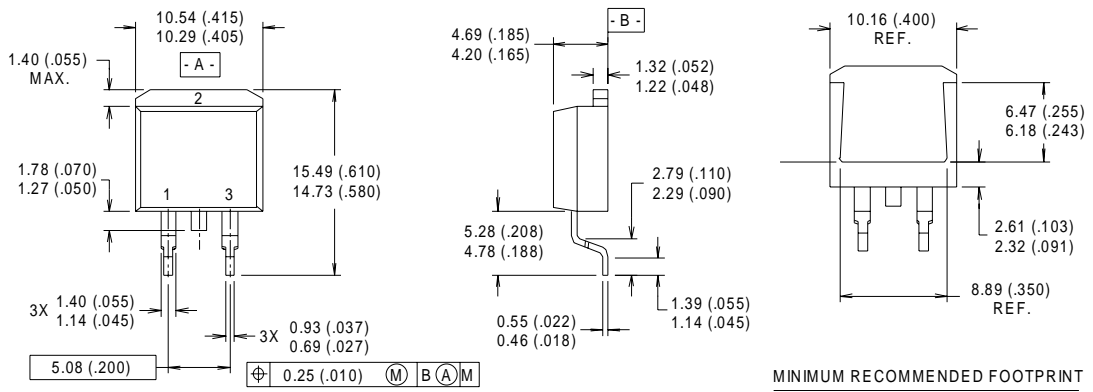
* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

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D²Pak Package Outline



NOTES:

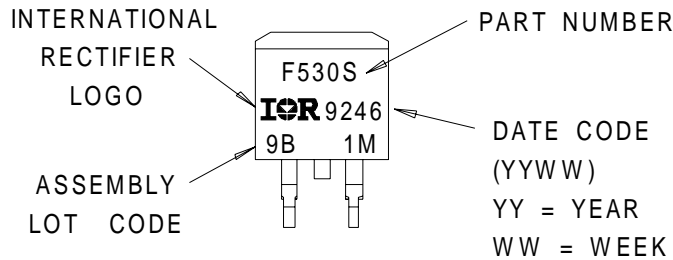
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

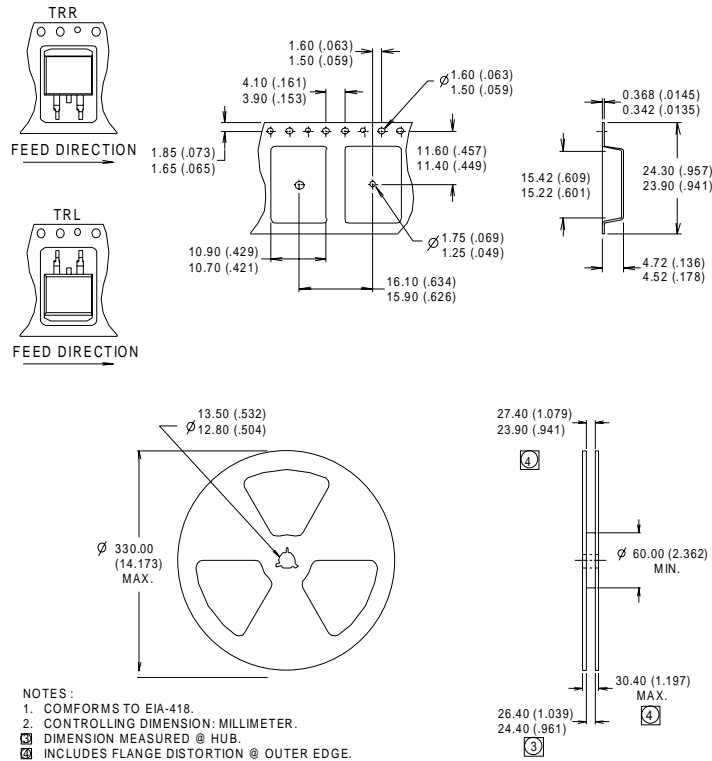
Part Marking Information

D²Pak



Tape & Reel Information

D²Pak



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 6.8\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 9.2\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 9.2\text{A}$, $di/dt \leq 50\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}