查询TC55V8512JI-15供应商 捷多邦，专业PCB打样工厂，24小时加急出货

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288-WORD BY 8-BIT CMOS STATIC RAM

DESCRIPTION

The TC55V8512JI/FTI is a 4,194,304-bit high-speed static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable ($\overline{CE}$) can be used to place the device in a low-power mode, and output enable ($\overline{OE}$) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V8512JI/FTI is available in plastic 36-pin SOJ and 44-pin TSOP with 400mil width for high density surface assembly. The TC55V8512JI/FTI guarantees –40° to 85°C operating temperature so it is suitable for use in wide operating temperature system.

FEATURES

- Fast access time (the following are maximum values)
  TC55V8512JI/FTI-12:12 ns
  TC55V8512JI/FTI-15:15 ns
- Low-power dissipation
  (the following are maximum values)

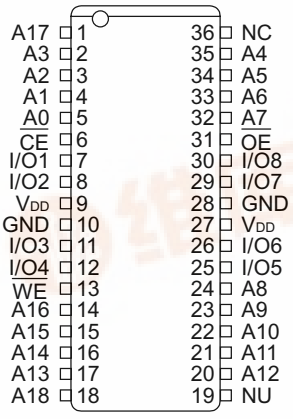
Cycle Time	12	15	20	25	ns
Operation (max)	180	150	140	120	mA

  Standby:10 mA (both devices)

- Single power supply voltage of 3.3 V ± 0.3 V
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using $\overline{OE}$
- Package:
  SOJ36-P-400-1.27 (JI) (Weight: 1.35 g typ)
  TSOP II44-P-400-0.80 (FTI) (Weight: 0.45 g typ)

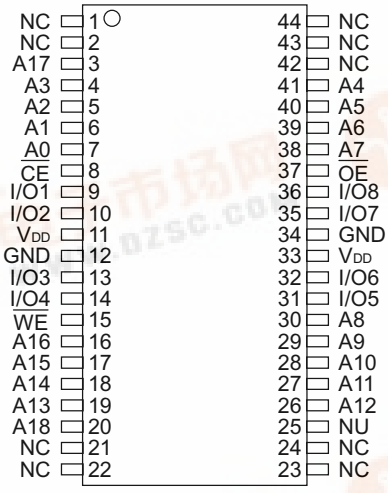
PIN ASSIGNMENT (TOP VIEW)

36 PIN SOJ



(TC55V8512JI)

44 PIN TSOP



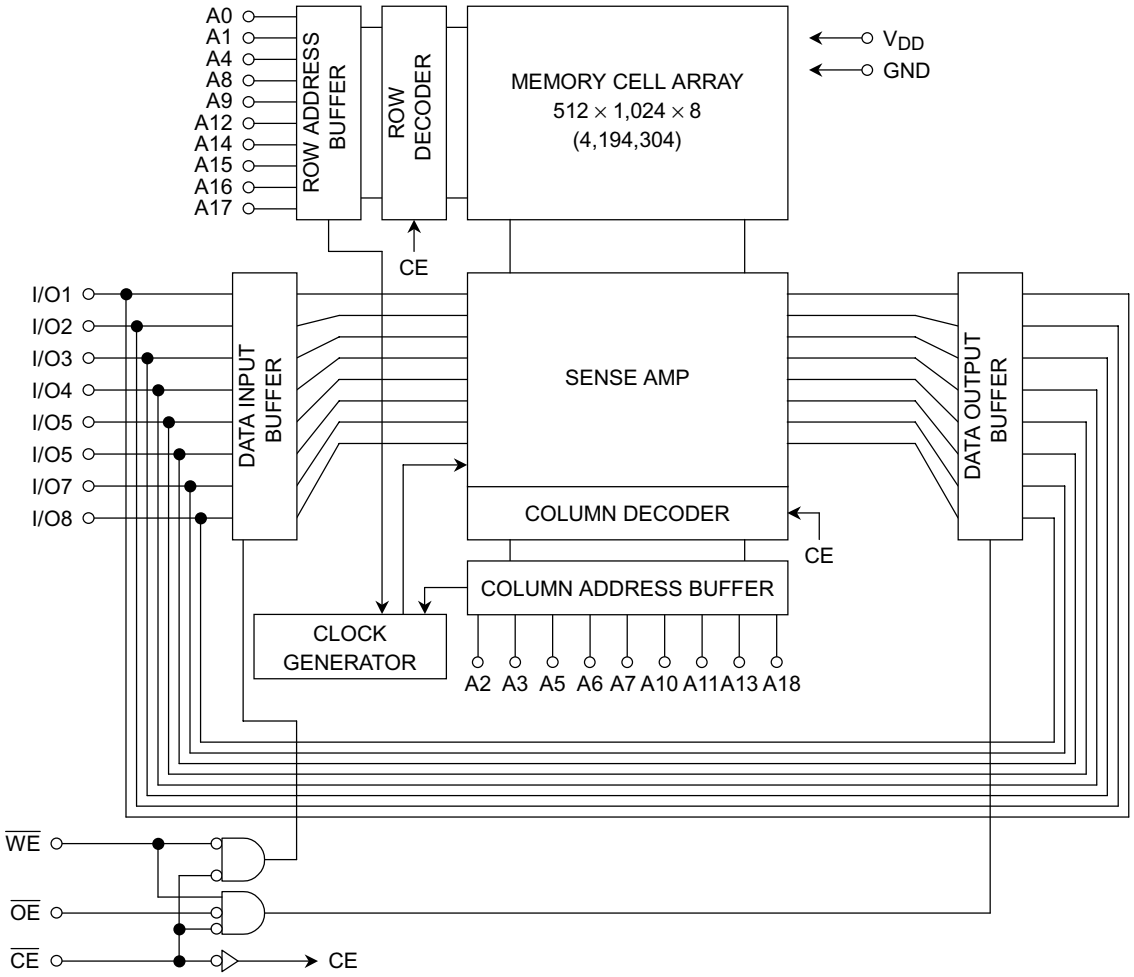
(TC55V8512FTI)

PIN NAMES

A0 to A18	Address Inputs
I/O1 to I/O8	Data Inputs/Outputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power (+3.3 V)
GND	Ground
NC	No Connection
NU	Not Usable (Input)

找PDF 维库一下 pdf.dzsc.com

BLOCK DIAGRAM



MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	−0.5 to 4.6	V
V_{IN}	Input Terminal Voltage	−0.5* to 4.6	V
$V_{I/O}$	Input/Output Terminal Voltage	−0.5* to V_{DD} + 0.5**	V
P_D	Power Dissipation	1.4	W
T_{solder}	Soldering Temperature (10s)	260	°C
T_{stg}	Storage Temperature	−65 to 150	°C
T_{opr}	Operating Temperature	−40 to 100	°C

*: −1.5 V with a pulse width of 20%・t_{RC} min (4 ns max)
**: V_{DD} + 1.5 V with a pulse width of 20%・t_{RC} min (4 ns max)

DC RECOMMENDED OPERATING CONDITIONS (Ta = –40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3**	V
V_{IL}	Input Low Voltage	−0.3*	—	0.8	V

*: −1.0 V with a pulse width of 20%・t_{RC} min (4 ns max)
**: V_{DD} + 1.0 V with a pulse width of 20%・t_{RC} min (4 ns max)

DC CHARACTERISTICS (Ta = –40° to 85°C, V_{DD} = 3.3 V ± 0.3 V)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current (Except NU pin)	V_{IN} = 0 to V_{DD}		–1	—	1	μA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH}, V_{OUT} = 0 to V_{DD}		–1	—	1	μA
$I_{I\ (NU)}$	Input Current (NU pin)	V_{IN} = 0 to 0.8 V		–1	—	20	μA
		V_{IN} = 0 to 0.2 V		–1	—	1	
V_{OH}	Output High Voltage	I_{OH} = –2 mA		2.4	—	—	V
		I_{OH} = –100 μA		V_{DD} – 0.2	—	—	
V_{OL}	Output Low Voltage	I_{OL} = 2 mA		—	—	0.4	
		I_{OL} = 100 μA		—	—	0.2	
I_{DDO}	Operating Current	$\overline{CE}$ = V_{IL}, I_{OUT} = 0 mA, $\overline{OE}$ = V_{IH}, Other Input = V_{IH}/V_{IL}	t_{cycle} = 12 ns	—	—	180	mA
			t_{cycle} = 15 ns	—	—	150	
			t_{cycle} = 20 ns	—	—	140	
			t_{cycle} = 25 ns	—	—	120	
I_{DDS1}	Standby Current	$\overline{CE}$ = V_{IH}, Other Input = V_{IH} or V_{IL}		—	—	55	mA
I_{DDS2}		$\overline{CE}$ = V_{DD} – 0.2 V, Other Input = V_{DD} – 0.2 V or 0.2 V		—	—	10	

CAPACITANCE (Ta = 25°C, f = 1 .0 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = GND	8	pF

Note: This parameter is periodically sampled and is not 100% tested.

OPERATING MODE

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O1 to I/O8	POWER
Read	L	L	H	Output	I_{DDO}
Write	L	*	L	Input	I_{DDO}
Outputs Disable	L	H	H	High Impedance	I_{DDO}
Standby	H	*	*	High Impedance	I_{DDS}

* : Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V.
You must not apply a voltage of more than 0.8 V to the NU.

AC CHARACTERISTICS (Ta = –40° to 85°C (See Note 1), V_{DD} = 3.3 V ± 0.3 V)

READ CYCLE

SYMBOL	PARAMETER	TC55V8512JI/FTI				UNIT
		-12		-15		
		MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	12	—	15	—	ns
t_{ACC}	Address Access Time	—	12	—	15	
t_{CO}	Chip Enable Access Time	—	12	—	15	
t_{OE}	Output Enable Access Time	—	6	—	8	
t_{OH}	Output Data Hold Time from Address Change	3	—	4	—	
t_{COE}	Output Enable Time from Chip Enable	3	—	4	—	
t_{OEE}	Output Enable Time from Output Enable	1	—	1	—	
t_{COD}	Output Disable Time from Chip Enable	—	7	—	8	
t_{ODO}	Output Disable Time from Output Enable	—	7	—	8	

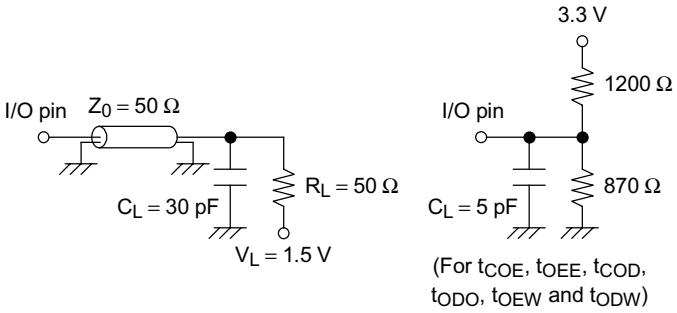
WRITE CYCLE

SYMBOL	PARAMETER	TC55V8512JI/FTI				UNIT
		-12		-15		
		MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	12	—	15	—	ns
t_{WP}	Write Pulse Width	8	—	9	—	
t_{CW}	Chip Enable to End of Write	10	—	12	—	
t_{AW}	Address Valid to End of Write	10	—	12	—	
t_{AS}	Address Setup Time	0	—	0	—	
t_{WR}	Write Recovery Time	0	—	0	—	
t_{DS}	Data Setup Time	7	—	8	—	
t_{DH}	Data Hold Time	0	—	0	—	
t_{OEW}	Output Enable Time from Write Enable	1	—	1	—	
t_{ODW}	Output Disable Time from Write Enable	—	7	—	8	

AC TEST CONDITIONS

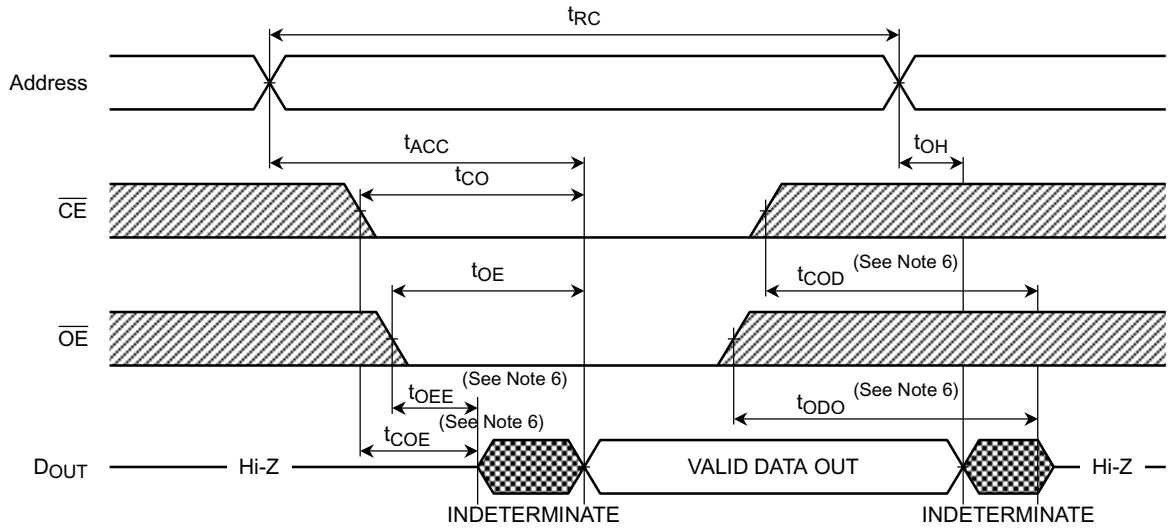
PARAMETER	TEST CONDITION
Input Pulse Level	3.0 V/ 0.0 V
Input Pulse Rise and Fall Time	2 ns
Input Timing Measurement Reference Level	1.5 V
Output Timing Measurement Reference Level	1.5 V
Output Load	Fig.1

Fig.1

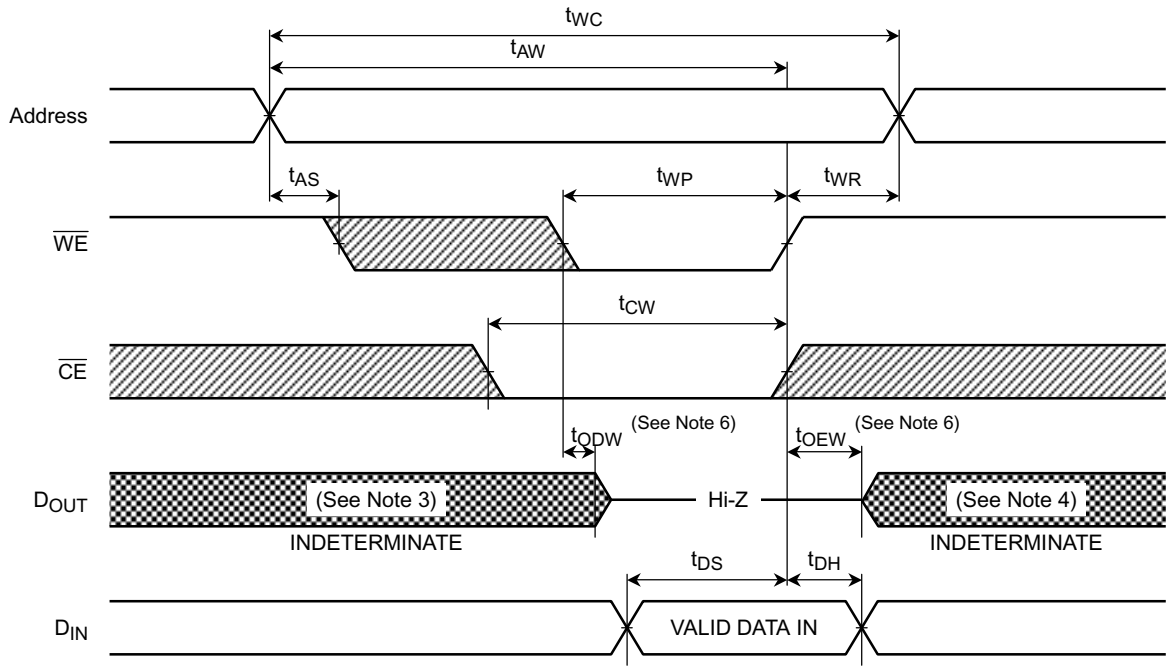


TIMING DIAGRAMS

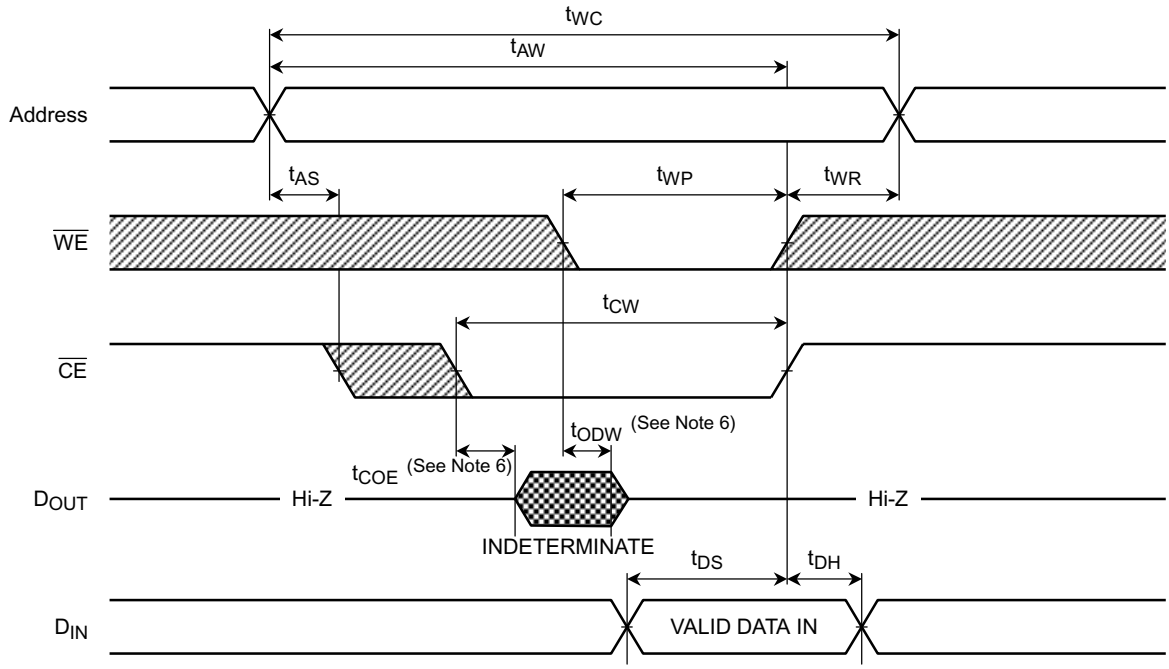
READ CYCLE (See Note 2)



WRITE CYCLE 1 ($\overline{WE}$ CONTROLLED) (See Note 5)



WRITE CYCLE 2 ($\overline{CE}$ CONTROLLED) (See Note 5)



Note:

(1) Operating temperature (Ta) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2) $\overline{WE}$ remains HIGH for the Read Cycle.

(3) If $\overline{CE}$ goes LOW coincident with or after $\overline{WE}$ goes LOW, the outputs will remain at high impedance.

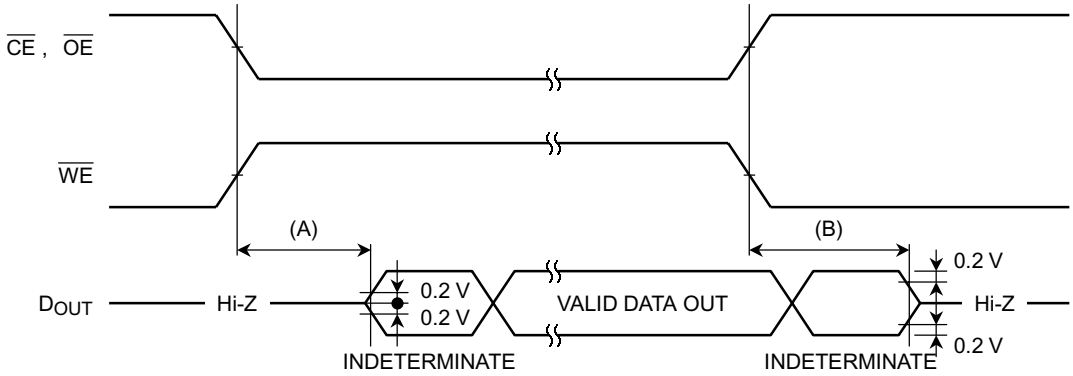
(4) If $\overline{CE}$ goes HIGH coincident with or before $\overline{WE}$ goes HIGH, the outputs will remain at high impedance.

(5) If $\overline{OE}$ is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig.1.

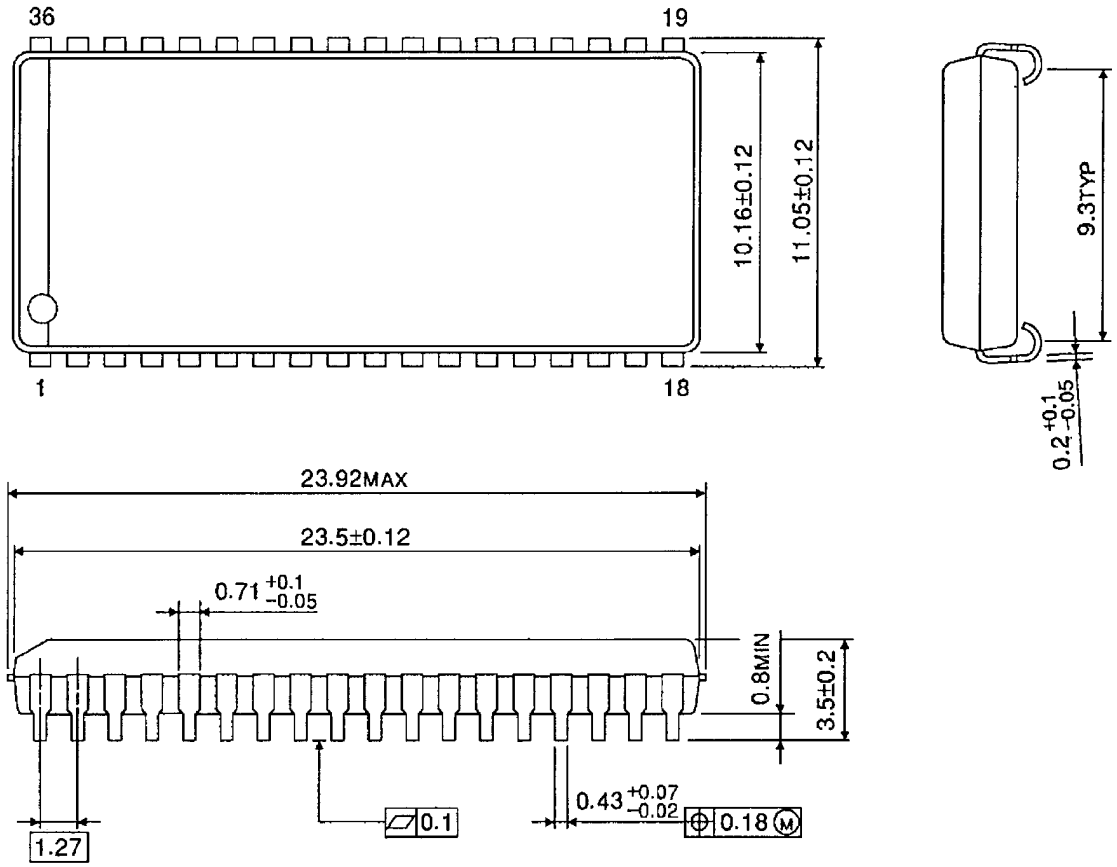
(A) t_{COE}, t_{OEE}, t_{OEW} ····· Output Enable Time

(B) t_{COD}, t_{ODO}, t_{ODW} ····· Output Disable Time



PACKAGE DIMENSIONS

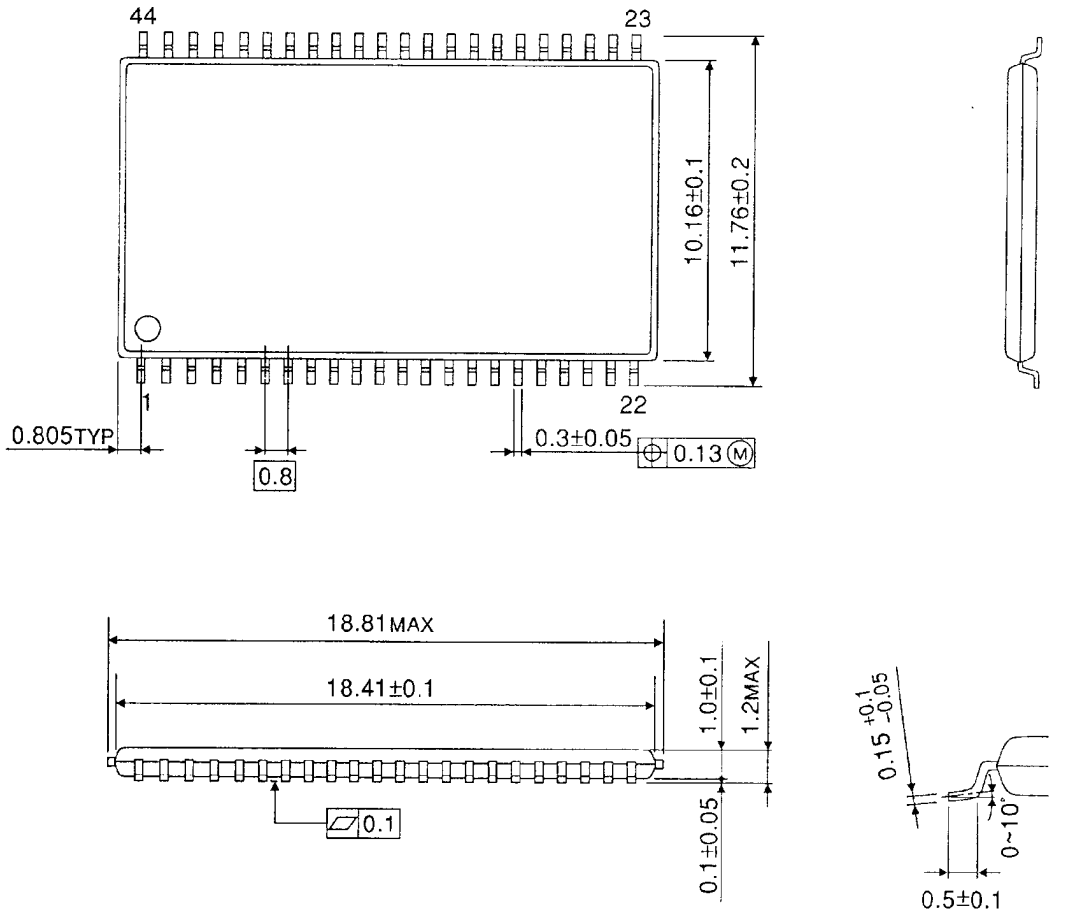
SOJ36-P-400-1.27 Unit : mm



Weight: 1.35 g (typ)

PACKAGE DIMENSIONS

TSOP II 44-P-400-0.80 Unit : mm



Weight: 0.45 g (typ)

RESTRICTIONS ON PRODUCT USE

000707EBA

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the “Handling Guide for Semiconductor Devices,” or “TOSHIBA Semiconductor Reliability Handbook” etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury (“Unintended Usage”). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer’s own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.