Ordering number :EN5848

P-Channel Silicon MOS FET

FW114

S/W Load Applications

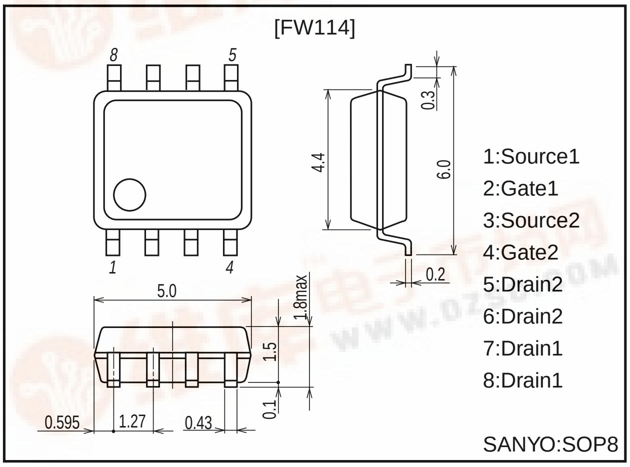
Features

- Low ON resistance.
- 2.5V drive.

Package Dimensions

unit:mm

2129



Specifications

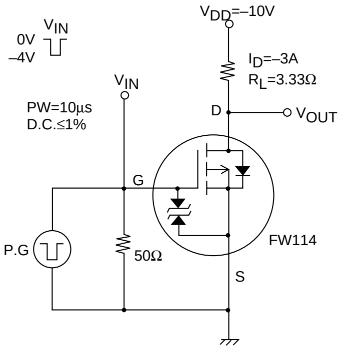
Absolute Maximum Ratings at Ta = 25˚C

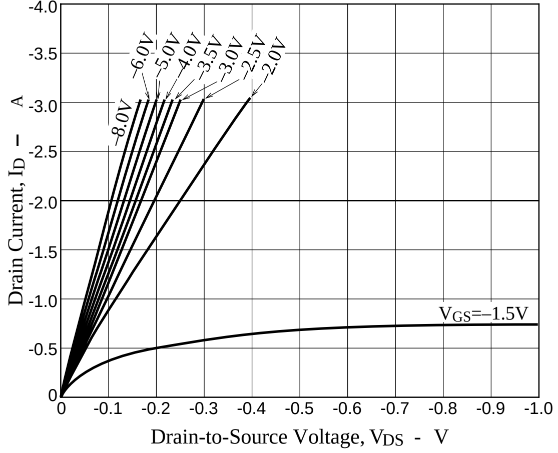
Parameter	Symbol	Conditions	Ratings	Unit
Drain-to-Source Voltage	V_{DSS}		–20	V
Gate-to-Source Voltage	V_{GSS}		±10	V
Drain Current (DC)	I_D		–3	A
Drain Current (pulse)	I_{DP}	PW≤10µs, duty cycle≤1%	–32	A
Allowable Power Dissipation	P_D	Mounted on ceramic board (1000mm^2×0.8mm) 1unit	1.7	W
Total Dissipation	P_T	Mounted on ceramic board (1000mm^2×0.8mm)	2.0	W
Channel Temperature	Tch		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C

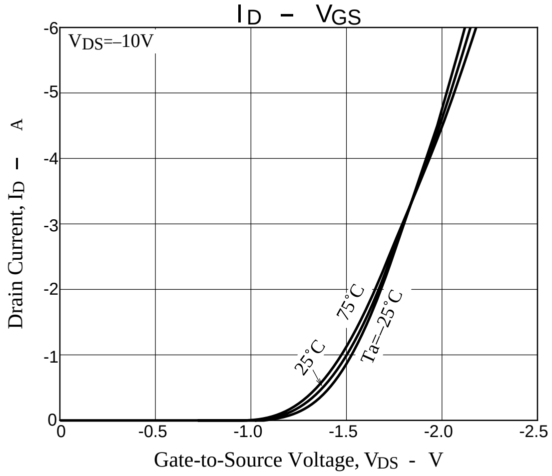
Electrical Characteristics at Ta = 25˚C

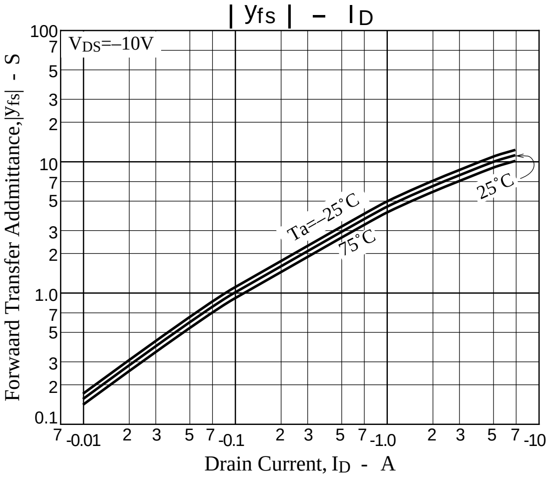
Parameter	Symbol	Conditions	Ratings min	Ratings typ	Ratings max	Unit
D-S Breakdown Voltage	$V_{(BR)DSS}$	I_D=–1mA, V_{GS}=0	–20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=–20V, V_{GS}=0			–100	µA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±8V, V_{DS}=0			±10	µA
Cutoff Current	$V_{GS(off)}$	V_{DS}=–10V, I_D=–1mA	–0.4		–1.4	V
Forward Transfer Admittance	| yfs |	V_{DS}=–10V, I_D=–3A	5	8		S
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}1$	I_D=–3A, V_{GS}=–4V		70	90	mΩ
	$R_{DS(on)}2$	I_D=–1A, V_{GS}=–2.5V		92	130	mΩ
Input Capacitance	Ciss	V_{DS}=–10V, f=1MHz		600		pF
Output Capacitance	Coss	V_{DS}=–10V, f=1MHz		300		pF
Reverse Transfer Capacitance	Crss	V_{DS}=–10V, f=1MHz		150		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit		15		ns
Rise Time	t_r	See specified Test Circuit		140		ns
Turn-OFF Delay Time	$t_{d(off)}$	See specified Test Circuit		80		ns
Fall Time	t_f	See specified Test Circuit		85		ns
Total Gate Charge	Qg	V_{DS}=–10V, V_{GS}=–10V, I_D=–3A		24		nC
Gate-to-Source Charge	Qgs	V_{DS}=–10V, V_{GS}=–10V, I_D=–3A		3		nC
Gate-to-Drain ("Miller") Charge	Qgd	V_{DS}=–10V, V_{GS}=–10V, I_D=–3A		6		nC
Diode Forward Voltage	V_{SD}	I_S=–3A, V_{GS}=0		–1.0	–1.5	V

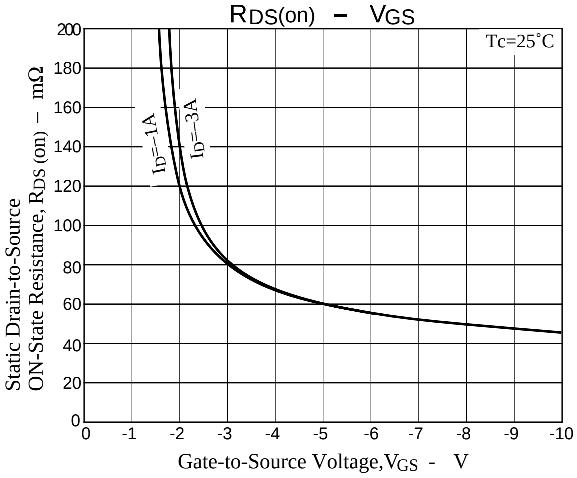
Switching Time Test Circuit

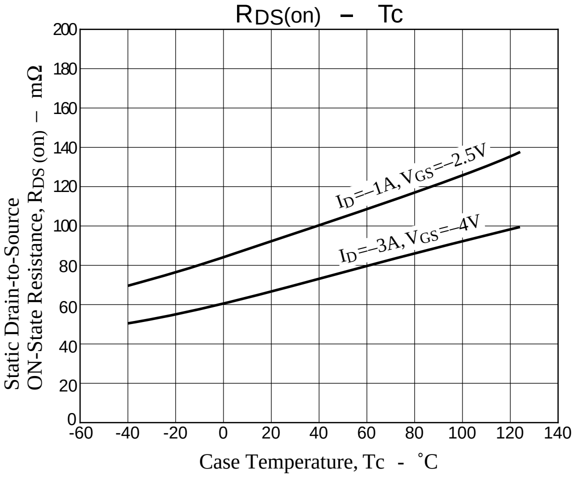


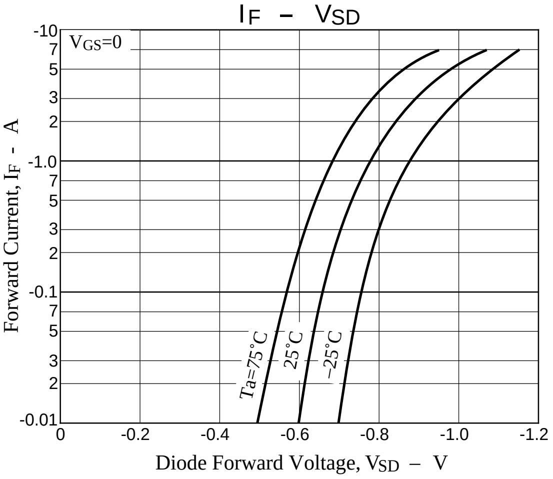

I_D – V_{DS}


I_D – V_{GS}

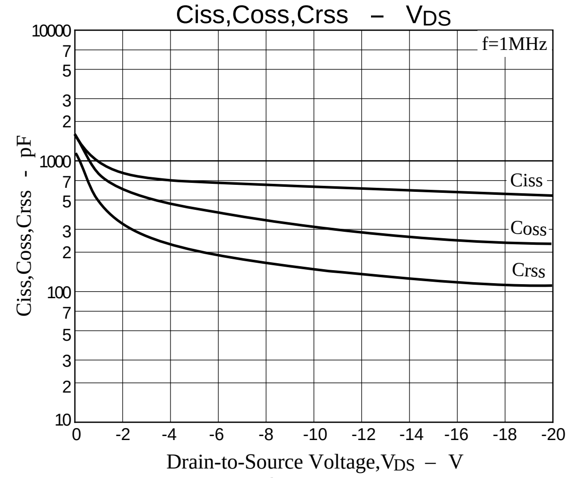

| y_{fs} | – I_D


R_{DS}(on) – V_{GS}

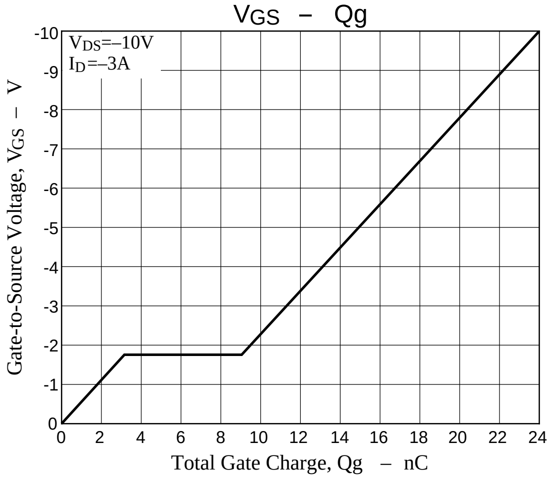

R_{DS}(on) – Tc


I_F – V_{SD}

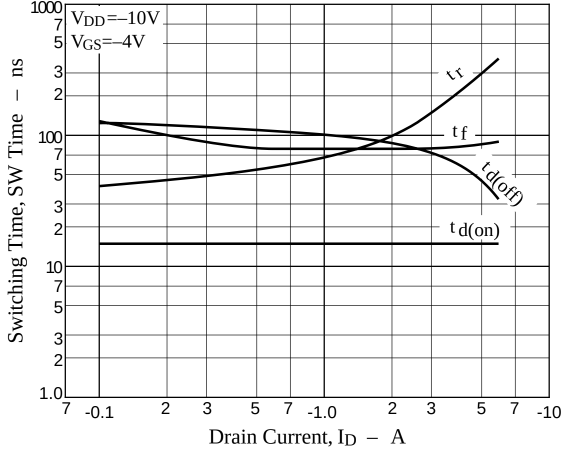
Ciss,Coss,Crss – VDS



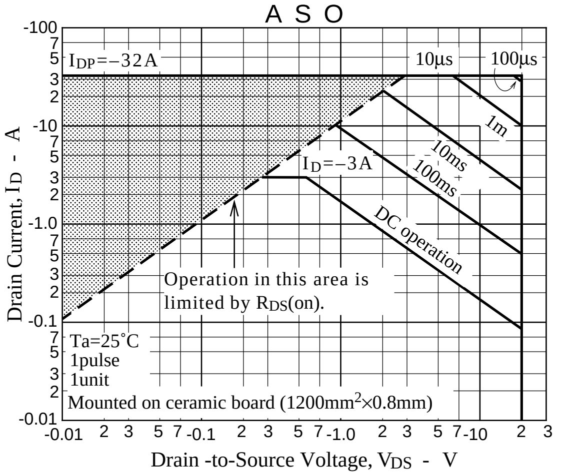
VGS – Qg



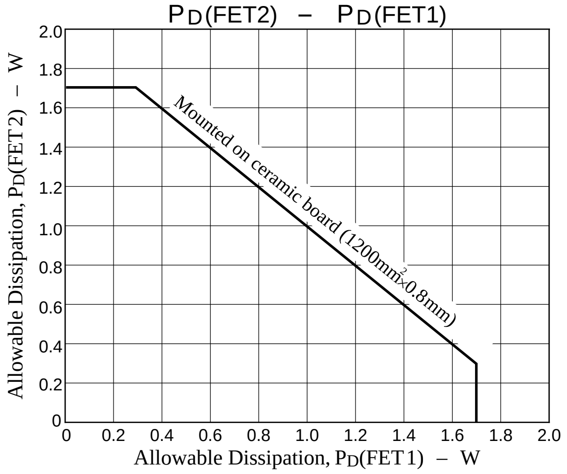
SW Time – ID



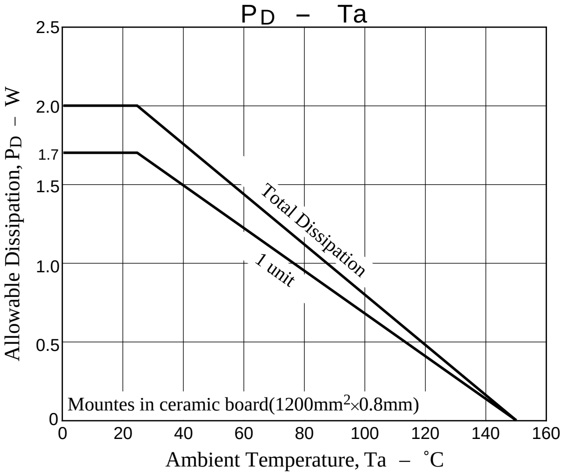
A S O



PD(FET2) – PD(FET1)



PD – Ta



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