



# CML Semiconductor Products

PRODUCT INFORMATION

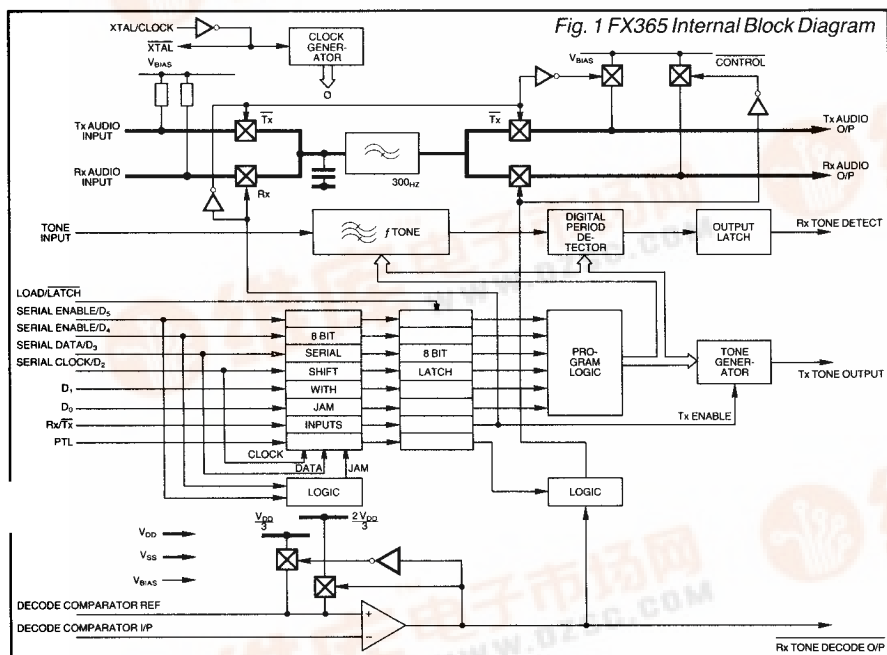
## FX365

$\mu$ P Compatible CTCSS Encoder/Decoder

Publication D/365/5 October 1991  
Provisional Issue

### Features/Applications

- CTCSS Encoder/Decoder
- Serial/Parallel  $\mu$ P Interface
- 38 Programmable Tones
- Separate Rx/Tx Audio Paths
- HP Filter for Rejection of CTCSS Tone and Prefiltering of Tx Audio
- Low Falsing with Noise Inputs
- Tx Phase Reversal Facility
- 'No Tone' Facility
- HF Filters on Inputs
- On-Chip Analogue Switching
- Low Power 5V CMOS
- Xtal Controlled Tones
- Meets EIA RS220(B)/MPT1306
- Choice of DIL or Surface Mount Package Styles



## FX365

### Brief Description

The FX365 is a CMOS LSI device intended for use as a CTCSS Encoder/Decoder in radio communications systems. Designed specifically for microprocessor controlled multichannel equipment, the FX365 incorporates a number of advanced features which improve performance and facilitate system design. The tone frequency to be encoded or decoded, the transmit enable command and the monitor receiver audio command may all be entered via an 8-bit port and a load/latch pulse. Alternatively, the programming

The tone encoder has a phase reversal facility, the tone decoder and speech path high pass filter have separate inputs and both are protected against the effects of incident RF voltages. The speech path filter has low passband ripple, low output noise and a cut-off frequency of 300Hz regardless of the programmed CTCSS tone. Separate Rx and Tx audio paths are provided for prefiltering of Tx audio and rejection of the CTCSS tone in Rx mode. The FX365 uses a 1MHz crystal reference

## Pin Number

## Function

DIL FX365J	Quad Plastic FX365LG	PLCC FX365LS
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13

**V<sub>DD</sub>**: Positive Supply.

**Xtal/Clock I/P**: Input to on-chip inverter used with a 1MHz Xtal or external clock source.

**Xtal**: Output of on-chip inverter (clock output).

**Load/Latch**: Controls 8 on-chip latches and is used to latch Rx/Tx, PTL, D<sub>0</sub>–D<sub>5</sub>. This pin is internally pulled to V<sub>DD</sub>. A logic '1' applied to this input puts the 8 latches in 'transparent' mode. A logic '0' applied to this input puts the 8 latches in the 'latched' mode. In parallel mode data is loaded and latched by a logic 1→0 transition (see Fig. 4). In serial mode data is loaded and latched by a 0→1→0 strobe pulse on this pin (see Fig. 5).

**D<sub>5</sub>/Serial Enable 1**: Data input D<sub>5</sub> (in parallel mode). A logic '1' applied to this input together with a logic '0' applied to D<sub>4</sub>/SERIAL ENABLE 2 will put the device in 'Serial mode' (see Fig. 5). This pin internally pulled to V<sub>DD</sub>.

**D<sub>4</sub>/Serial Enable 2**: Data input D<sub>4</sub> (in parallel mode). A logic '0' applied to this input together with a logic '1' on pin 5 will place the device in 'serial mode' (see Fig. 5). This pin internally pulled to V<sub>DD</sub>.

**D<sub>3</sub>/Serial Data**: Data input D<sub>3</sub> (in parallel mode). In serial mode this pin becomes the serial data input for D<sub>5</sub>–D<sub>0</sub>, Rx/Tx, PTL (see Fig. 5). D<sub>5</sub> is clocked first and PTL last. This pin internally pulled to V<sub>DD</sub>.

**D<sub>2</sub>/Serial Clock**: Data D<sub>2</sub> (in parallel mode). In serial mode this pin becomes the serial clock input. Data is clocked on the positive going edge (see Fig. 5). This pin is internally pulled to V<sub>DD</sub>.

**D<sub>1</sub>**: Data D<sub>1</sub> (in parallel mode). This pin internally pulled to V<sub>DD</sub>.

**D<sub>0</sub>**: Data D<sub>0</sub> (in parallel mode). This pin internally pulled to V<sub>DD</sub>.

**V<sub>SS</sub>**: Negative supply.

**Decode Comparator Ref (I/P)**: This pin is internally biased to V<sub>DD</sub>/3 or 2V<sub>DD</sub>/3 via 1MΩ resistors depending on the logical state of the TONE DECODE O/P pin. TONE DEC O/P = 1 will bias this input to 2V<sub>DD</sub>/3, a logic '0' will bias this input to V<sub>DD</sub>/3. This input provides the decode comparator reference voltage, and switching of bias voltages provides hysteresis to reduce 'chatter' under marginal conditions.

**Rx Tone Decoder (O/P)**: Gated output of the decode comparator. This output is used to gate the Rx Audio path. A logic '0' on this pin indicates a successful decode and indicates that the 'decode comparator input' pin is more positive than the 'decode comparator ref' input (see Table 2).

## Pin Number

## Function

DIL FX365J	Quad Plastic FX365LG	PLCC FX365LS	
14	14	14	<b>Decode Comparator Input:</b> This is the inverting input of the decode comparator. This pin is to be connected to the Rx TONE DETECT pin via an external integrator (see Figs. 2 & 3).
15	15	15	<b>Rx Tone Detect (O/P):</b> In Rx mode this pin will go to logic '1' during a successful decode (see Table 2). This pin is normally connected to the Decode Comparator input via the external integrator circuitry, as shown in Figs. 2 & 3.
16	16	16	<b>Tx Tone O/P:</b> A low impedance emitter follower stage for sourcing the CTCSS sinewave under the control of the Rx/Tx pin. This O/P when not transmitting a tone may be biased to $\frac{V_{DD}}{2} - 0.7V$ or O/C (see Table 2).
17	17	17	<b>Rx/Tx:</b> This input (in parallel mode) selects Rx or Tx modes (see Fig. 2). In serial mode this function is serially loaded. This pin is internally pulled to $V_{DD}$ via a $1M\Omega$ resistor.
18	18	18	<b>PTL:</b> In parallel Rx mode this pin operates as a 'press to listen' function by enabling the Rx audio path thus overriding the tone squelch function. In parallel Tx mode this pin reverses the phase of the transmitted CTCSS tone (squelch tail elimination). In serial mode this function is serially loaded (see Fig. 3). The phase reversal function should be applied by timing circuit to ensure correct system operation.
19	19	19	<b>Rx Audio Out:</b> This is the high pass filtered "Receive" audio output pin. This pin outputs audio when Rx TONE DECODE=0, or PTL=1 or NOTONE is programmed (see Table 2). In Tx mode this pin is biased to $\frac{V_{DD}}{2}$ .
20	20	20	<b>Tx Audio Out:</b> This is the high pass filtered "Transmit" audio output pin. In Tx mode this pin outputs audio present at the 'Tx AUDIO INPUT' pin. In Rx mode this pin is biased to $\frac{V_{DD}}{2}$ .
21	21	21	<b>Bias:</b> This pin is the output of an internally generated $\frac{V_{DD}}{2}$ bias level and would normally be externally decoupled to $V_{SS}$ via $C_6$ .
22	22	22	<b>Tx Audio I/P:</b> This is the Tx Audio input pin. In Tx mode audio may be prefiltered, using the Tx audio path, thus helping to avoid talkoff due to intermodulation of speech frequencies with the transmitted CTCSS tone. The Tx audio path may also be used to prefilter speech when using scramblers which introduce noise in the low frequency band. This pin is internally biased to $\frac{V_{DD}}{2}$ .
23	23	23	<b>Rx Audio Input:</b> This is the input to the audio high pass filter in Rx mode. This pin is internally biased to $\frac{V_{DD}}{2}$ .
24	24	24	<b>Tone Input:</b> This is the input to the CTCSS tone detector and is internally biased to $\frac{V_{DD}}{2}$ .

External Component Connections

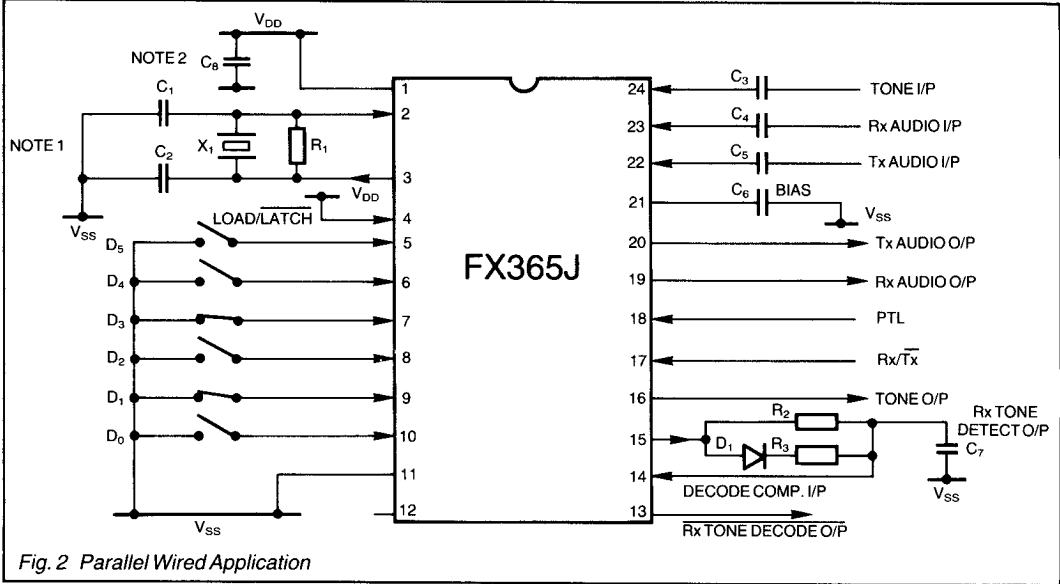


Fig. 2 Parallel Wired Application

Component	Unit Value	Note
R <sub>1</sub>	1M	1
R <sub>2</sub>	820k	
R <sub>3</sub>	330k	
C <sub>1</sub>	68p	1
C <sub>2</sub>	33p	1
C <sub>3</sub>	0.1μ	
C <sub>4</sub>	0.1μ	

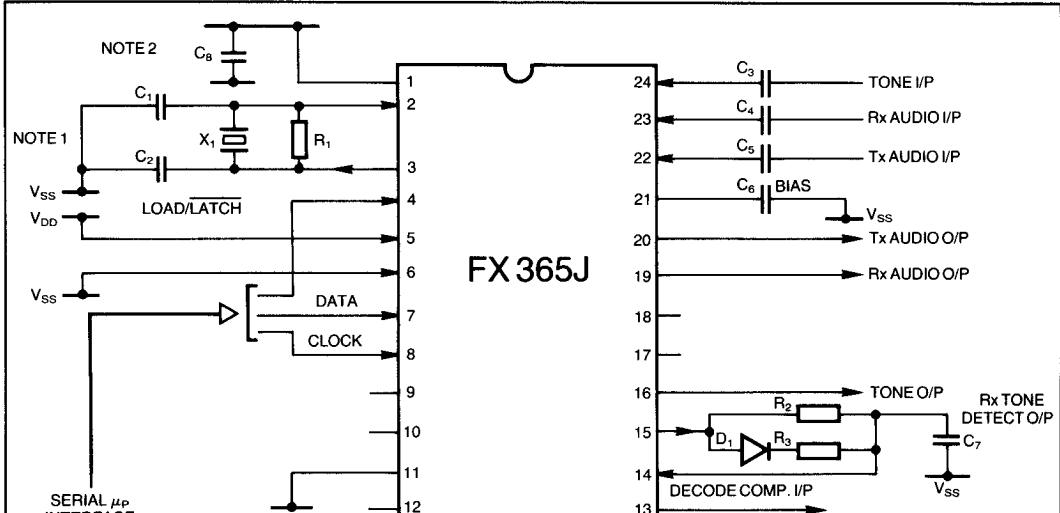
Component	Unit Value	Note
C <sub>5</sub>	0.1μ	
C <sub>6</sub>	1.0μ	
C <sub>7</sub>	0.1μ	
C <sub>8</sub>	1.0μ	2
D <sub>1</sub>	small signal	
X <sub>1</sub>	1MHz	1

NOTES:

Tolerances: Resistors ±10%. Capacitors ±20%  
1. Xtal circuitry shown is in accordance with CML.  
Application Note D/XT/1 April 1986.

2. C<sub>8</sub> is used for power supply decoupling.  
Depending on application further filtering may be required.

Table 1 Component References and Values



## Truth Tables

Input Pin – Condition				Output Pin – Condition		Result/Function					Notes
D <sub>0</sub> -D <sub>5</sub>	Rx/Tx	PTL	Decode Comp Input	Rx Tone Detect	Tone Decode	Tone Transmitter Enabled	Tx Tone Phase Reversed	Tx Audio Path Enabled	Tone Decoder Enabled	Rx Audio Path Enabled	
Tone	0	0	x	0	1	Yes	No	Yes	No	No (bias)	1a
Tone	0	1	x	0	1	Yes	Yes	Yes	No	No (bias)	1b
No tone	0	x	x	0	1	No (bias)	x	Yes	No	No (bias)	2
Tone	1	0	0	0	1	No (o/c)	x	No	Yes	No (bias)	3a
Tone	1	1	0	0	1	No (o/c)	x	No	Yes	Yes	3b
Tone	1	x	1	1	0	No (o/c)	x	No	Yes	Yes	4
No tone	1	x	x	x	0	No (o/c)	x	No	Yes	Yes	5

### Notes:

1a. Normal tone transmit condition.

1b. Tone transmit with phase reversed.

2. 'NOTONE' programmed in Tx mode, tone transmit O/P set to  $V_{DD}/2 - 0.7V$ . Tx audio path enabled.

3a. Normal decode standby.

3b. Normal decode standby with PTL used to enable audio.

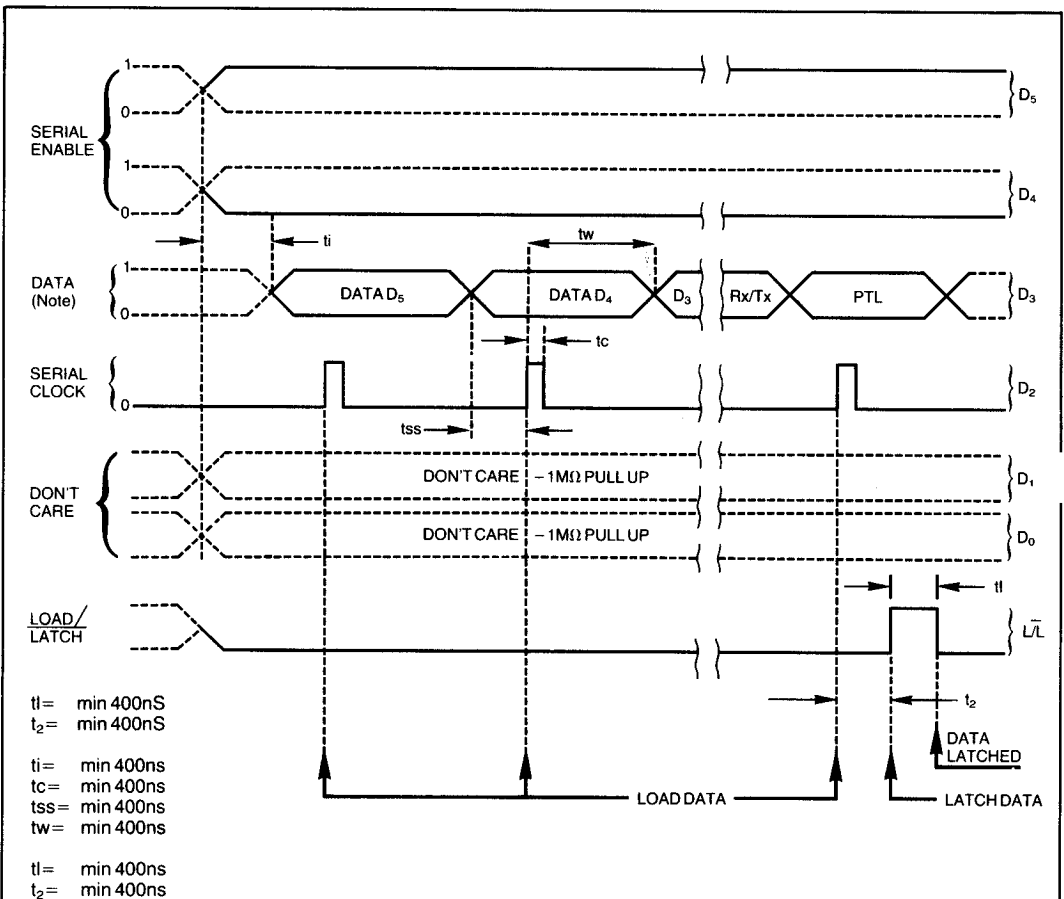
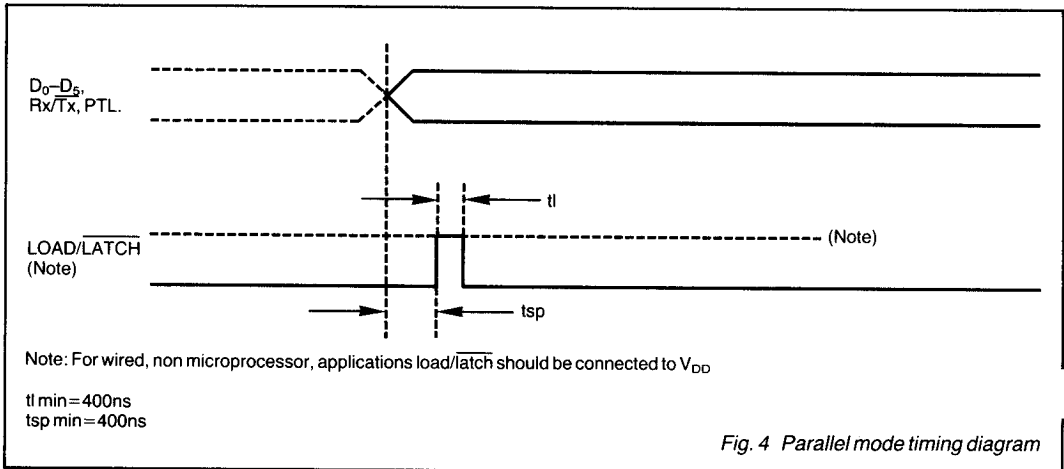
4. Normal 'decode of correct CTCSS tone' condition, PTL has no effect.

5. 'NOTONE' programmed in Rx mode, tone transmit O/P (o/c), Rx audio path enabled.

**Table 2 Truth table defining combinations of input/output conditions.**

Nominal Freq. Hz		FX365 Frequency		Programme Inputs						
		$\Delta f_o\%$	D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>		
67.0	67.05	+0.07	1	1	1	1	1	1		
71.9	71.90	0.0	1	1	1	1	1	0		
74.4	74.35	-0.07	0	1	1	1	1	1		
77.0	76.96	-0.05	1	1	1	1	0	0		
79.7	79.77	+0.09	1	0	1	1	1	1		
82.5	82.59	+0.10	0	1	1	1	1	0		
85.4	85.38	-0.02	0	0	1	1	1	1		
88.5	88.61	+0.13	0	1	1	1	0	0		
91.5	91.58	+0.09	1	1	0	1	1	1		
94.8	94.76	-0.04	1	0	1	1	1	0		
97.4	97.29	-0.11	0	1	0	1	1	1		
100.0	99.96	-0.04	1	0	1	1	0	0		
103.5	103.43	-0.07	0	0	1	1	1	0		
107.2	107.15	-0.05	0	0	1	1	0	0		
110.9	110.77	-0.12	1	1	0	1	1	0		
114.8	114.64	-0.14	1	1	0	1	0	0		
118.8	118.80	0.0	0	1	0	1	1	0		
123.0	122.80	-0.17	0	1	0	1	0	0		
127.3	127.08	-0.17	1	0	0	1	1	0		
131.8	131.67	-0.10	1	0	0	1	0	0		
136.5	136.61	+0.08	0	0	0	1	1	0		
141.3	141.32	+0.02	0	0	0	1	0	0		
146.2	146.37	+0.12	1	1	1	0	1	0		
151.4	151.09	-0.20	1	1	1	0	0	0		
156.7	156.88	+0.11	0	1	1	0	1	0		
162.2	162.31	+0.07	0	1	1	0	0	0		
167.9	168.14	+0.14	1	0	1	0	1	0		
173.8	173.48	-0.19	1	0	1	0	0	0		
179.9	180.15	+0.14	0	0	1	0	1	0		
186.2	186.29	+0.05	0	0	1	0	0	0		
192.8	192.86	+0.03	1	1	0	0	1	0		
203.5	203.65	+0.07	1	1	0	0	0	0		
210.7	210.17	-0.25	0	1	0	0	1	0		
218.1	218.58	+0.22	0	1	0	0	0	0		
225.7	226.12	+0.18	1	0	0	0	1	0		
233.6	234.19	+0.25	1	0	0	0	0	0		
241.8	241.08	-0.30	0	0	0	0	1	0		
250.3	250.28	-0.01	0	0	0	0	0	0		
Notone	Notone	—	0	0	0	0	1	1		
Serial Input Mode			x	x	Clock	Data	0	1		

## Parallel and Serial Mode Timing Diagrams



Note 1: Serial bit 1 through bit 8 =  $D_7$ ,  $D_6$ ,  $D_5$ ,  $D_4$ ,  $D_3$ ,  $D_2$ ,  $D_1$ ,  $D_0$ , Rx/Tx and PTL respectively

## Specification

### Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage	–0.3V to 7.0V
Input voltage at any pin (ref $V_{SS}=0V$ )	–0.3V to ( $V_{DD}+0.3V$ )
Output sink/source current (total)	20mA
Operating temperature range:	FX365J –30°C to +85°C
	FX365LG/LS –30°C to +70°C
Storage temperature range:	FX365J –55°C to +125°C
	FX365LG/LS –40°C to +85°C
Maximum device dissipation	800mW
Derating	10mW/°C

### Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$V_{DD} = 5.0V$ ,  $T_{AMB} = 25^{\circ}C$ , 0dB ref: = 300mVrms. Composite Signal = 0dB 1kHz Tone, –12dB Noise (band-limited 6kHz gaussian white noise), –20dB  $f_o$  CTCSS Tone.

Characteristics	See Note	Min.	Typ.	Max.	Unit
<b>Static Characteristics</b>					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
(Tx)		–	3.5	–	mA
(Rx)		–	3.5	–	mA
Tone Input Impedance		–	1.0	–	MΩ
Audio Input Impedance		–	1.0	–	MΩ
Audio Output Impedance		–	1.0	–	kΩ
Digital Input Impedance	1	–	1.0	–	MΩ
Input Logic "1"	1	3.5	–	–	V
Input Logic "0"	1	–	–	1.5	V
Logic "1" Output 1' source = 0.1mA	2	4.0	–	–	V
Logic "0" Output 1' sink = 0.1 mA	2	–	–	1.0	V
<b>Dynamic Characteristics</b>					
<b>Decoder</b>					
Decode Input Signal Level	3	–20	–	–	dB
Decode Response Time	3, 6	–	–	250	ms
De-Response Time	3, 6	–	–	250	ms
Decode Selectivity	3	±0.5	–	±3.0	% $f_o$
<b>Encoder</b>					
Tone Output Level (relative 775mVrms)		–3.0	0	–	dB
Tone Frequency Accuracy ( $f_o$ error)		–0.3	–	+0.3	% $f_o$
<b>Risetime to 90% (nominal output)</b>					
$f_o > 100Hz$	4	–	55.0	–	ms
$f_o < 100Hz$	4	–	70.0	–	ms
Tone Output Load Current		–	–	5.0	mA
Total Harmonic Distortion		–	2.0	5.0	%
Output Level Variation Between Tones		–	0.1	–	dB
<b>Audio Filter</b>					
Total Harmonic Distortion	5	–	2.0	5.0	%
<b>Output Noise Level</b>					
<b>Input a.c. Short Cct, Audio Switch Enabled</b>					
Cut-Off frequency		–	300	–	Hz
Bandpass Ripple (300Hz –3000Hz)	5	–1.0	–	+1.0	dB
Stopband Attenuation <250Hz	5	36.0	40.0	–	dB
Passband Gain (ref. 1kHz)		–	0	–	dB
<b>Audio Switch</b>					
Isolation	5	–	60.0	–	dB
<b>Serial/Parallel Inputs</b>					
Parallel Set-Up Time ( $t_{sp}$ )	7	400	–	–	ns
Load/Latch Pulse Width ( $t_L$ )	7	400	–	–	ns
Serial Clock Pulse Width ( $t_{c}$ )	7	400	–	–	ns
Serial Set-Up Time ( $t_{ss}$ )	7	400	–	–	ns
Serial Clock Frequency	7	–	1.0	–	MHz

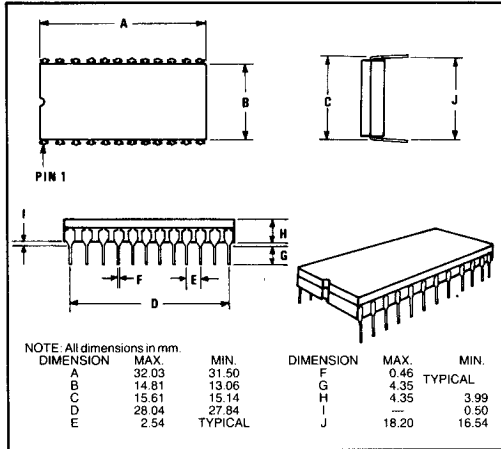
### Notes

- Refers to Rx/Tx, PTL, Decode Comparator Input,  $D_0$ ,  $D_1$ ,  $D_2$ ,  $D_3$ ,  $D_4$ ,  $D_5$ .
- All logic outputs.
- Composite Signal Test Condition.
- Any programme tone and RL = 600Ω. CL = 15pF. Includes response to a phase reversal instruction.
- 1kHz reference = 0dB.
- $f_o > 100Hz$ . (for 100Hz >  $f_o$  > 67Hz:  $t = (100/f_o \text{ Hz}) \times 250\text{ms}$ ).

## Packaging Outlines

The FX365J, the cerdip package, is illustrated in figure 6. The 'LG' version is shown in figure 7, and the 'LS' version in figure 8. To allow complete identification, the FX365 LG and 'LS' packages have an indent spot adjacent to pin 1 and a chamfered corner between pins 3 and 4. Pins number anti-clockwise when viewed from the top (indent side).

Fig. 6 FX365J Cerdip DIL Package



## Ordering Information

- FX365J** 24-pin cerdip DIL
- FX365LG** 24-pin quad plastic encapsulated, bent and cropped
- FX365LS** 24-lead plastic leaded chip carrier

## Handling Precautions

The FX365J/LG/LS is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

Fig. 7 FX365LG Package

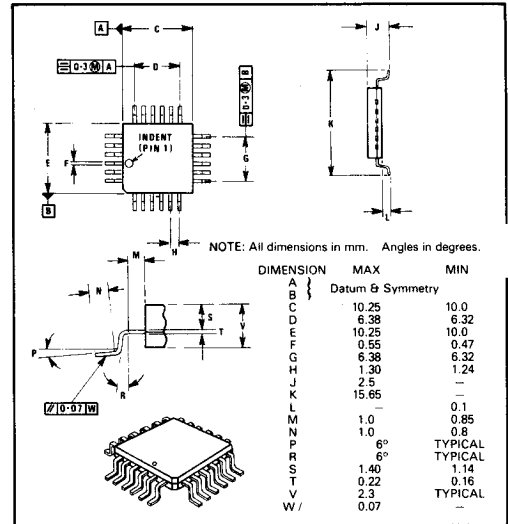
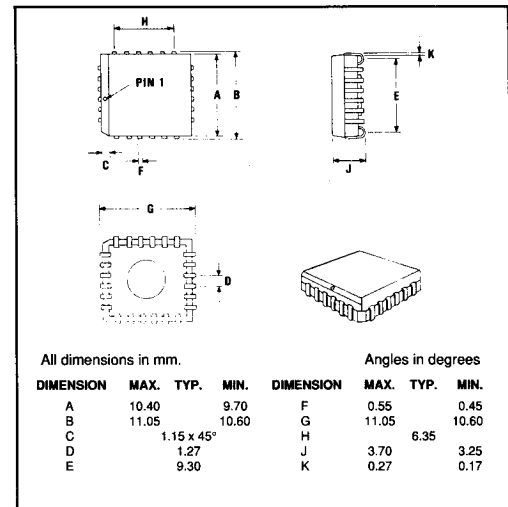


Fig. 8 FX365LS Package





In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc (*Consumer Microcircuits Limited (UK)*, *CML Microcircuits (USA)* and *CML Microcircuits (Singapore) Pte Ltd*) have undergone name changes, maintaining their separate new names (*CML Microcircuits (UK) Ltd*, *CML Microcircuits (USA) Inc* and *CML Microcircuits (Singapore) Pte Ltd*), now operate under the single name **CML Microcircuits**.

These companies are all 100% owned operating companies of the CML Microsystems Group and these changes are purely changes of name and do not change any legal entities and hence will have no effect on any agreements or contracts currently in force.

### **CML Microcircuits Product Prefix Codes**

Until the latter part of 1996, the differentiator between products manufactured by CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc. and Consumer Microcircuits Limited were denoted by the prefix codes CMX, CML and CMC respectively. These products use the same silicon etc. and today still carry the same prefix. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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