CONSUMER MICROCIRCUITS LTD

PRODUCT INFORMATION

Publication D/419/4 May 1987
Provisional Issue

Features

- 1200 Baud FFSK Modem
- Meets Cellular and Trunked Radio Specifications
- Full Duplex 1200 Baud
- On-Chip Rx and Tx Bandpass Filters
- Clock Recovery and Carrier Detect Facilities
- Single 5 Volt CMOS Process
- Surface Mount or DIL Package Styles

Applications

- Mobile and Cellular Radio Data Signalling
- NMT 450/900
- Band III
- Radiocom 2000
- ZVEI
- Personal Radio
- Portable Data Terminals
- General Purpose Applications

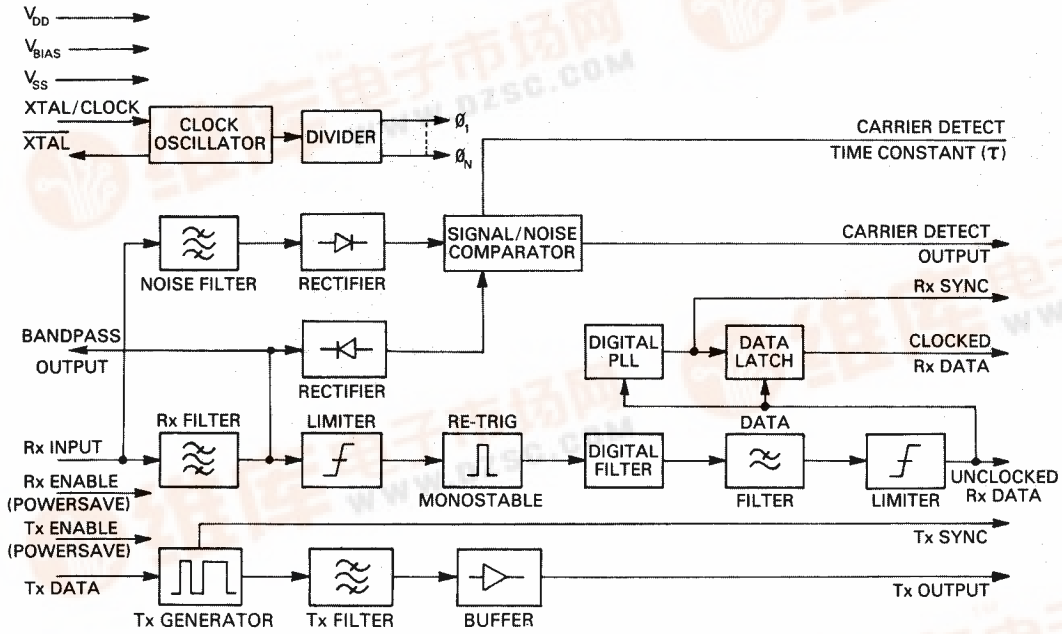


Fig. 1 Internal Block Diagram

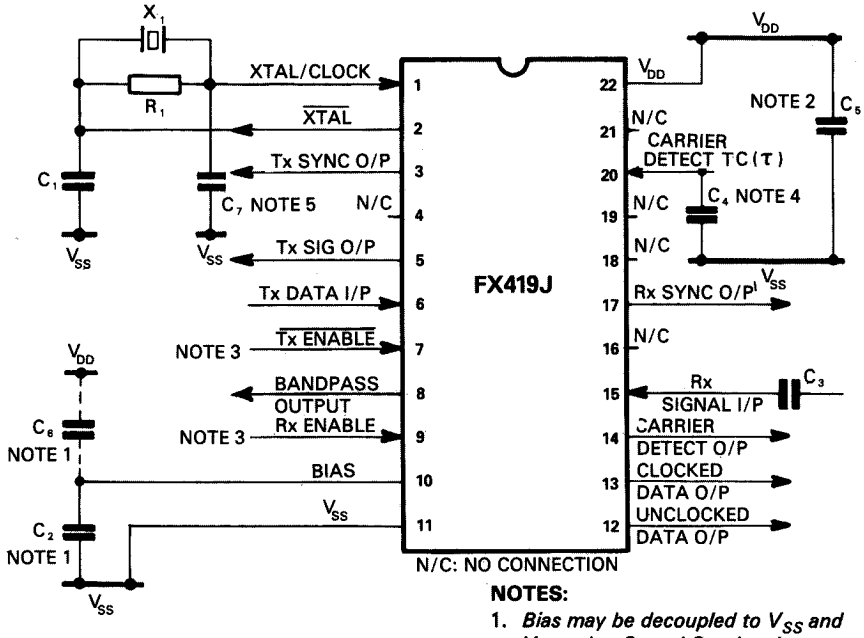
FX419

Brief Description

The FX419 is a single chip CMOS LSI circuit which operates as a 1200 baud FFSK modem. The mark and space frequencies are 1200Hz and 1800Hz phase continuous and the frequency transitions occur at the zero crossing point. The transmitter and receiver will work independently, thus providing full duplex operation at 1200 baud. The baud rate, transmit mark and space frequencies, Tx synchronization and Rx synchronization are all derived from a crystal oscillator for high stability, and an external 1.008MHz crystal is required for this purpose. The device includes circuitry for carrier detect and facility for the Rx clock recovery. An on-board switched capacitor 900Hz—2100Hz bandpass filter provides optimum carrier filtering. The use of switched capacitor analogue filters and digital signal processing results in excellent dynamic performance with few external components, the CMOS process and current saving techniques offer low standby supply current for portable battery powered applications.

Pin Number			Function
DIL FX419J	Quad Plastic FX419LG	PLCC FX419LH	
1	1	1	**Xtal/Clock:** The input to an on-chip inverter for use with a 1.008MHz xtal. Alternatively, a 1.008MHz clock may be used.
2	2	2	$\overline{\text{Xtal}}$: Output of on-chip inverter.
—	—	3	**No Connection:** Leave open circuit.
3	3	4	**Tx Sync O/P:** A 1200Hz squarewave used to synchronize the input of logic data and transmission of the FFSK signal *(See Fig. 5).*
4	4	5,6	**No Connection:** Leave open circuit.
5	5	7	**Tx Signal O/P:** With transmitter disabled, this pin is set to a high impedance state. When transmitter is enabled, this pin outputs the 1200/1800Hz (140 step pseudo-sinewave) FFSK signal *(See Fig. 5).*
—	—	8	**No Connection:** Leave open circuit.
6	7	9	**Tx Data I/P:** Serial logic data to be transmitted, is input to this pin and synchronized by the "Tx Sync O/P" *(See Fig. 5).*
7	8	10	$\overline{\text{Tx Enable}}$: A logic '1' applied to this input will put the transmitter into powersave whilst forcing "Tx Sync O/P" to logic '1' and "Tx Signal O/P" to a high impedance state. A logic '0' will enable the transmitter *(See Fig. 5).* This pin is internally pulled to V_{DD}.
8	9	11	**Bandpass O/P:** This is the output of the Rx 900-2100Hz bandpass filter. The output impedance of this pin is typically 10kΩ and may require buffering prior to use.
9	10	12	**Rx Enable:** A logic '0' applied to this input will put the receiver into powersave whilst forcing "Clocked Data O/P" and "Carrier Detect" to logic '0'. A logic '1' will enable the receiver *(See Figures 2 and 6).* "Rx Sync Out" may be logic '1' or '0' during powersave. This pin is internally pulled to V_{DD}.
10	11	13	**Bias:** Provides bias internally and should be decoupled externally to V_{SS} by a capacitor *(See Fig 2).*
11	12	14	V_{SS}: Negative supply.
12	13	15	**Unclocked Data O/P:** This pin outputs recovered asynchronous serial data from the receiver.
13	14	16	**Clocked Data O/P:** This pin outputs recovered synchronous serial data from the receiver and is internally latched out by a recovered clock appearing on the "Rx Sync O/P" pin *(See Figures 2 and 6).*
14	15	17	**Carrier Detect:** This pin will output a logic '1' when an FFSK signal is being received.
—	—	18,19	**No Connection:** Leave open circuit.
15	16	20	**Rx Signal I/P:** This is the FFSK signal input pin for the receiver and should be decoupled via a capacitor C_3.
16	17	21	**No Connection:** Leave open circuit.
17	18	22	**Rx Sync O/P:** This is a flywheel 1200Hz squarewave output which upon presentation of FFSK data signal is synchronised internally to the incoming data *(See Figures 2 and 6).*
18,19	19,20,21	23,24, 25,26	**No Connection:** Leave open circuit.
20	22	27	**Carrier Detect Time Constant (τ):** This input forms part of the carrier detect integration function. The value of C_4 connected to this pin will affect the carrier detect response time and hence noise performance *(See Fig. 2, Note 4).*
21	23	—	**No Connection:** Leave open circuit.
22	24	28	V_{DD} : Positive supply.

Note: Output Loading



NOTES:

1. *Bias may be decoupled to V_{SS} and V_{DD} using C_2 and C_6 when input signals are referenced to the bias pin. For input signals referenced to V_{SS}, decouple Bias to V_{SS} using C_2 only.*
2. *Use C_5 when input signals are referenced to V_{SS}, to decouple V_{DD}.*
3. *The value of C_4 determines the carrier detect time constant. A long time constant results in improved noise immunity but increased response time. C_4 may be varied to trade-off response time for noise immunity.*
4. *The value of C_7 reduces xtal voltage overshoot. Refer to CML Xtal Oscillator application note D/XT/1 APRIL 1986.*

Component References

Component	Unit Value	Tolerance %
R_1	1M	±10
C_1	33p	
C_2	1μ	±20
C_3	0.1μ	
C_4	0.1μ	±10
C_5	1μ	±20
C_6	1μ	
X_1	1.008 MHz	Customer Selectable
C_7	33p	

Fig. 2 External Component Connections

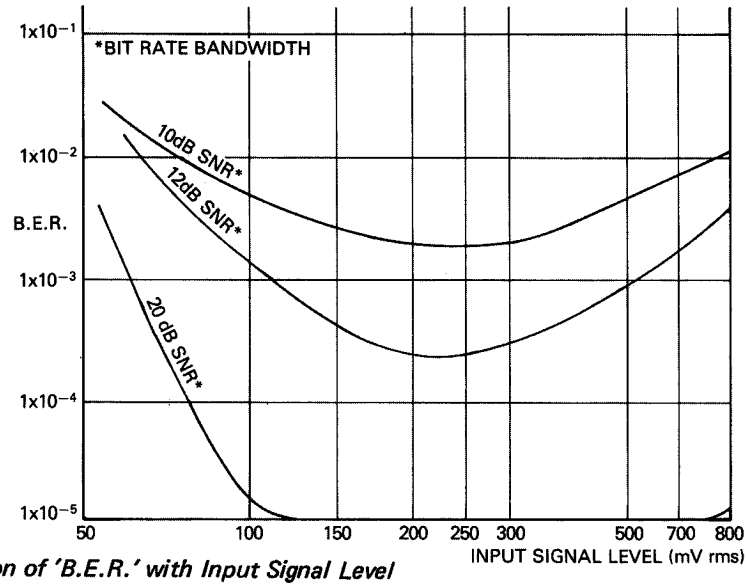
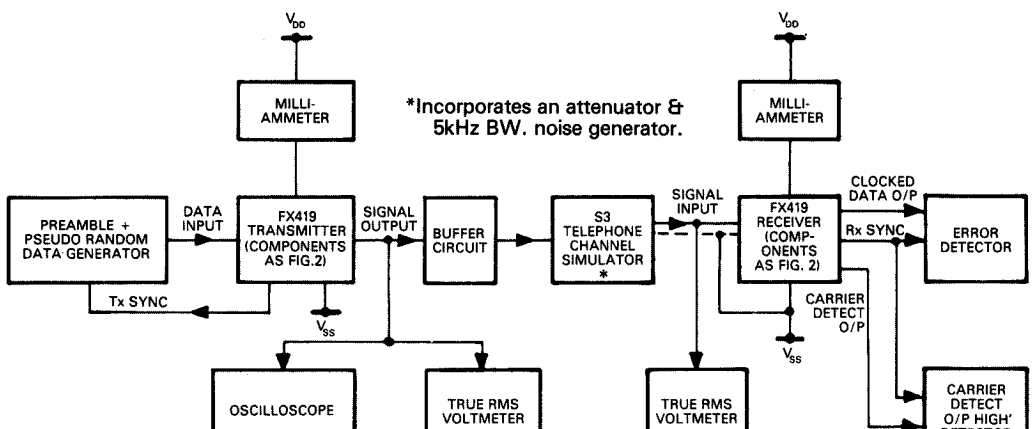


Fig. 3 Typical Variation of 'B.E.R.' with Input Signal Level



Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		−0.3V to 7.0V
Input voltage at any pin (ref V_{SS} = OV)		−0.3V to (V_{DD} + 0.3V)
Output sink/source current (total)		20mA
Operating temperature range:	FX419J	−30°C to + 85°C
	FX419LG/LH	−30°C to + 70°C
Storage temperature range:	FX419J	−55°C to +125°C
	FX419LGLH	−40°C to + 85°C
Maximum device dissipation:		All versions 100mW

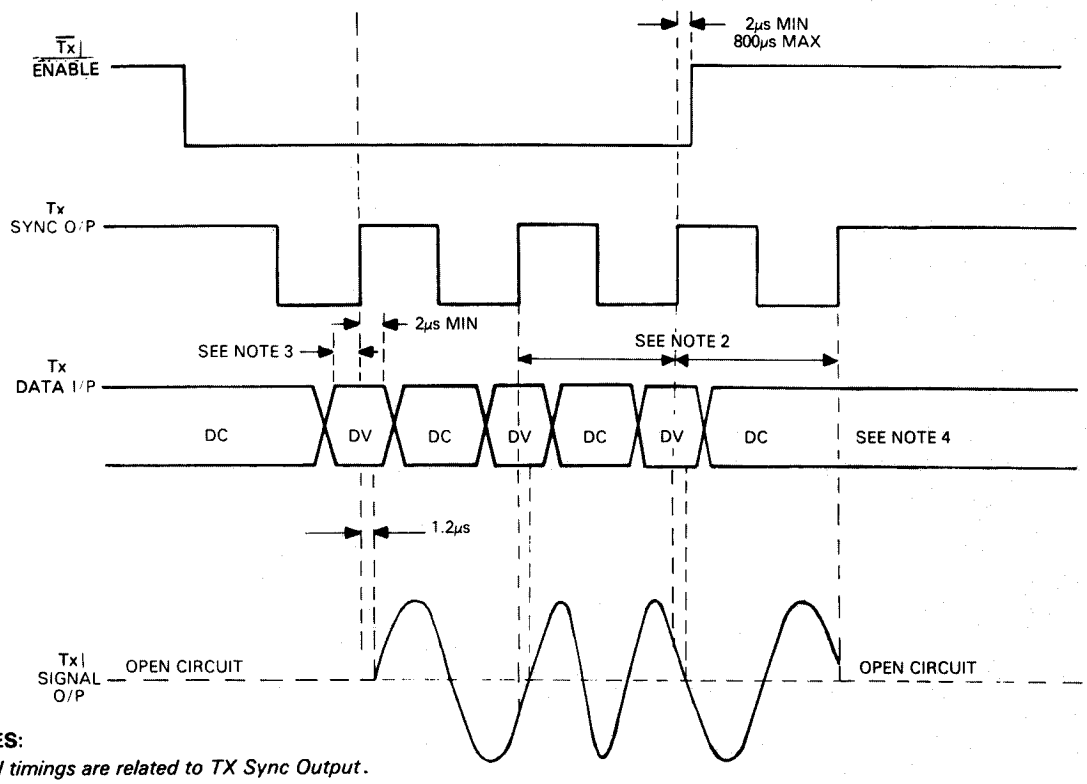
Operating Limits

V_{DD} = +5V, T_{amb} = 25°C, Ø = 1.008MHz (Xtal), $\Delta f\emptyset$ = 0
All characteristics measured using the standard test circuit (figure 4) with the following test parameters and is valid for all tests unless otherwise stated:

0dB reference	300mV rms
Noise	(band limited 5kHz gaussian white noise)
SNR ratio measured in bit rate bandwidth (1200Hz)	

Characteristics	See Note	Min	Typ	Max	Unit
Static Characteristics					
Supply volts		4.5	5.0	5.5	V
Supply current: Rx (Enabled) Tx (Disabled)		—	3.6	—	mA
Rx (Enabled) Tx (Enabled)		—	4.5	—	mA
Rx (Disabled) Tx (Disabled)		—	650	—	µA
Logic '1' level		80%V_{DD}	—	—	V
Logic '0' level		—	—	20%V_{DD}	V
Digital O/P Impedance		—	4	—	kΩ
Analogue and Digital input impedance		100	—	—	kΩ
Tx O/P impedance		—	10	—	kΩ
On-chip crystal oscillator:					
R_{in}		10	—	—	MΩ
R_{out}		5	—	15	kΩ
Inverter gain		10	—	20	dB
Gain Bandwidth Product		3×10^6	—	—	
Crystal frequency	1	—	1.008	—	MHz
Dynamic Characteristics					
Receiver:					
Signal Input: Dynamic range (50dB SNR)	2, 3	100	230	1000	mV rms
Bit Error Rate: 12dB SNR	3	—	7.0	—	10^{-4}
20dB SNR	3	—	1.0	—	10^{-8}
Receiver Synchronization 12dB SNR:	6				
Probability of bit 8 being correct			0.99		
Probability of bit 16 being correct			0.995		
Carrier Detect	6				
Probability of Carrier Detect being high:					
12dB SNR after bit 8	4		0.99	0.98	
12dB SNR after bit 16	4		0.999	0.995	
0dB noise				0.01	
Transmitter O/P					
Tx O/P level		—	775	—	mV rms
Output level variation 1200/1800Hz		0	—	±1.00	dB
O/P distortion		—	3	5	%
3rd harmonic distortion		—	2	3	%
Logic '1' carrier frequency	5	—	1200	—	Hz
Logic '0' carrier frequency	5	—	1800	—	Hz
Isochronous distortion					
1200Hz – 1800Hz		—	25	40	µs
1800Hz – 1200Hz		—	20	40	µs

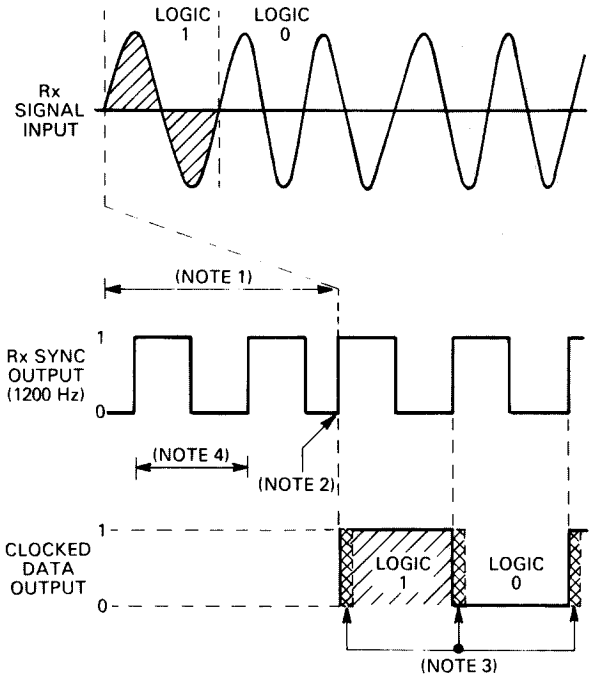
Notes: *1. Crystal tolerance depends on system requirements.*
2. See Fig. 3.
3. SNR (Bit Rate Bandwidth)

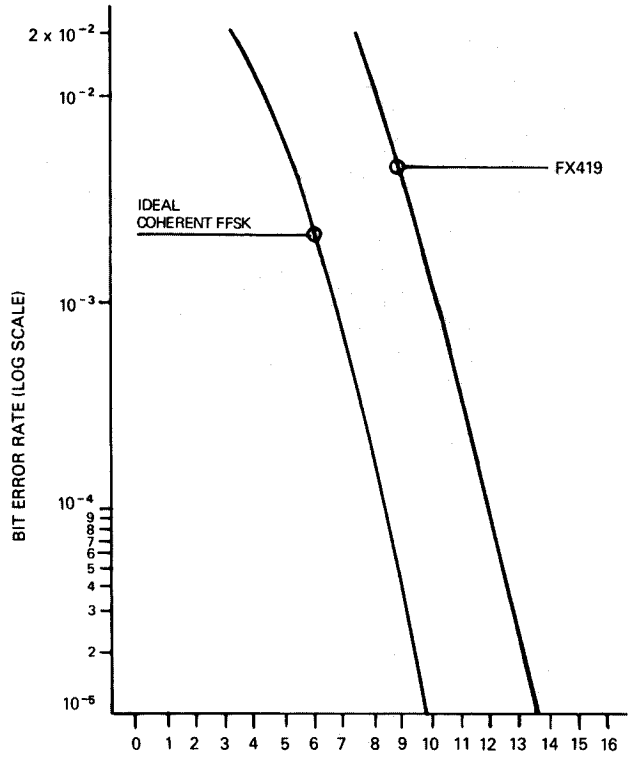


NOTES:

1. *All timings are related to TX Sync Output.*
2. *0.833ms for 1.008MHz Crystal Input.*
3. *2μs Min + Crystal tolerance.*
4. *DC = Don't Care, DV = Data Valid.*

Fig. 5 Transmitter Timing Diagram



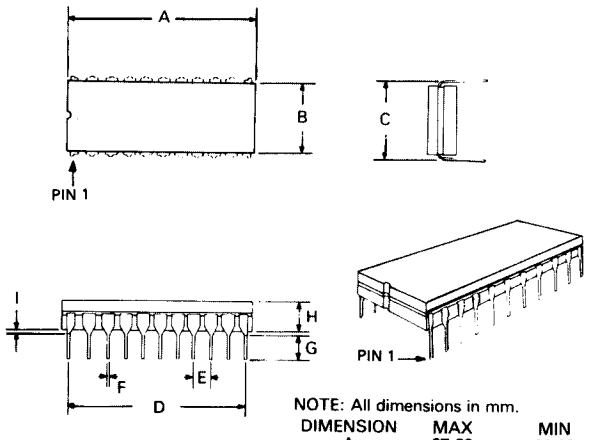


NOTES:

1. *Internal Delay-typ 1.5ms.*
2. *From freely running to Sync in 8 data bits (See spec).*
3. *Undetermined state—2μs max.*
4. *Min 800μs—Max 865μs*

Package Details

The FX419J, the cerdip package, is illustrated in *Figure 8.* The 'LG' version is shown in *Figure 9,* and the 'LH' version in *Figure 10.* Both 'LG' and 'LH' packages are supplied in conductive trays for handling convenience. To allow complete identification, the FX419LG and LH packages have an indent spot adjacent to Pin 1 and a chamfered corner between Pins 3 and 4 for LG package, between Pins 4 and 5 for LH package. Pins number anti-clockwise when viewed from the top (indent side).



NOTE: All dimensions in mm.

DIMENSION	MAX	MIN
A	27.38	26.98
B	9.75	9.55
C	10.60	10.40
D	25.50	25.30
E	2.54	TYPICAL
F	0.46	DIMENSION
G	4.30	4.10
H	4.27	3.99
I	1.4	TYPICAL

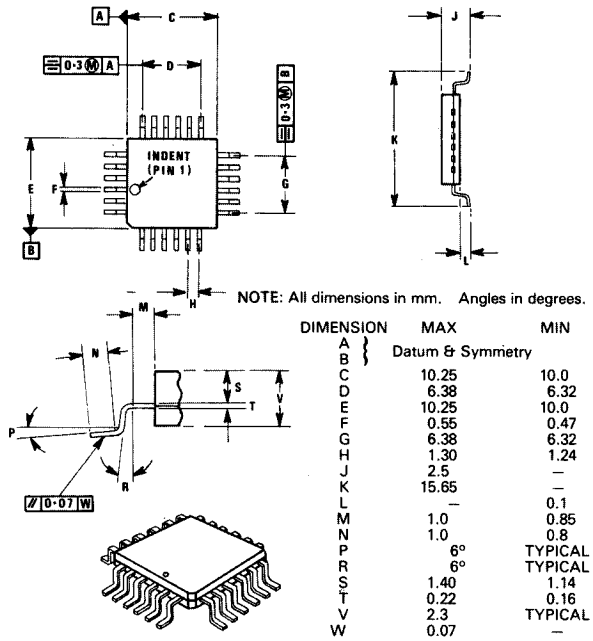
FX419J **22-pin Cerdip DIL**

FX419LG **24-pin quad plastic encapsulated, bent and cropped.**

FX419LH **28-lead Plastic leaded chip carrier.**

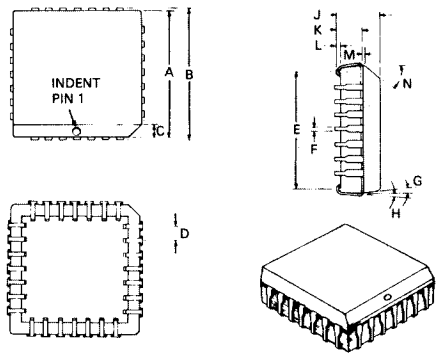
Handling Precautions

The FX419J/LG/LH is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX	MIN
A, B	Datum & Symmetry	
C	10.25	10.0
D	6.38	6.32
E	10.25	10.0
F	0.55	0.47
G	6.38	6.32
H	1.30	1.24
J	2.5	—
K	15.65	—
L	—	0.1
M	1.0	0.85
N	1.0	0.8
P	6°	TYPICAL
R	6°	TYPICAL
S	1.40	1.14
T	0.22	0.16
V	2.3	TYPICAL
W	0.07	—



NOTE: All dimensions in mm. Angles in degrees.

DIMENSION	MAX.	MIN.
A	11.6	11.4
B	12.6	12.3
C	1.1 x 45°	TYPICAL
D	1.3	TYPICAL
E	10.8	10.0
F	0.46	TYPICAL
G	7°	3°
H	7°	3°
J	4.5	4.3
K	2.5	TYPICAL
L	1.1	0.5
M	0.59	TYPICAL
N	45°	TYPICAL