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CML Semiconductor Products

PRODUCT INFORMATION

FX429A 1200/2400 Baud FFSK Modem for Trunked Radio Systems

Publication D/429A/1 January 1995
Provisional Information

Features

- Band III and General Purpose Trunked Radio Applications
- Full-Duplex 1200 and 2400 Baud Operation
- High Intelligence
- Error Check Word Generation and Checking
- Frame SYNC and SYNT Detection
- Preamble Generation
- µProcessor Compatible Interface
- Low Power Consumption
- General Purpose Timer

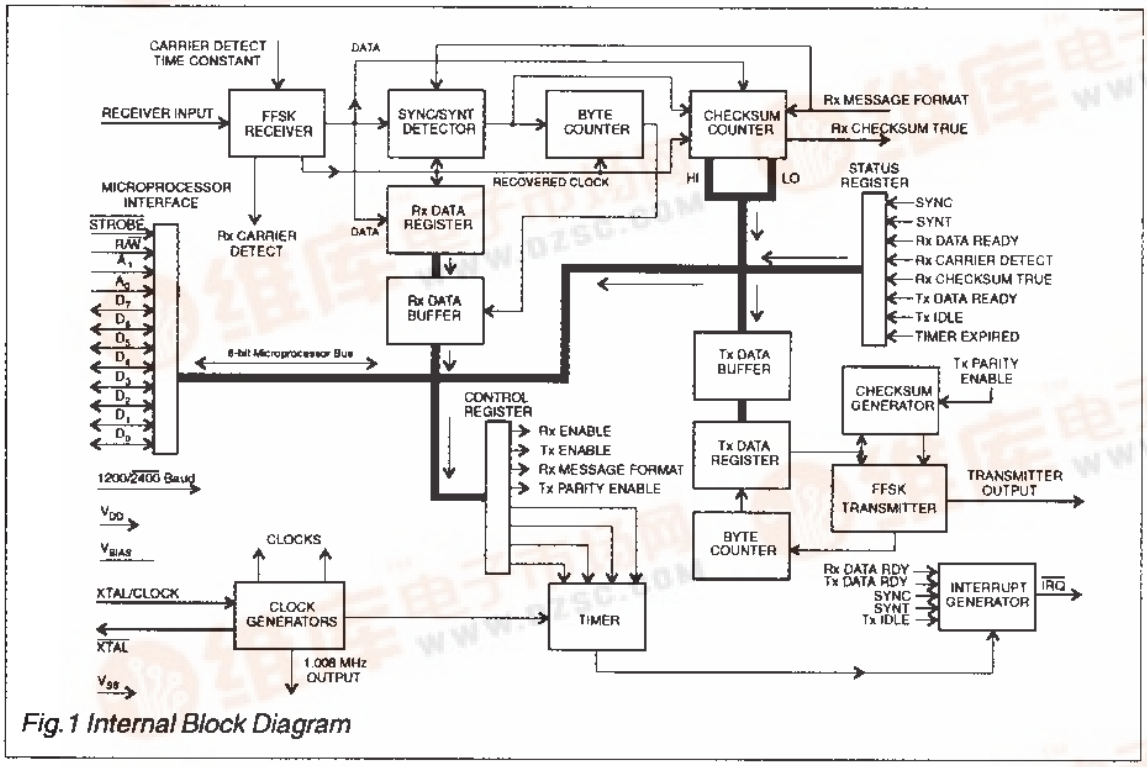


Fig.1 Internal Block Diagram

FX429A

Brief Description

The FX429A is a single-chip CMOS 1200 and 2400 baud FFSK modem, designed primarily for use in trunked radio systems but may also be employed in other general purpose radio or line data communication applications. The device has been designed to conform to the UK Band III trunked radio protocols MPT 1317/1327.

The FX429A is full duplex at 1200 and 2400 baud and includes an 8-bit parallel microprocessor interface and a programmable timer which may be set for interrupt periods of 8 to 120 bits.

Preamble may be generated by the device in transmit. The 16-bit SYNC or SYNT words are detected in receive. An error check word is automatically generated in transmit and error checking is performed in the receive mode. An on-chip Xtal/clock generator requiring an external 4.032MHz Xtal or clock input provides both 4.032MHz and 1.008MHz outputs and performs all modem timings. The FX429A requires a single 5-volt power supply and has a powersave facility.

This device is available in both DIL and SMD packages.

Pin Number Function

FX429A J4	FX429A L1/L2	
1	1	V_{BIAS}: The internal circuitry bias line, held at $V_{DD}/2$ this pin must be decoupled to V_{SS} by a capacitor, see Figure 3.
2	2	**Transmit Output:** The 1200 baud, 1200Hz/1800Hz and 2400 baud, 1200Hz/2400Hz FFSK Tx output. When not enabled by the Control Register (D_0) its output impedance is set high.
3	4	**Receiver Input:** The 1200/2400 baud received FFSK signal input. The 1200Hz/1800Hz, 1200Hz/2400Hz audio to this pin must be ac coupled via a capacitor, see Figure 3.
5	5	V_{DD}: Positive Supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to V_{SS} by a capacitor, see Figure 3.
6	6	**Carrier Detect Time Constant:** The on-chip Carrier Detect function requires external component(s) on this pin. See Figure 3 for recommended component(s).
7	7	**Xtal/Clock:** The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here, see Figure 3.
8	8	$\overline{\text{Xtal}}$: The output of the 4.032 MHz clock oscillator.
9	9	D_0: **Microprocessor Data Interface**
10	10	D_1:
11	11	D_2:
12	12	D_3: These 8 lines are used by the device to communicate with a microprocessor
13	13	D_4 : with the R/$\overline{W}$, A_0 and A_1 inputs determining register selection.
14	14	D_5 :
15	15	D_6 :
16	16	D_7 :

Pin Number		Function
FX429A J4	FX429A L1/L2	
17 18	17 18	**A_0 : Register Selection:** These inputs, with the R/$\overline{W}$ input, select the required register to the data bus as shown in Table 1 (below). **A_1 :**

Table 1

Register	R/$\overline{W}$	A_0	A_1
Control	0	1	1
Status	1	1	1
Rx Data	1	0	1
Tx Data	0	0	1
Syndrome Low	1	0	0
Syndrome High	1	1	0

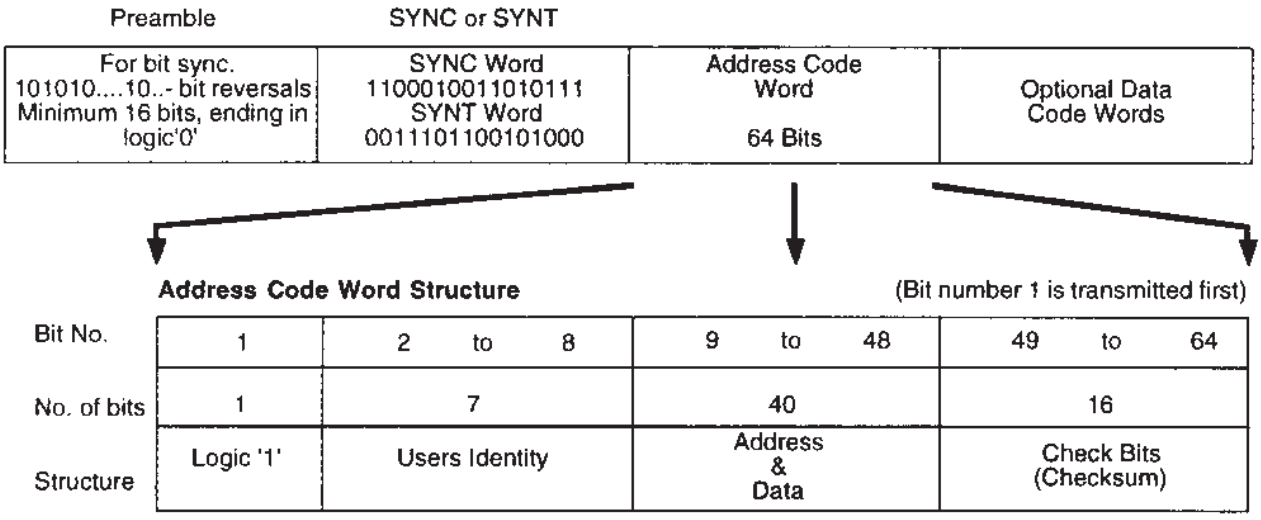
19	19	**$\overline{\text{Strobe}}$:** Performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating the high order address bits with a Read/Write clock. The FX429A is selected when this pin is a logic '0'.
20	20	**R/$\overline{W}$:** Used in conjunction with A_1 and A_0 to determine which internal registers are connected to the data interface pins (D_0 to D_7) during $\overline{\text{Strobe}}$.
21	21	**$\overline{\text{IRQ}}$:** Interrupt Request. This line will go to a logic '0' when an interrupt occurs. This output can be "wire OR'd" with other active low components (100kΩ pullup to V_{DD}). The conditions that cause the interrupts are indicated at the Status Register and are as follows: *Timer Expired* *Rx Data Ready* *Tx Data Ready* *Tx Idle* *Rx SYNC Detect* *Rx SYNT Detect*
22	24	**1200/$\overline{2400}$ Baud Select:** A logic '1' on this pin selects the 1200 baud option. Tone frequencies are: one cycle of 1200Hz represents a logic '1', one and a half cycles of 1800Hz represents a logic '0'. A logic '0' on this pin selects the 2400 baud option. Tone frequencies are: one half cycle of 1200Hz represents a logic '1', one cycle of 2400Hz represents a logic '0'. This pin has an internal 1MΩ pullup resistor.
23	22	**V_{SS}:** Negative Supply (GND).
24	23	**Clock ÷ 4:** A 1.008 MHz (X_1 ÷ 4) clock is available at this output for external circuit use, note the source impedance and source current limits.
4	3	Leave this pin open-circuit.

Modems in Mobile Data Signalling ..... An Introduction

Digital Code Format

The recommended Digital Code Format for use over Land Mobile Radio Systems is detailed in the UK Department of Trade and Industry, Radio Regulatory Division's publications MPT 1317 and MPT 1327, and is as described briefly below.

Fig. 2 The Data stream – Rx and Tx, the minimum overall transmission length is 96 bits.



Operation

The FX429A can be used for Full-Duplex operation with the host microprocessor only having to operate on the data whilst the modem (FX429A) handles all other signalling routines and requirements.

In the **Tx** mode the FX429A will :-
(1) Internally generate and transmit a preamble – bit reversals, for system bit synchronization.
(2) Accept from the host, and transmit, a 16-bit 'SYNC' or 'SYNT' word.
(3) Accept from the host, and transmit, 6 bytes of data (Address Code Word).
(a) Upon a software command, internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes. – or –
(b) Upon a software command, disable internal checksum generation and allow continuous data transmission.
(4) Transmit 1 'hang bit' and go idle when all loaded data traffic has been sent (followed by a "Tx Idle" interrupt).

In the **Rx** mode the FX429A will :-
(1) Detect and achieve bit synchronization within 16 bits.
(2) Search for and detect the 16-bit 'SYNC'/'SYNT' word.
(3) Output all received data after 'SYNC/SYNT,' in byte form.
(4) Upon a software command (Rx Message Format), use the received checksum to calculate the presence (if any) of errors, and advise the host with an interrupt and a 16-bit Syndrome word.
Note – In Rx a software command is used to determine whether a 'SYNC'/'SYNT' word is required after every 8 (6 data + 2 checksum) received bytes, or "data" is received continually.
Normally the 'SYNC' word is used on the Control data channel and the 'SYNT' word is used on the Traffic data channel.

Non MPT Application – Full-Duplex

The functions described in this section, to allow the FX429A modem to operate as a general purpose device, are obtained using the commands and indications detailed in the "Register Instructions" pages.

Tx – When enabled the device transmits a "101010.....10" preamble until data for transmission is loaded by the host microprocessor.
Transmits 6 bytes of the loaded data followed by a 2-byte checksum based on that data. As long as Tx data is loaded the transmitter will transmit, the 2-byte checksum being produced after every 6 bytes (8 byte packages).
Automatic checksum generation can be inhibited by a software command to allow transmission of continuous data streams.

Rx – When enabled requires the 16-bit SYNC or SYNT word (see notes) before outputting data bytes. The modem receiver will then output continuous bytes of data, after every 6 bytes received a 2-byte checksum word will be output and can be ignored or used for error checking.

Control Register $A_1 = 1$ $A_0 = 1$ $R/\overline{W} = 0$ Write Only

The Control Register, when selected, directs the modem's operation as described below.

Bit	Description	Function	Set = logic '1' (High) Clear = logic '0' (Low)
Bit 0 D_0	**Tx Enable**	**Set** – D_0 enables the transmitter for operation. A '0 – 1' transition causes bit synchronization and the start of 1010.....10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the Tx Data Buffer before one byte has been sent then that data will follow, otherwise whole bytes of preamble will continue until data is loaded. **Clear** – The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced.	
Bit 1 D_1	**Tx Parity Enable**	**Set** – D_1 indicates to the transmitter that 2–byte checksums are to be generated by the modem. A '0 – 1' transition starts checksum generation on the next six bytes loaded from the Tx Data Buffer into the Tx Data Register. Checksum generation continues for every 6 bytes loaded until this bit is cleared. The transmiter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded checksum generation will abort, the transmission will cease after one 'hang' bit has been sent and Bit 4 in the Status Register (Tx Idle) will be set. No checksum will be transmitted. **Clear** – No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written".	
Bit 2 D_2	**Rx Enable**	**Set** – D_2 enables the receiver for operation. No data is produced (i.e. No Rx Data Ready interrupts) until a 'SYNC' or 'SYNT' word is found in the received bit stream. **Clear** – The receiver is disabled and all interrupts caused by the receiver are inhibited.	
Bit 3 D_3	**Rx Message Format**	**Set** – D_3 is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If 'set' the receiver will assume that the next 6 bytes are data and will start error checking accordingly. **Clear** – The receiver will stop data transfer to the host after the 2 checksum bytes until another 'SYNC' or 'SYNT' frame word is received.	
Bit 4 D_4	**Timer LSB**	These four bits control the timer as follows :-	
Bit 5 D_5	**Timer**		
Bit 6 D_6	**Timer**		
Bit 7 D_7	**Timer MSB**		

D_7	D_6	D_5	D_4	
0	0	0	0	Reset counter and disable timer interrupts
0	0	0	1	Count and interrupt every - 8 bits
0	0	1	0	" " " 16 bits
0	0	1	1	" " " 24 bits
0	1	0	0	" " " 32 bits
0	1	0	1	" " " 40 bits
0	1	1	0	" " " 48 bits
0	1	1	1	" " " 56 bits
1	0	0	0	" " " 64 bits
1	0	0	1	" " " 72 bits
1	0	1	0	" " " 80 bits
1	0	1	1	" " " 88 bits
1	1	0	0	" " " 96 bits
1	1	0	1	" " " 104 bits
1	1	1	0	" " " 112 bits
1	1	1	1	" " " 120 bits

If a new timer value is written to these inputs within 1 byte period of the last timer interrupt then the next timer period will be correct without first having to reset the timer, otherwise the timer must be reset to zero and then set to the new time.

Tx Enable

If using the internal Tx preamble generation facility, e.g. with the internal timer setting the preamble length, the device may occaisionally produce a Tx Ready interrupt immediately after a Tx Enable command. User software should handle this occurrence by either:

a. *Detecting that the timer interrupt status bit is not set and that it is not appropriate to load Tx data at this time, or,*

b. *Not using the timer. i.e. immediately after Tx Enable, reading the Status Register and loading a byte of preamble. This resets any interrupt. The length of preamble transmitted is now controlled by the number of bytes loaded.*

Status Register $A_1 = 1$ $A_0 = 1$ $R/\overline{W} = 1$ Read Only

When an interrupt is generated the $\overline{IRQ}$ Output goes Low with the Status Register bits indicating the sources of the interrupt.

Bit	Description	Function Set = logic '1' (High) Clear = logic '0' (Low)
Bit 0 D_0	**Rx Data Ready**	D_0 when set, causes an interrupt indicating that received data is ready to be read from the Rx Data Buffer. This data must be read within 8 bit periods. **Set** – when a byte of data is loaded into the Rx Data Buffer, if a frame (SYNC/SYNT) word has been received. **Bit and Interrupt Cleared** – (i) by a read of the Status Register followed by a read of the Rx Data Buffer or (ii) by Rx Enable going Low.
Bit 1 D_1	**Rx Checksum True**	D_1 when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the Rx Data Ready bit (D_0) is set for the second byte of the received checksum, does not cause an interrupt. **Set** – by a correct comparison between the received and generated checksums. **Cleared** – (i) by a read of the Status Register followed by a read of the Rx Data Buffer, or (ii) by Rx Enable going Low.
Bit 2 D_2	**Rx Carrier Detect**	D_2 is a "Real Time" indication from the modem receiver's carrier detect circuit and does not cause an interrupt. When FFSK tones are present at the receiver input this bit goes High, for no FFSK input this bit goes Low. When the Rx Enable bit (D_2– Control Register) is Low Rx Carrier Detect will go Low.
Bit 3 D_3	**Tx Data Ready**	D_3 when set, causes an interrupt to indicate that a byte of data should be written to the Tx Data Buffer within 8 bit periods. **Set** – (i) when the contents of the Tx Data Buffer are transferred to the Tx Data Register, or (ii) when the Tx Enable is set – No interrupt is generated in this case. **Bit Cleared** – (i) by a read of the Status Register followed by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. **Interrupt Cleared** – (i) by a read of the Status Register, or (ii) by Tx Enable going Low.
Bit 4 D_4	**Tx Idle**	D_4 causes an interrupt when set, to indicate that all loaded data and one 'hang' bit have been transmitted. **Set** – one bit period after the last byte is transmitted. This last byte could be either "checksum" or " loaded data" depending upon the Tx Parity Enable state (Control Register D_1). **Bit Cleared** – (i) by a write to the Tx Data Buffer, or (ii) by Tx Enable going Low. **Interrupt Cleared** – (i) by a read of the Status Register, or (ii) by Tx Enable going Low.
Bit 5 D_5	**Timer Interrupt**	D_5, when set, causes an interrupt to indicate that the set timer period has expired. (Control Register D_4 — D_7). **Set** – by the timer. **Bit and Interrupt Cleared** – by a read of the Status Register.
Bit 6 D_6	**Rx SYNC Detect** *	D_6, when set, causes an interrupt to indicate that a 16-bit 'SYNC' word (1100010011010111) has been detected in the received bit stream. **Set** – on receipt of the 16th bit of a 'SYNC' word. **Bit and Interrupt Cleared** – (i) By a read of the Status Register, or (ii) by Rx Enable going Low.
Bit 7 D_7	**Rx SYNT Detect** *	D_7, when set, causes an interrupt to indicate that a 16-bit 'SYNT' word (0011101100101000) has been detected in the received bit stream. **Set** – on receipt of the 16th bit of a 'SYNT' word. **Bit and Interrupt Cleared** – (i) By a read of the Status Register, or (ii) by Rx Enable going Low.
* ***Note*** –		'SYNC' and 'SYNT' Detection is disabled whilst the checksum checker is running.

Rx Data Buffer — $A_1 = 1$ — $A_0 = 0$ — $R/\overline{W} = 1$ — Read Only

These 8 bits are the last byte of data received with bit 7 being received first. *Note the relative positions of the **MSB** and **LSB** presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.*

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

Tx Data Buffer — $A_1 = 1$ — $A_0 = 0$ — $R/\overline{W} = 0$ — Write Only

These 8 bits loaded to the Tx Data Buffer are the next byte of data that will be transmitted, with bit 7 being transmitted first. *Note the relative positions of the **MSB** and **LSB** presented in this bit stream, the position may be different to the convention used in other µProcessor peripherals.* If the the Tx Parity Enable bit (Control Register D_1) is set, a 2–byte checksum will be inserted and transmitted by the modem after every 6 transmitted " message " bytes.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

The Syndrome Word

This 16-bit word (both **Low** and **High** bytes) may be used to correct errors.
Bits S_1 to S_{15} are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of " received message." For a correct message all 15 bits (S_1 to S_{15}) will be zero.
The 2 Syndrome bytes are valid when the Rx Data Ready bit (Status Register D_0) is set for the second byte of the received checksum and should be read, if required, before 8 byte periods.

Syndrome Low Byte — $A_1 = 0$ — $A_0 = 0$ — $R/\overline{W} = 1$ — Read Only

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S1	S2	S3	S4	S5	S6	S7	S8

Syndrome High Byte — $A_1 = 0$ — $A_0 = 1$ — $R/\overline{W} = 1$ — Read Only

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S9	S10	S11	S12	S13	S14	S15	PARITY ERROR

D_7 – This is a "Parity Error Bit" – Indicating an error between the received parity bit and the parity bit internally generated from the incoming message. Thus for a correctly received message all 16 bits of the Syndrome Word (S_1 to S_{15} and Parity Error) will be zero.

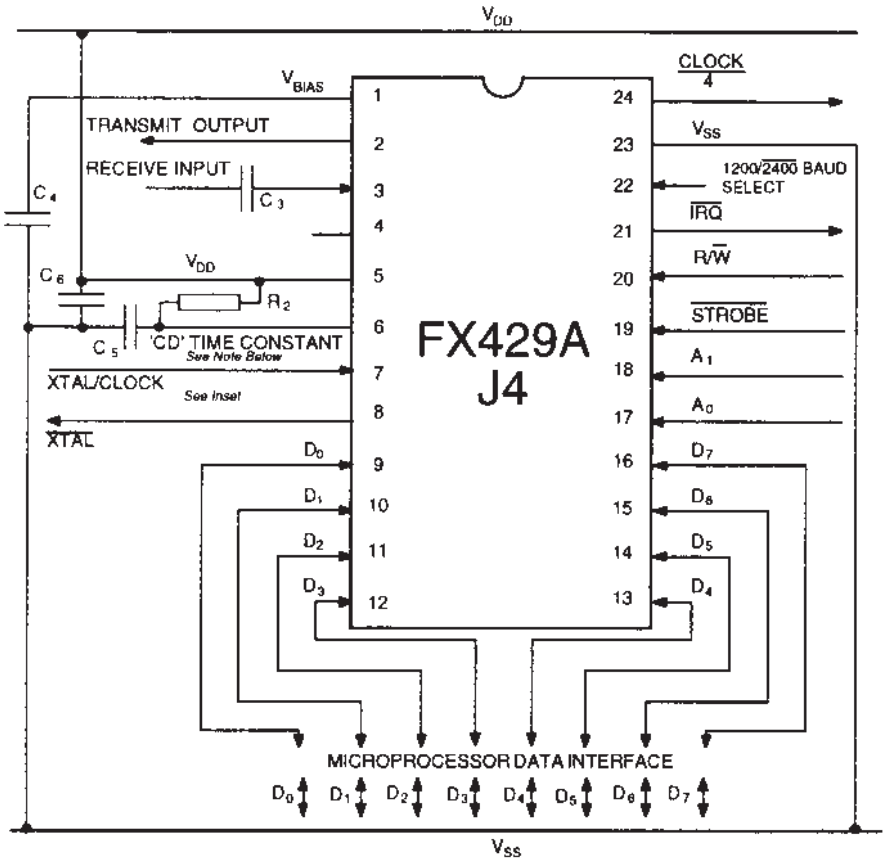
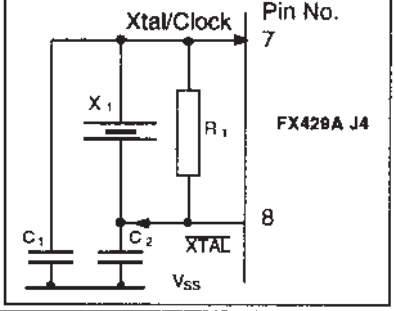


Fig. 3 Recommended External Components

Component References	
Component	**Unit Value**
R_1	1M
R_2	1M
C_1	33p
C_2	33p
C_3	0.1µ
C_4	1.0µ
C_5	1.0µ
C_6	1.0µ
X_1	4.032MHz

Tolerances. Resistors ± 10%
Capacitors ± 20%

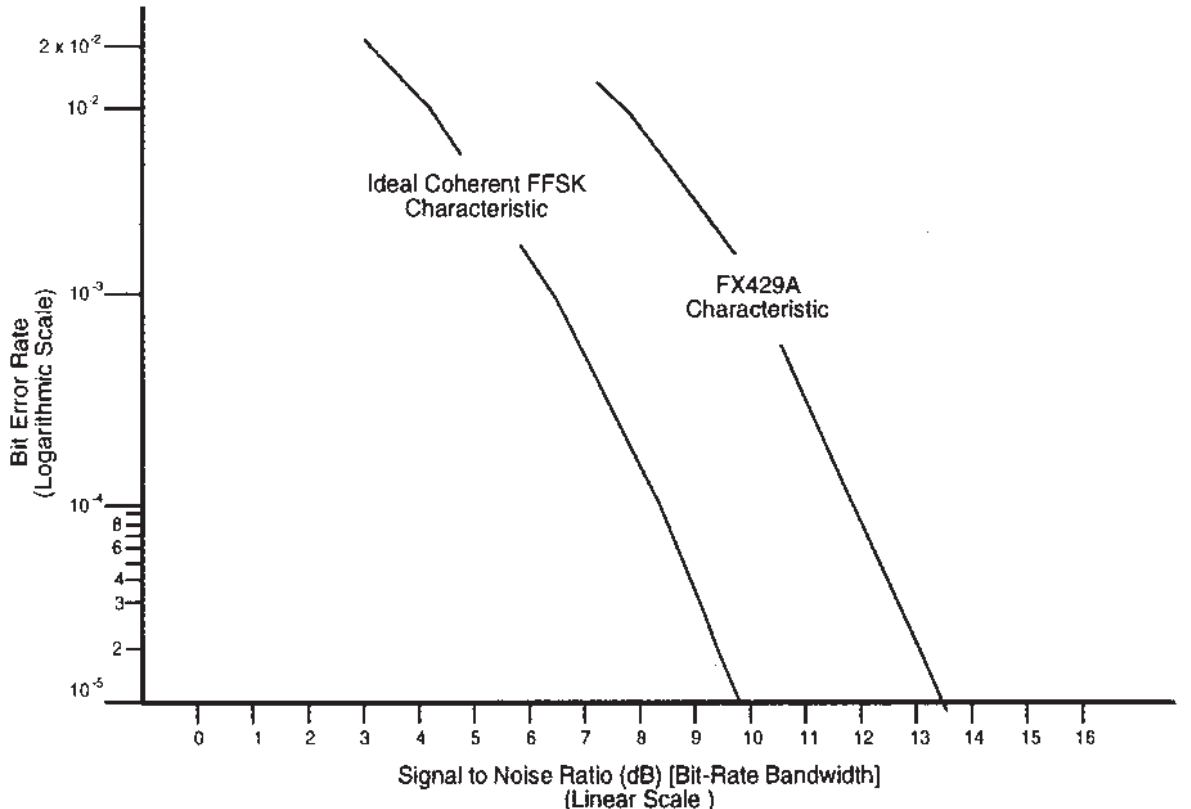
Recommended Xtal Components



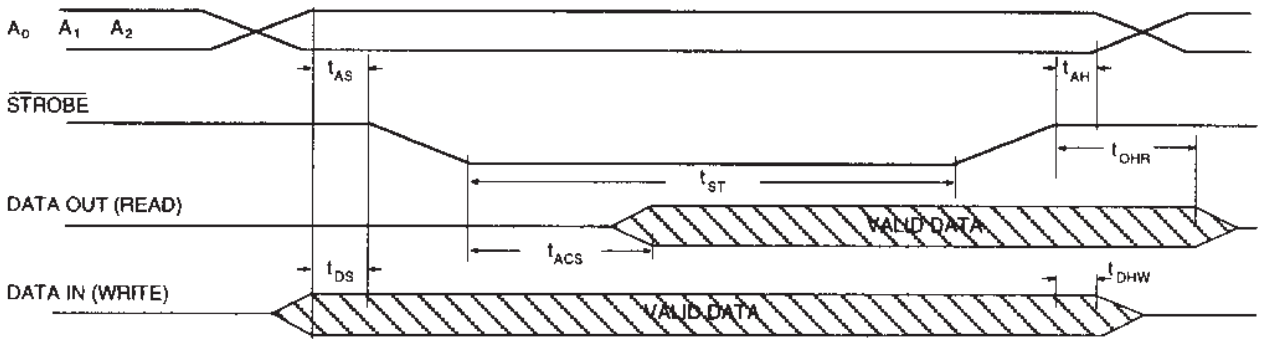
CD *(Carrier Detect)* **Time Constant**

The value of the Carrier Detect capacitor, C_5, determines the carrier detect time constant. A long time constant (larger value C_5), results in improved noise immunity but increased response time. C_5 may be varied to optimise noise immunity/response time.

1. With R_2 = 1MΩ and C_5 = 1µF as external components for the carrier detect function at 1200 baud only.
2. By using C_5 = 0.1µF and removing R_2 completely the FX429A will operate at both 1200 and 2400 baud rates.



Timing Information

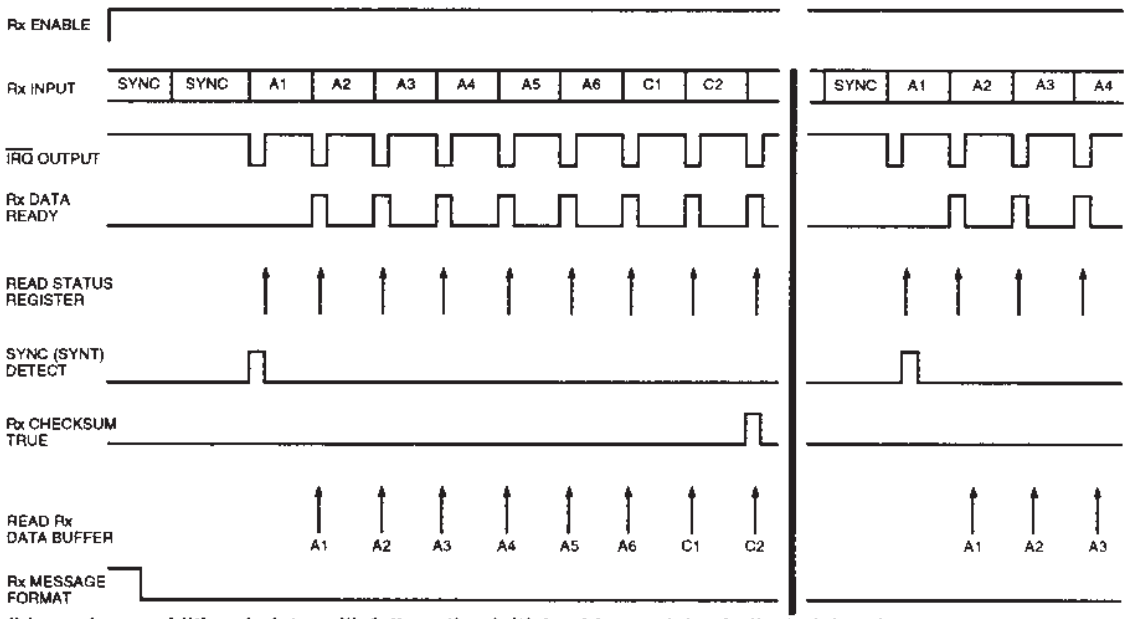


t_{ACS} – Access Time
t_{AS} – Address Set-Up Time
t_{DS} – Data Set-Up Time
t_{AH} – Address Hold Time
t_{DHW} – Data Hold Time (Write)
t_{OHR} – Output Hold Time (Read)
t_{ST} – Strobe Time

Fig. 5 Read and Write Timing Diagram

Operation – Rx

(a) Rx – where SYNC/SYNT is required after every message



(b) – where additional data will follow the initial address data, indicated by the state of the Rx Message Format bit

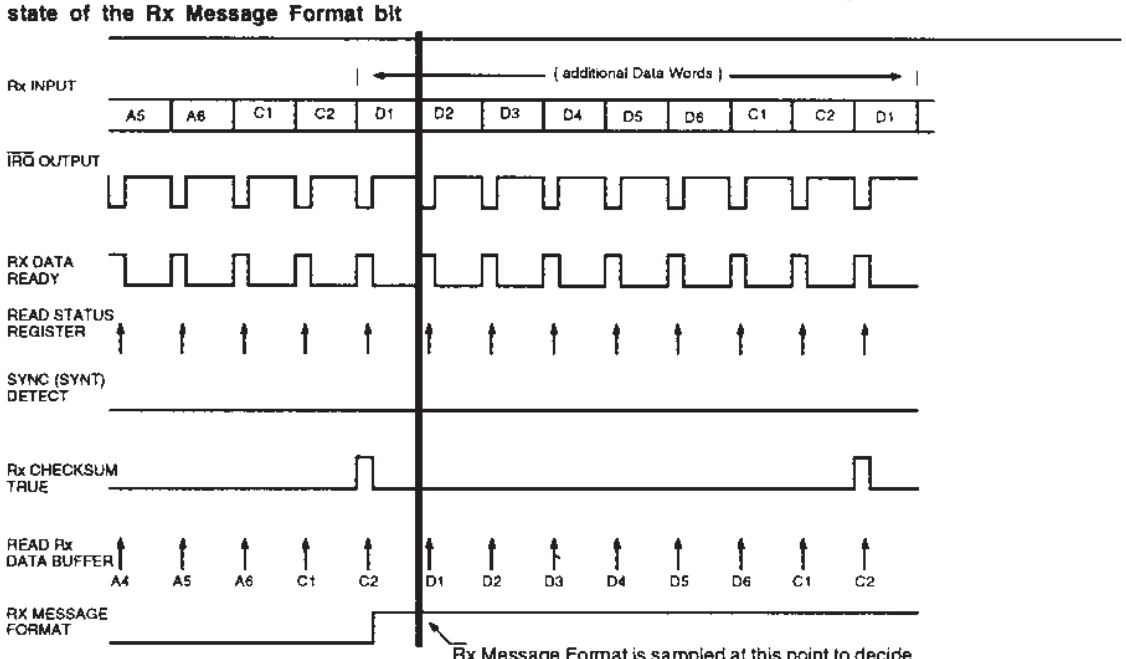


Fig. 6 Simplified Rx Timing

Operation – Tx

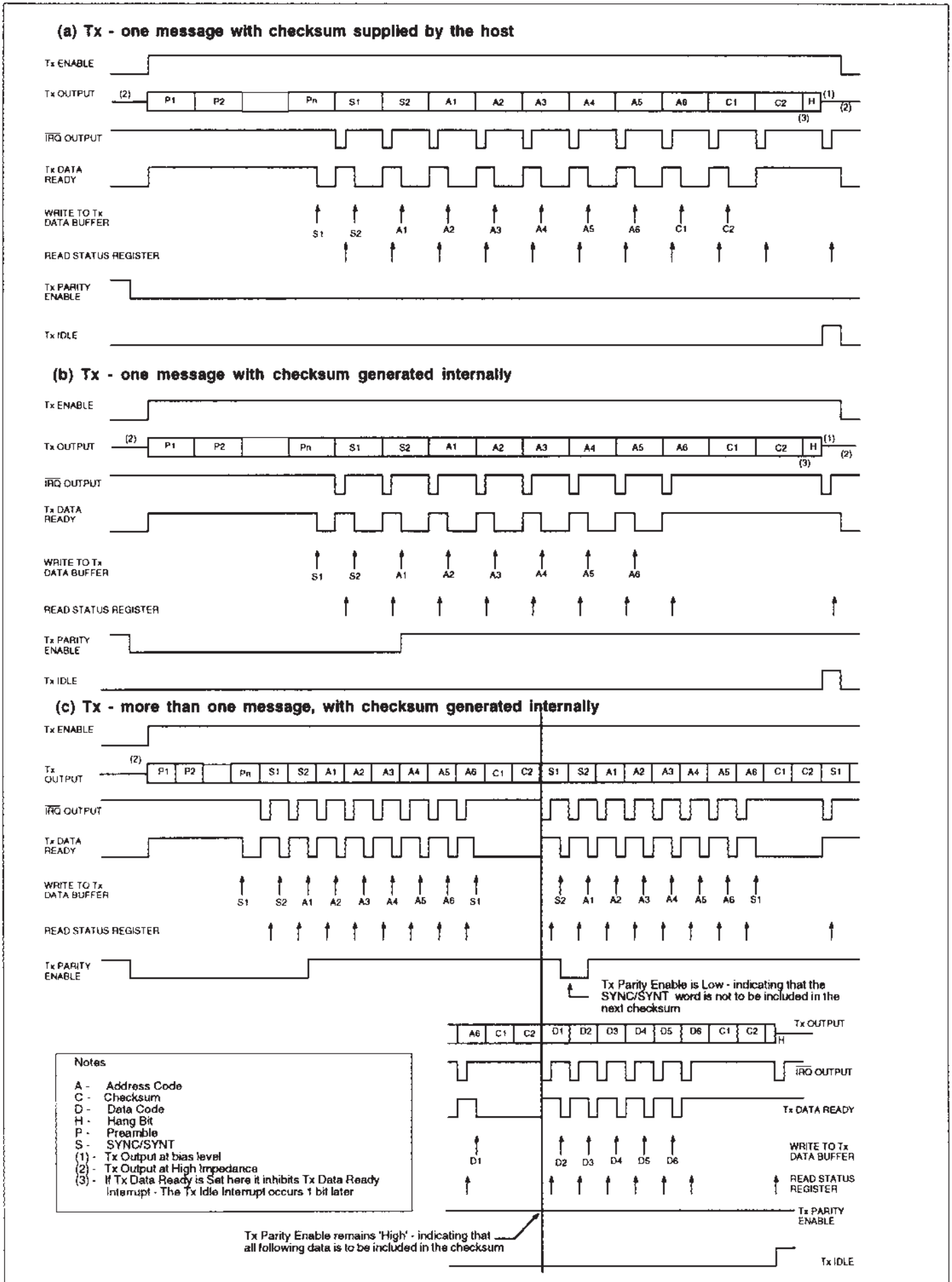
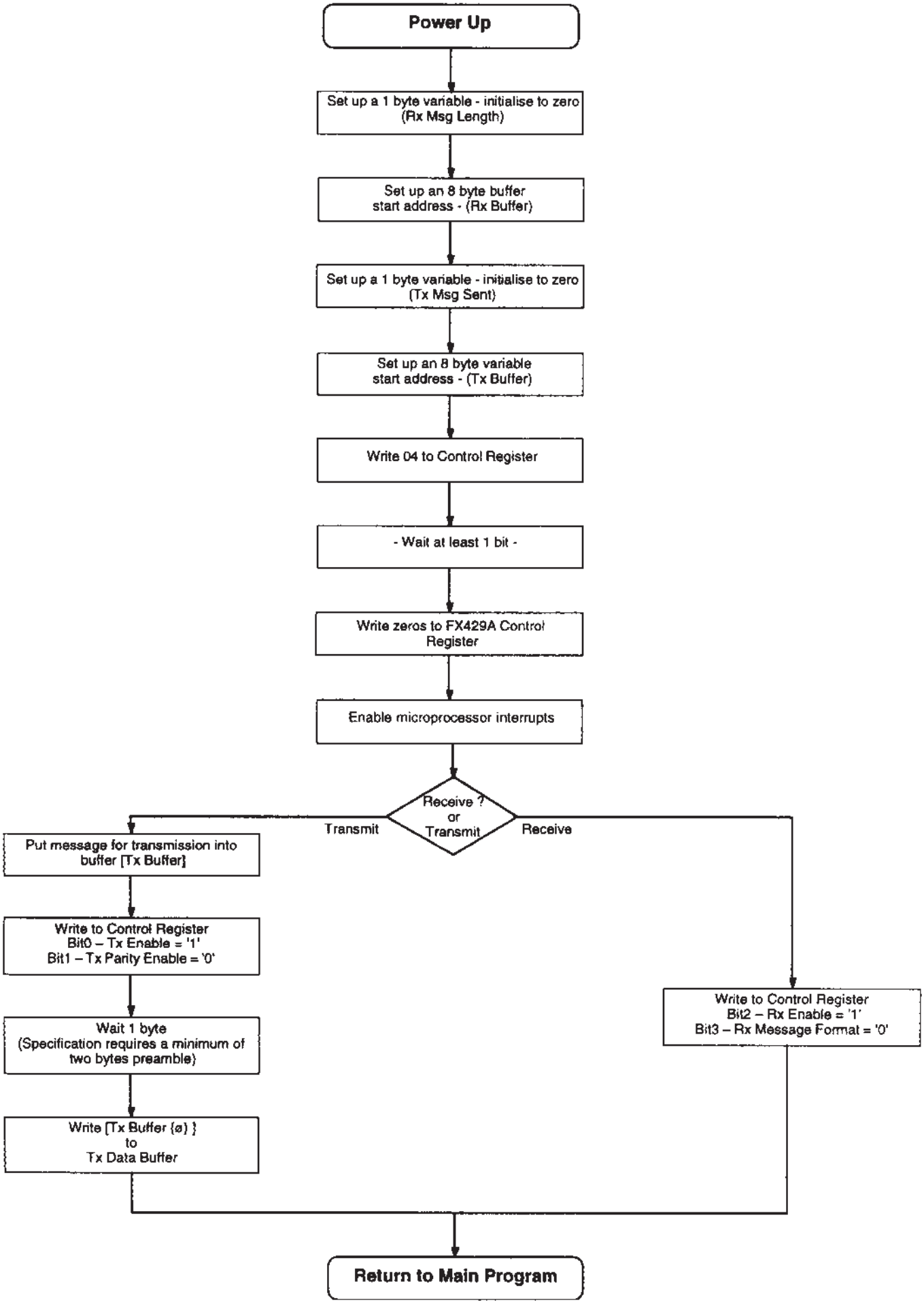
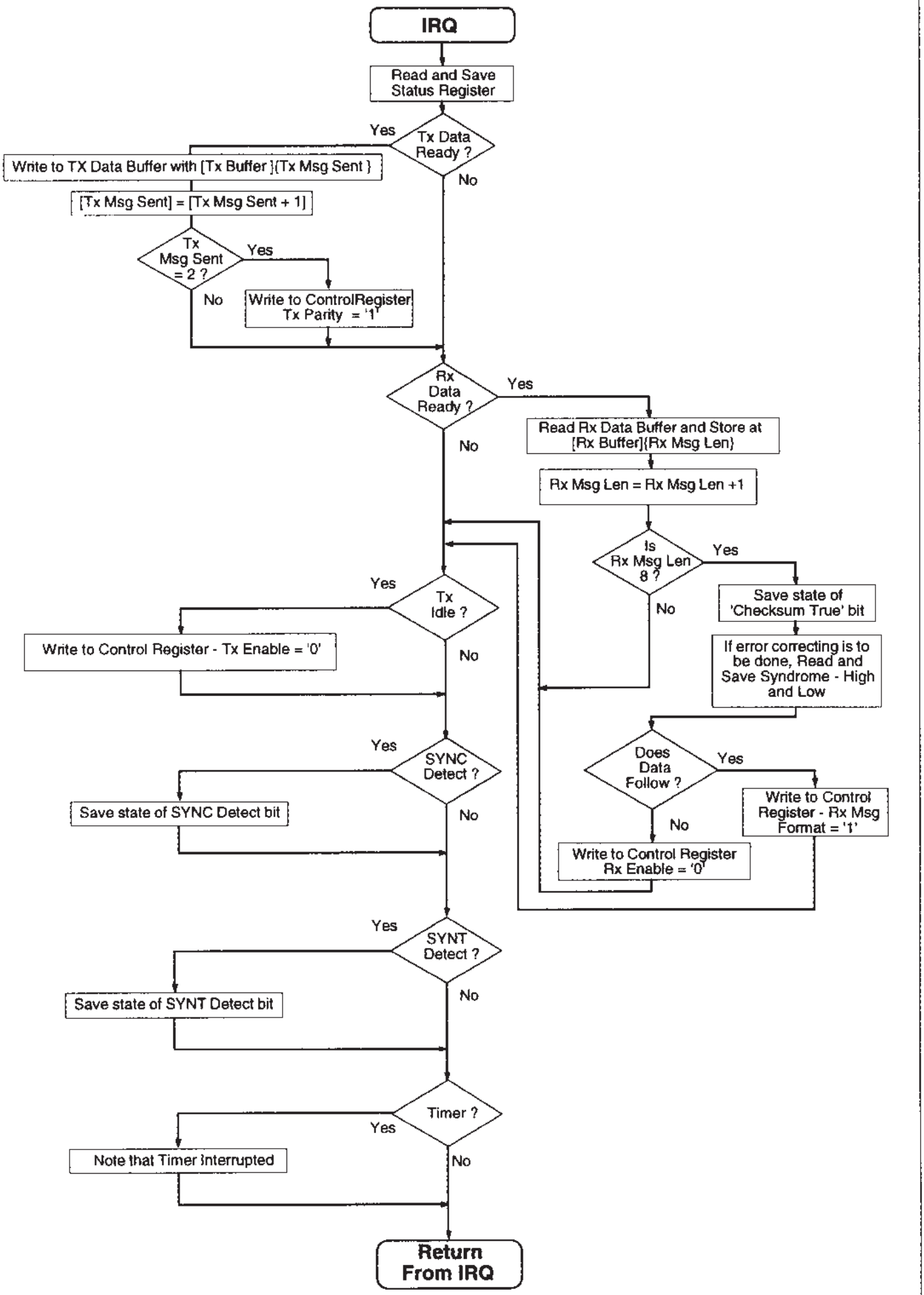


Fig. 7 Simplified Tx Timing

Basic Power-Up Software



Basic Software Interrupt Flow



Specification

Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

Supply voltage		-0.3 to 7.0V
Input voltage at any pin (ref V_{SS} = 0V)		-0.3 to (V_{DD} + 0.3V)
Sink/source current (supply pins)		+/- 30mA
(other pins)		+/- 20mA
Total allowable device dissipation @ T_{AMB} 25°C		800mW Max.
Derating		10mW/°C
Operating temperature range:	**FX429A J4**	-30°C to +85°C (ceramic)
	FX429A L1/L2	-30°C to +70°C (plastic)
Storage temperature range:	**FX429A J4**	-55°C to +125°C (ceramic)
	FX429A L1/L2	-40°C to +85°C (plastic)

Operating Limits

All characteristics are measured using the following parameters unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C. Xtal/Clock f_o = 4.032 MHz. Audio level 0dB ref: = 300mV rms.

Bit Rate Bandwidth = 1200Hz.

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	–	5.5	V
Supply Current Ranges					
Rx and Tx Enabled		–	–	7.0	mA
Rx Enabled, Tx Disabled		–	4.0	6.0	mA
Rx Disabled, Tx Enabled		–	–	7.0	mA
Rx and Tx Disabled		–	1.5	2.5	mA
Dynamic Values					
Modem Internal Delay		–	1.5	–	ms
Interface Levels					
Output Logic '1' Source Current	2	–	–	120	µA
Output Logic '0' Sink Current	3	–	–	360	µA
Three State Output Leakage Current		–	–	4.0	µA
D_0 – D_7 Data In/Out	1				
Logic '1' Level		3.5	–	–	V
Logic '0' Level		–	–	1.5	V
A_1, A_0, R/W, $\overline{\text{STROBE}}$, $\overline{\text{IRQ}}$	4				
Logic '1' Level		4.0	–	–	V
Logic '0' Level		–	–	1.0	V
Analogue Impedances					
Rx Input		100	–	–	kΩ
Tx Output (Enabled)		–	10	–	kΩ
Tx Output (Disabled)		–	5.0	–	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10.0	–	–	MΩ
R_{OUT}	5	–	30.0	–	kΩ
Oscillator Gain		–	25.0	–	dB
Xtal frequency		–	4.032	–	MHz
Timing – (Fig. 5)					
Access Time – (t_{ACS})		–	–	135	ns
Address Hold Time – (t_{AH})		0	–	–	ns
Address Set-up Time – (t_{AS})		0	–	–	ns
Data Hold Time (Write) – (t_{DHW})		85	–	–	ns
Data Set-up Time (Write) – (t_{DS})		0	–	–	ns
Output Hold Time (Read) – (t_{OHR})		15	–	105	ns
Strobe Time – (t_{ST})		140	–	–	ns

Specification...

Characteristics		See Note	Min.	Typ.	Max.	Unit
Dynamic Values.....						
Receiver						
Signal Input Levels		6	–9.0	–2.0	+10.5	dB
Bit Error Rate		7				
@ 12dB Signal/Noise Ratio			–	7.0	–	10^{-4}
@ 20dB Signal/Noise Ratio			–	1.0	–	10^{-8}
Synchronization @ 12dB Signal/Noise Ratio		8				
Probability of Bit 16 being correct			–	99.5	–	%
Carrier Detect Response Time		8	–	13.0	–	ms
Transmitter						
Output Level			–	8.25	–	dB
Output Level Variation			-1.0	–	+1.0	dB
Output Distortion			–	3.0	5.0	%
3rd Harmonic Distortion			–	2.0	3.0	%
Logic '1' Frequency	1200 baud	9	–	1200	–	Hz
	2400 baud	9	–	1200	–	Hz
Logic '0' Frequency	1200 baud	9	–	1800	–	Hz
	2400 baud	9	–	2400	–	Hz
Isochronous Distortion						
1200Hz – 1800Hz/1200Hz - 2400Hz			–	25	40	µs
1800Hz – 1200Hz/2400Hz - 1200Hz			–	20	40	µs

Notes

1. With each data line loaded as, C = 50pf and R = 10kΩ.
2. V_{OUT} = 4.6V.
3. V_{OUT} = 0.4V
4. Sink/Source currents ≤ 0.1mA.
5. Both Xtal and Xtal ÷ 4 Outputs.
6. With 50dB Signal/Noise Ratio.
7. See Figure 4, Bit Error Rate.
8. This Response Time is measured using a 10101010101....01 pattern input signal at a level of 230mV rms (-2.3dB) with no noise.
9. Dependent upon Xtal tolerance.

Checksum Generation and Checking

Generation – The checksum generator takes the 48 bits from the 6 bytes loaded into the Tx Data Buffer and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
This 16–bit word is used as the "Checksum."

Checking – The checksum checker does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo–2, by the generating polynomial;-

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

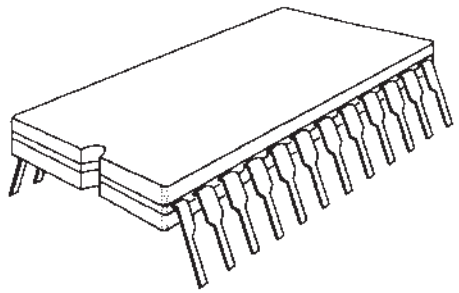
The 15 bits remaining in the polynomial divider are checked for all zero.
Secondly, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64).
If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the Rx Checksum True bit (SR D_1) bit is set.

Package Outlines

The FX429A is available in the package styles outlined below. Mechanical package diagrams and specifications are detailed in Section 10 of this document.
Pin 1 identification marking is shown on the relevant diagram and pins on all package styles number anti-clockwise when viewed from the top.

FX429AJ4 24-pin cerdip DIL (J)

NOT TO SCALE



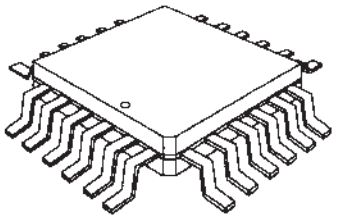
Max. Body Length 32.00mm
Max. Body Width 13.36mm

Handling Precautions

The FX429A is a CMOS LSI circuit which includes input protection. However precautions should be taken to prevent static discharges which may cause damage.

FX429AL1 24-pin quad plastic encapsulated bent and cropped (LG)

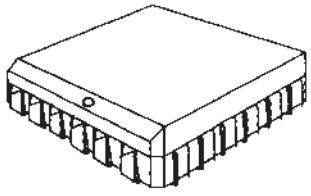
NOT TO SCALE



Max. Body Length 10.25mm
Max. Body Width 10.25mm

FX429AL2 24-lead plastic leaded chip carrier (LS)

NOT TO SCALE



Max. Body Length 10.40mm
Max. Body Width 10.40mm

Ordering Information

FX429AJ4 24-pin cerdip DIL (J)

FX429AL1 24-pin quad plastic encapsulated bent and cropped (LG)

FX429AL2 24-lead plastic leaded chip carrier (LS)

CML does not assume any responsibility for the use of any circuitry described. No circuit patent licences are implied and CML reserves the right at any time without notice to change the said circuitry.

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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