Ordering number:EN4895

FX855

MOSFET:N-Channel Silicon MOSFET
SBD:Schottky Barrier Diode

DC-DC Converter Applications

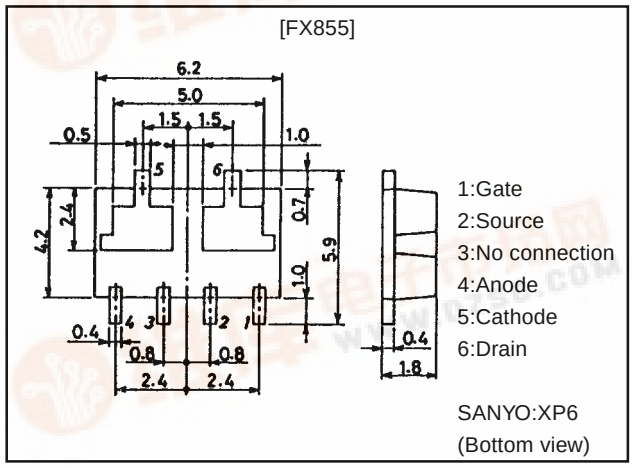
Features

- Composite type composed of a ow ON-resistance N-channel MOSFET for ultrahigh-speed switching and low-voltage driving and a fast-recovery, low forward -voltage Schottky barrier diode. Facilitates high-density mounting.
- The FX855 is formed with 2 chips, one being equivalent to the 2SK1470 and the other the SB05-09, placed in one package.

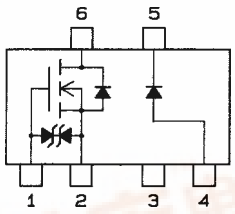
Package Dimensions

unit:mm

2119



Electrical Connection



1:Gate
2:Source
3:No connection
4:Anode
5:Cathode
6:Drain

(Top view)

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
[MOSFET]				
Drain-to-Source Voltage	V_{DSS}		60	V
Gate-to-Source Voltage	V_{GSS}		±15	V
Drain Current (DC)	I_D		2	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	8	A
Allowable Power Dissipation	P_D	Tc=25˚C	6	W
	P_D	Mounted on ceramic board (750mm²×0.8mm)	1.5	W
Channel Temperature	Tch		150	˚C
Storage Temperature	Tstg		–55 to +150	˚C
[SBD]				
Repetitive Peak Reverse Voltage	V_{RRM}		90	V
Non-repetitive Peak Reverse Surge Voltage	V_{RSM}		95	V
Average Rectified Current	I_O		500	mA
Surge Forward Current	I_{FSM}	50Hz sine wave, 1cycle	10	A
Junction Temperature	Tj		–55 to +125	˚C
Storage Temperature	Tstg		–55 to +125	˚C

· Marking:855

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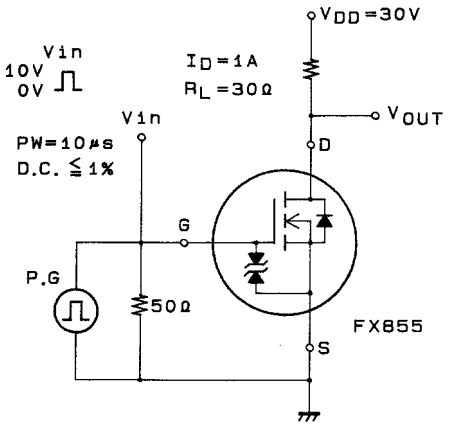
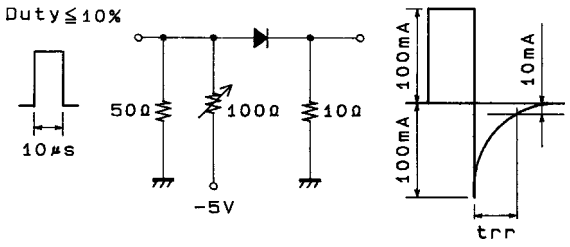
Electrical Characteristics at Ta = 25˚C

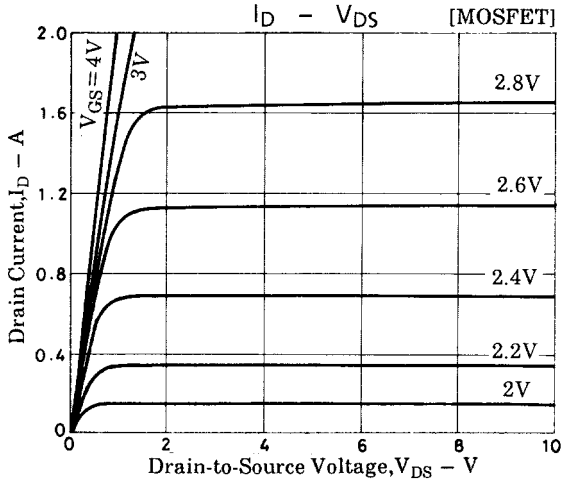
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[MOSFET]						
D-S Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0			100	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±12V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	1.0		2.0	V
Forward Transfer Admittance	$\|Y_{fs}\|$	V_{DS}=10V, I_D=1A	1.2	2.0		S
Static Drain-to-Source ON-State Resistance	$R_{DS(on)}$	I_D=1mA, V_{GS}=10V		0.35	0.45	Ω
	$R_{DS(on)}$	I_D=1A, V_{GS}=4V		0.45	0.6	Ω
Input Capacitance	Ciss	V_{DS}=10V, f=1MHz		150		pF
Output Capacitance	Coss	V_{DS}=10V, f=1MHz		60		pF
Reverse Transfer Capacitance	Crss	V_{DS}=10V, f=1MHz		12		pF
Turn-ON Delay Time	$t_{d(on)}$	See specified Test Circuit		6		ns
Rise Time	t_r	See specified Test Circuit		10		ns
Turn-OFF Delay Time	$t_{d(off)}$	See specified Test Circuit		60		ns
Fall Time	t_f	See specified Test Circuit		20		ns
Diode Forward Voltage	V_{SD}	I_S=2A, V_{GS}=0		1.0		V
[SBD]						
Reverse Voltage	V_R	I_R=300μA	90			V
Forward Voltage	V_F	I_F=500mA			0.7	V
Reverse Current	I_R	V_R=45V			80	μA
Interterminal Capacitance	C	V_R=10V, f=1MHz Cycle		34		pF
Reverse Recovery Time	trr	I_F=I_R=100mA, See specified Test CIrcuit			10	ns
Thermal Resistance	Rthj-a	Mounted on ceramic board (750mm²×0.8mm)		85		˚C/W

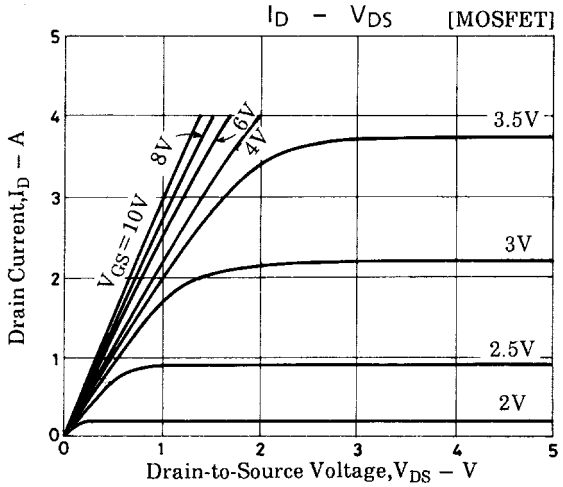
Switching Time Test CIrcuit [MOSFET]

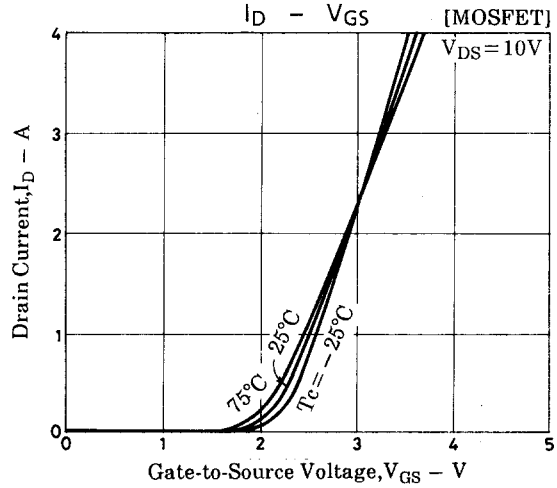


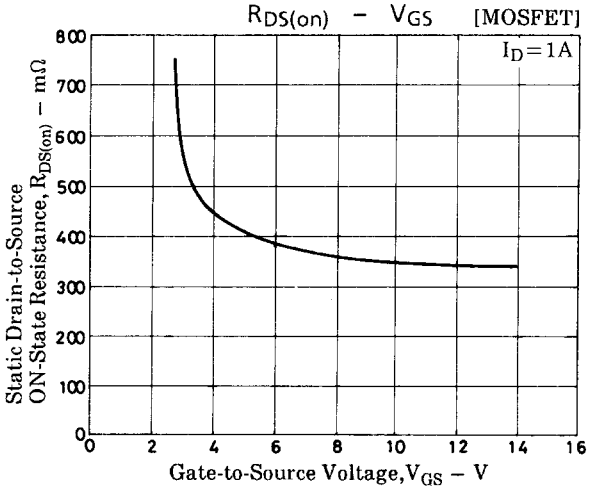
Trr Test Circuit [SBD]

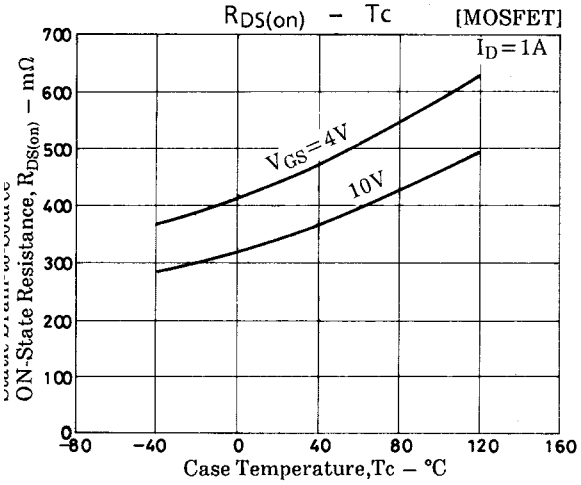


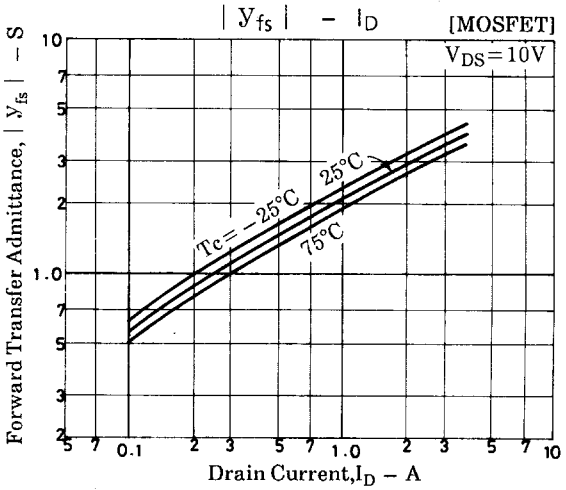


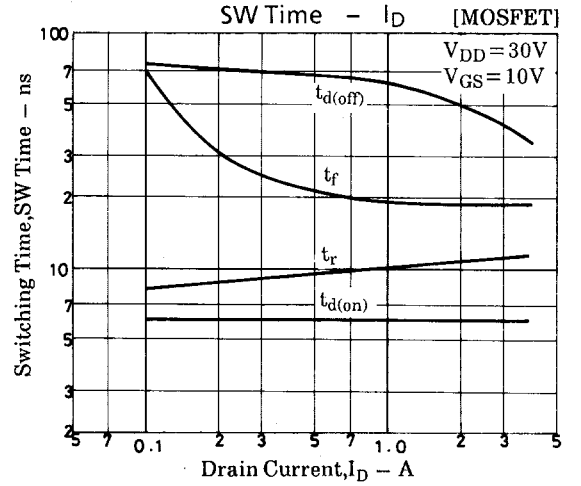


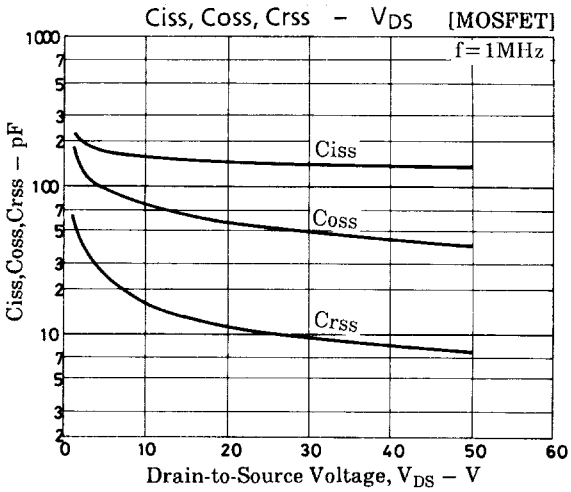

ID – VGS [MOSFET]
VDS=10V
Drain Current,ID – A
Gate-to-Source Voltage,VGS – V
75°C
25°C
Tc=–25°C

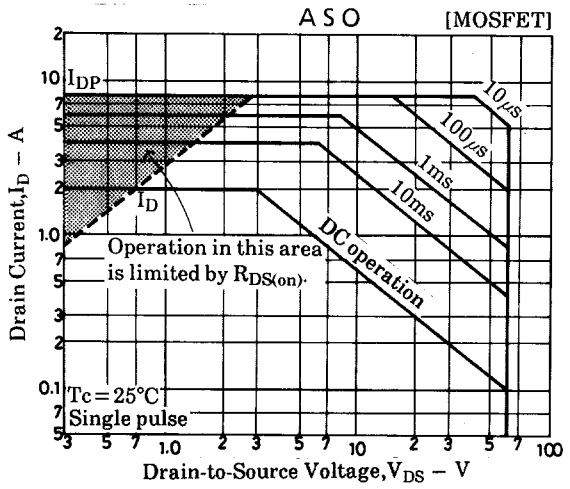

RDS(on) – VGS [MOSFET]
ID=1A
Static Drain-to-Source ON-State Resistance, RDS(on) – mΩ
Gate-to-Source Voltage,VGS – V

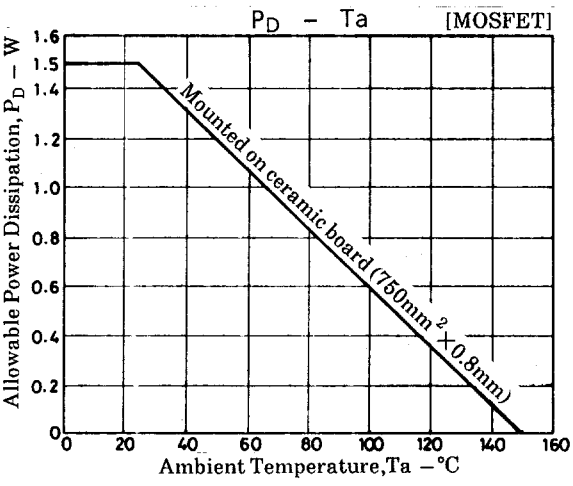

RDS(on) – Tc [MOSFET]
ID=1A
VGS=4V
10V
ON-State Resistance, RDS(on) – mΩ
Case Temperature,Tc – °C


| yfs | – ID [MOSFET]
VDS=10V
Tc=–25°C
25°C
75°C
Forward Transfer Admittance, | yfs | – S
Drain Current,ID – A

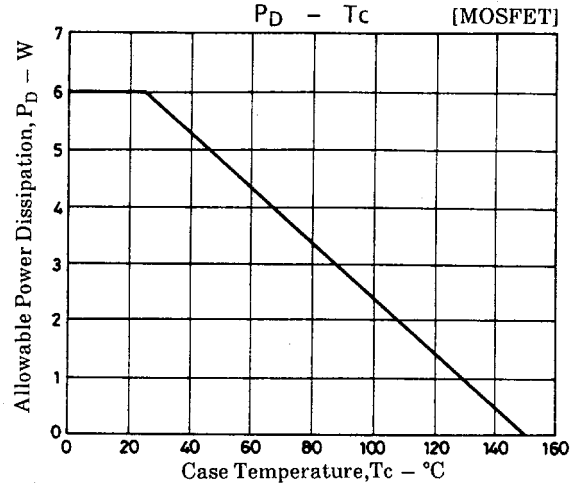

SW Time – ID [MOSFET]
VDD=30V
VGS=10V
td(off)
tf
tr
td(on)
Switching Time,SW Time – ns
Drain Current,ID – A


Ciss, Coss, Crss – VDS [MOSFET]
f=1MHz
Ciss
Coss
Crss
Ciss,Coss,Crss – pF
Drain-to-Source Voltage, VDS – V

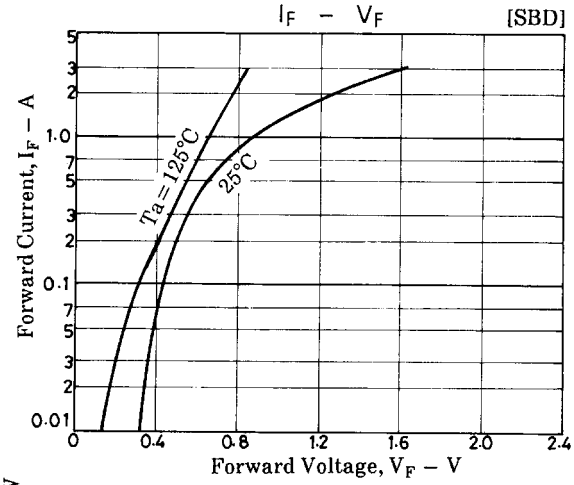

A S O [MOSFET]
IDP
ID
10μs
100μs
1ms
10ms
DC operation
Operation in this area is limited by RDS(on).
Tc=25°C
Single pulse
Drain Current,ID – A
Drain-to-Source Voltage,VDS – V


PD – Ta [MOSFET]
Mounted on ceramic board (750mm2×0.8mm)
Allowable Power Dissipation, PD – W
Ambient Temperature,Ta – °C

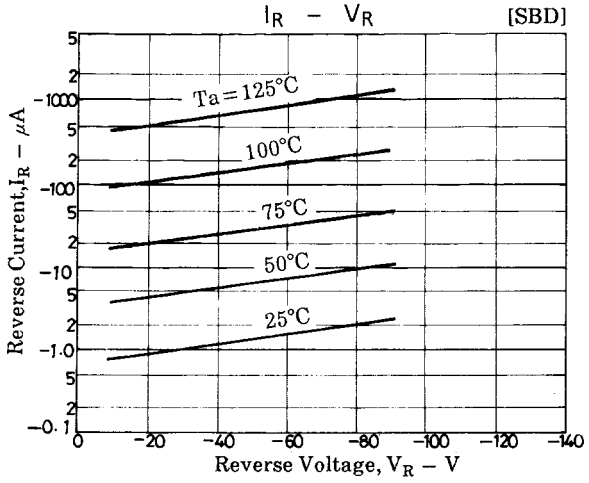
P_D – Tc [MOSFET]



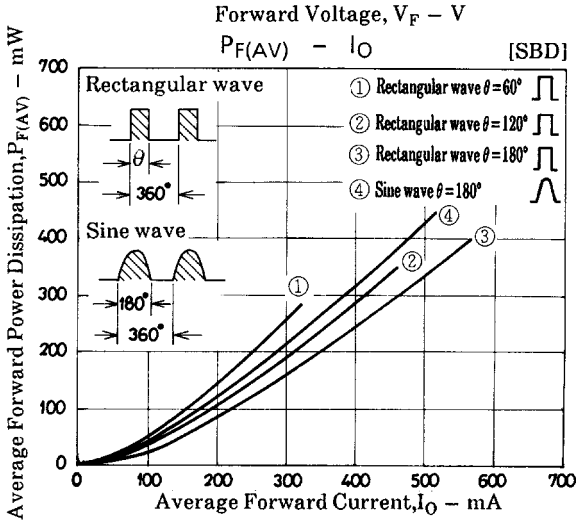
I_F – V_F [SBD]



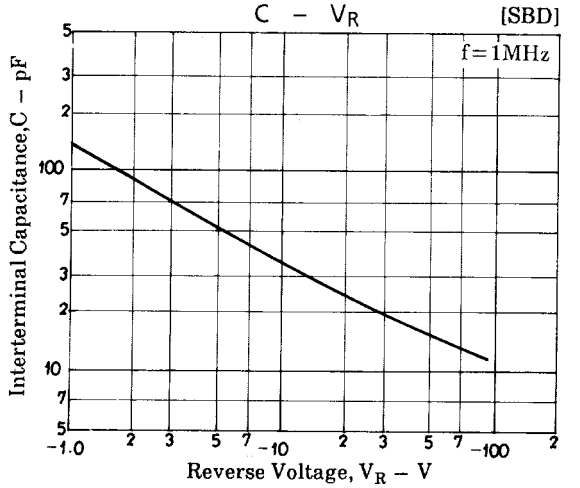
I_R – V_R [SBD]



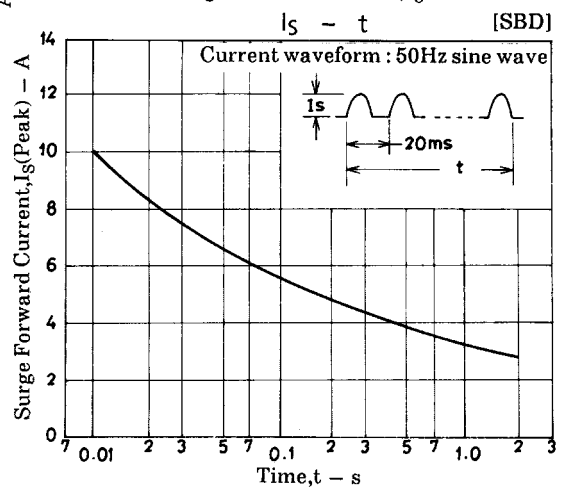
$P_{F(AV)}$ – I_O [SBD]



C – V_R [SBD]



I_S – t [SBD]



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