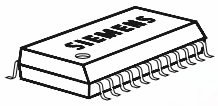
SIEMENS

8 x Digital Sensor Interface

FZE 1658G

Features

- Input protection against 2000 V burst/500 V surge pulse according to IEC 801 4/5
- Input characteristic according to IEC 65 A, type 2 (24 V DC)
- Digital filter
- Serial in/out for easy cascading
- Low power dissipation
- SMD package

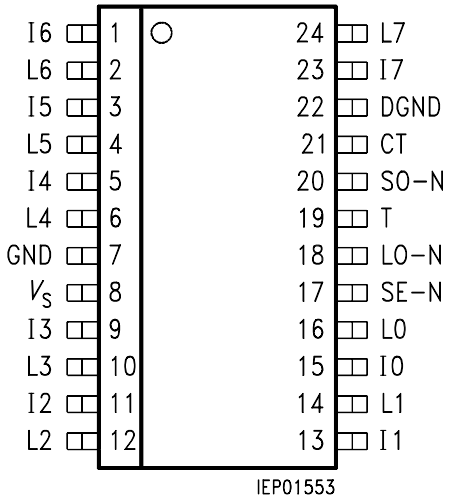


P-DSO-24-1

Type	Ordering Code	Package
FZE 1658G	Q67000-A8361	P-DSO-24-1

The FZE 1658G is an integrated interface for digital sensors - i.e. proximity switches - in industrial automation equipment. The IC has eight integrated highly protected and failsafe inputs with status LED and a serial synchronous output for direct MC-interfacing.

Pin Configuration
(top view)



Pin Definitions and Functions

Pin	Symbol	Function
15, 13, 11, 9, 5, 3, 1, 23	I0 - I7	Inputs for 24-V signals, in conjunction with R_V and R_{EXT} current sink characteristic.
16, 14, 12, 10, 6, 4, 2, 24	L0 - L7	Outputs for the status LEDs; LED lights when H-signal is present at input.
21	CT	Pin for connecting the frequency-determining capacitor for the filter clock; also reset input if CT is connected to DGND.
7	GND	Ground for all 24-V signals, substrate.
22	DGND	Ground for all 5-V signals, no internal connection to GND. Any interruption of GND or DGND with the supply voltage present may result in destruction of the device.
8	V_S	Supply voltage; undervoltage activates internal reset.
20	SO-N	Serial output, open drain.
17	SE-N	Extention input for serial cascading with pull-up current source.
18	LO-N	Latch input, edge H-L results in transfer of data from the digital filters to the output register.
19	T	Clock for serial output, positive edge triggered.

Functional Description and Application

The Integrated circuit FZE 1658G is used to detect the signal states of eight independent input lines according to IEC 65A Type 2 (e.g. two-wire proximity switches) with a common ground (GND). For operation in accordance with IEC 65A, it is necessary for the device to be wired with resistors rated R_V = 820 Ω and R_{EXT} = 4.4 kΩ with ± 2 % tolerance and 200 ppm TK. The input device has the following characteristics:

- Minimization of power dissipation due to constant current characteristic
- Inputs protected against reverse polarity and transient overvoltages
- Status LED output for each input
- Digital averaging of the input signals to suppress interference pulses
- Serial output of the detected signals (cascadable)

Maximum voltage ratings at inputs D0 ... D7 within test circuit 2.

	Voltage Range	**Notes**
DC voltage	– 3 V … + 32 V – 32 V … + 32 V	full function non-destructive, no latch-up
Overvoltage 500 ms	– 3 V … + 35 V – 35 V … + 35 V	full function non-destructive, no latch-up
Overvoltage 1.3 ms to VDE 0160	– 3 V … + 55 V ± 55	full function non-destructive, no latch-up
Surge pulse 50 µs to IEC 801-5, Z_i = 2 Ω	± 0.5 kV	1)
Burst pulse 50 ns to IEC 801-4, Z_i = 50 Ω	± 2 kV	2)

1) Non-destructive in temperature range 15 °C ≤ T_A ≤ 35 °C.

2) In temperature range 15 °C ≤ T_A ≤ 35 °C:
Data retained if the supply voltage remains within the operating range; without supply voltage non-destructive.

The rated voltage may be applied to all inputs simultaneously.

The values given in the table may be regarded as guaranteed, but are only checked as part of a qualification (no 100 % series testing).

Within the application circuit given the same voltage ratings as above apply for the supply line.

Circuit Description

In IEC 65A, the following values are specified for 24-VDC input stages of type 2:

Level	Input Voltage	Input Current
1 0	min. 11 V max. 11 V or max. 5 V	min. 6 mA max. 2 mA

The current in the input circuit is determined by the switching element in state “0” and by characteristics of the input stage in state “1”.

The octal input device FZE 1658G is intended for a configuration comprising two specified external resistors per channel, as shown in the block diagram. As a result the power dissipation within the P-DSO-24-1 package is at a minimum.

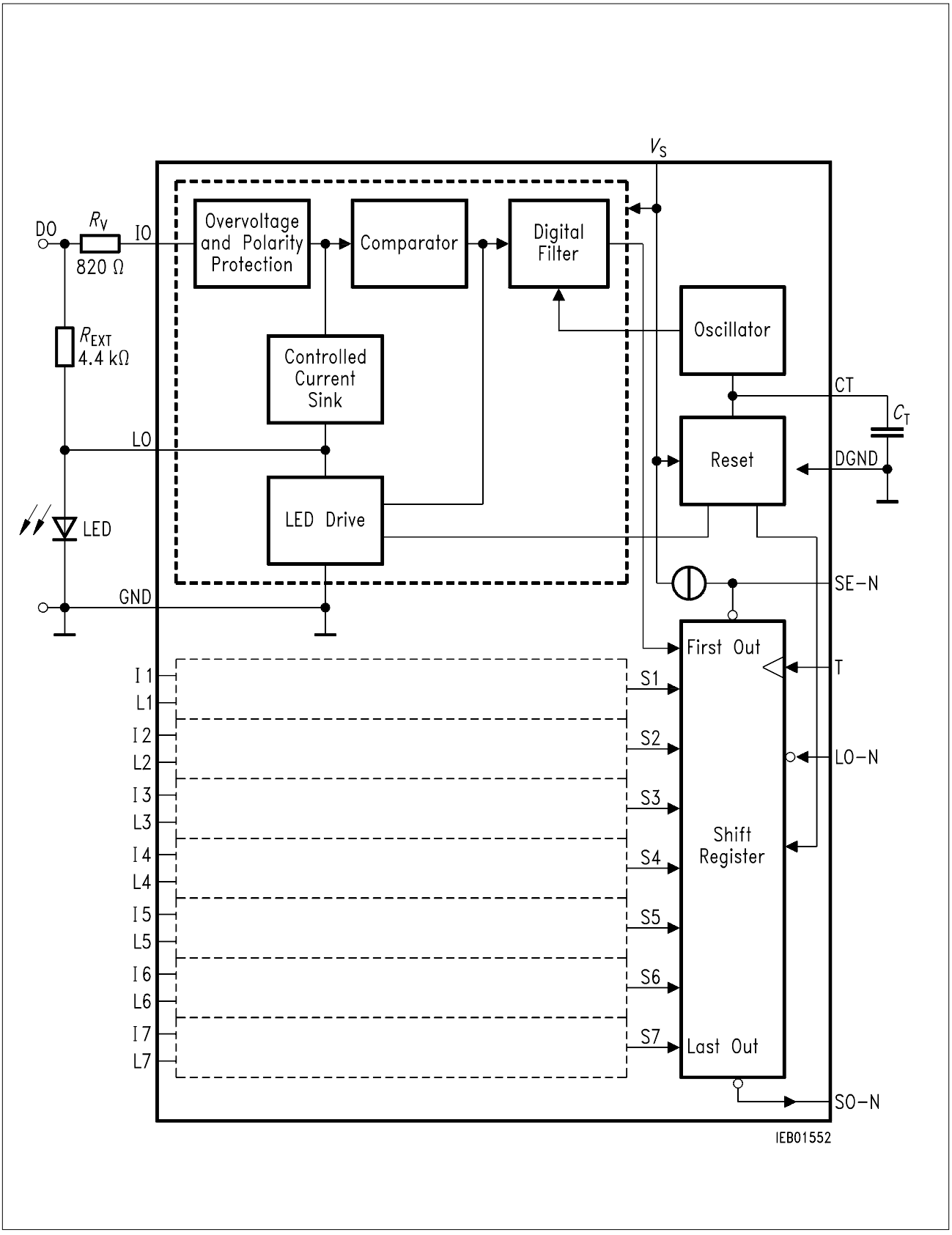
The voltage dependent current through the external resistor R_{EXT} is compensated by a negative differential resistance of the current sink across pins E and L, therefore input D behaves like a constant current sink.

The comparator assigns level 1 or 0 to the voltage present at input E. To improve interference protection, the comparator is provided with hysteresis and a delay element.

A status LED is connected in series with the input circuit (R_{EXT} and current sink). The LED drive short-circuits the status LED if the comparator detects “0”. A constant current sink in parallel with the LED reduces the operating current of the LED, and a voltage limiter ensures that the input circuit remains operational if the LED is interrupted. The specified switching thresholds may change if the LED is interrupted.

For each channel a digital filter is provided which samples the comparator signal at a rate provided by the clock oscillator. The digital filter is designed as a 5-section shift register. If any four out of 5 sampling values are identical, the output S changes to the corresponding state.

On a falling edge at input LO-N, the parallel data S0 - S7 are clocked into the output shift register. The data can be shifted out serially to the output SO-N by the clock signal T, with a “1” at the input being represented by a L-signal at the output SO-N. The serial interface of the shift register fits the synchronous interface of the 8051 microcontroller (**see diagram Serial Data Output Function**). By connecting output SO-N to input SE-N of the next device, several FZE 1658G can be cascaded (**see Application Circuit**). SO-N is designed as an open-drain output. SE-N has an internal pull-up current source. Inputs SE-N, T and SO-N have Schmitt trigger characteristics. The device has separate ground pins for the input circuitry (GND) and for the logic (DGND). If the supply voltage falls below V_{USR} or CT is connected to DGND, the output shift register will be cleared and the output SO-N disabled. If the supply voltage is too low, the LED drives will also be disabled, i.e. the LED lights as soon as current flows in the input circuit.



Block Diagram

Absolute Maximum Ratings
T_j = – 40 to 150 °C

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Transient input current inputs I0 - I7	I_I	– 0.6 – 1.2 – 2.5	0.6 1.2 2.5	A A A	$t_{50\,\%} \leq 50$ µs $t_{50\,\%} \leq 1.2$ µs $t_{50\,\%} \leq 50$ ns
Ground current	I_{GND}	– 5 – 10	5 10	A A	$t_{50\,\%} \leq 50$ µs $t_{50\,\%} \leq 50$ ns
Junction temperature	T_j	– 40	150	°C	
Storage temperature	T_S	– 50	125	°C	
Thermal resistance System/air	R_{thja}		95	K/W	soldered-in
Transient thermal resistance; Same current through all inputs I0 - I7	Z_{th} Z_{th}		0.15 0.4	K/W K/W	50 µs pulse 120 µs pulse
Supply voltage	V_S	– 0.3	65	V	
Ground offset DGND to GND	V_{DGND}	– 4	4	V	$V_{DGND} < V_S$
Current at the LED outputs	I_L	– 15 – 500 – 250 – 125	15 500 250 125	mA mA mA mA	 $t_{50\,\%} \leq 50$ µs $t_{50\,\%} \leq 1.2$ µs $t_{50\,\%} \leq 50$ µs
Voltage at T, LO-N, SO-N, SE-N	V_{LOG}	– 4 – 0.3	9 9	V V	 referred to DGND
Capacitance at CT	C_{CT}		2	µF	when V_S falls below V_{CT}
ESD voltage 100 pF / 1.5 kΩ	V_{ESD}	1000	1000	V	MIL Std. 883 Meth. 3015

All voltages are, unless otherwise specified, referred to GND. This also applies to the operating range and the characteristics.

Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_S	10	48	V	Note power dissipation[1)]
Supply voltage rise	SR_{VS}	– 0.1	1	V/µs	
Supply voltage	V_S-V_{DGND}	9		V	[2)]
GND potential difference	V_{DGND}	– 1.5	1.5	V	
Input terminal current	I_{IT}	– 10	10	mA	
Input voltage SE-N, T, LO-N	V_{IH} V_{IL}	2.8 – 0.5	6 1.7	V V	
Input current SE-N, T, LO-N	I_I	– 1	1	mA	Clamp current
Junction temperature	T_j	– 25	150	°C	
Ambient temperature	T_A	– 25	105	°C	Dependent on R_{th}
Clock frequency	f_T		1	MHz	
Clock pulse width H or L	t_{TH}, t_{TL}	300		ns	
SE-N set up time to T ↑	t_{VSE}	300		ns	
LO-N set up time to T ↑	t_{VLO}	1.2		µs	
SE-N, LO-N, T rise and fall time within thresholds	t_r, t_f		3	µs	[3)]

1) Input voltages may rise before the supply voltage.
Full function at $V_S > V_{VSRO}$ (see Characteristics).

2) Limits GND potential difference at minimum supply voltage.

3) Also applies to several cascaded FZE 1658G (note dependence with clock frequency).

For definition of timing items, see timing diagram.

Characteristics

V_S = 15 V to 30 V; V_{DGND} = 0, T_j = – 25 °C < T_j < 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Inputs I0 - I7 or D0 - D7 Respectively							
Switching threshold H	V_{DH}			10.85 [1]	V		2
Switching threshold L	V_{DL}	8			V	$V_L \leq 2.2$ V	2
Hysteresis	V_{DHY}	1			V	$V_L \leq 2.2$ V	2
Switching threshold L	I_{DLL}	2.5			mA	$I_{LED} = 0$	2
Input current	I_{DH}	6.2 [1]		8	mA	$V_L \leq 3.5$ V, V_D = 11 … 30 V	2
Input current	I_{DL}	5		7	mA	$V_L = V_{LL}$, V_D = 5 V	2
Input current	I_{IC+}			1	mA	V_I = 30 V [2]	1
Input clamp voltage	V_{IT+}	35		75	V	I_I = 10 mA, T_j = 25 °C [2]	1
Input current	I_{IC-}	– 1			mA	V_I = – 30 V [2]	1
Input clamp voltage	V_{IT-}	– 75		– 35	V	I_I = – 10 mA, T_j = 25 °C [2]	1

[1] Headroom to IEC 65 A for tolerance of ext. resistor.

[2] Also valid at V_S = 0.

Characteristics (cont'd)
V_S = 15 V to 30 V; V_{DGND} = 0, T_j = – 25 °C < T_j < 125 °C

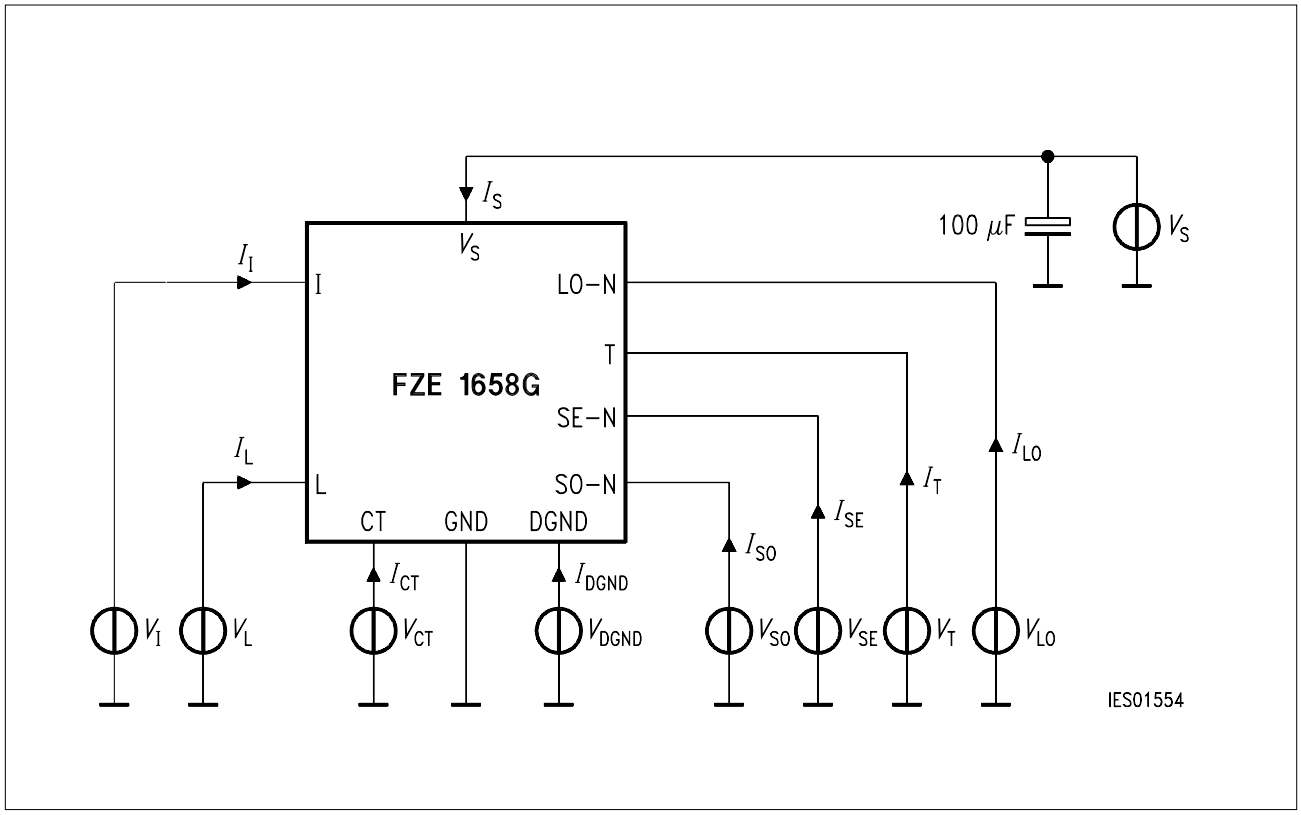
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
LED Drive L0 - L7							
Open-load voltage	V_{LO}	3.5		5	V	V_D = 24 V, I_{LED} = 0	2
"Low"- voltage	V_{LL}	0		0.75	V	V_D = 5 V, I_{LED} = 0	2
Output current	I_{LED}	3		5	mA	V_D = 11 … 30 V, V_L = 1.5 … 3 V	2
Output current	I_{LED}	1.5		6	mA	V_D = 11 … 30 V, V_L = 1.2 … 3.5 V	2
Power down output current	I_L	– 0.12			mA	$V_S < V_{VSRU}$	1
Propagation delay rising and falling edge	t_{DL}	7.5		75	µs	V_D = 12 V ⇆ 7 V	2
Oscillator							
CT source/sink current	I_{CT}	150		250	µA		1
Frequency	f_{CT}	1		1.5	kHz	C_T = 39 nF	2
Upper switching threshold	V_{CTP}	3.3		4.3	V		2
Lower switching threshold	V_{CTN}	1.4		2.2	V		2
Reset threshold	V_{CTR}	0.8		1.4	V		1
Reset input current	I_{CTR}	– 300		– 150	µA	V_{CT} = 0.8 V	1
Signal delay	t_{DFI}	2		4	ms	C_T = 39 nF	2

Characteristics (cont'd)
V_S = 15 V to 30 V; V_{DGND} = 0, T_j = – 25 °C < T_j < 125 °C

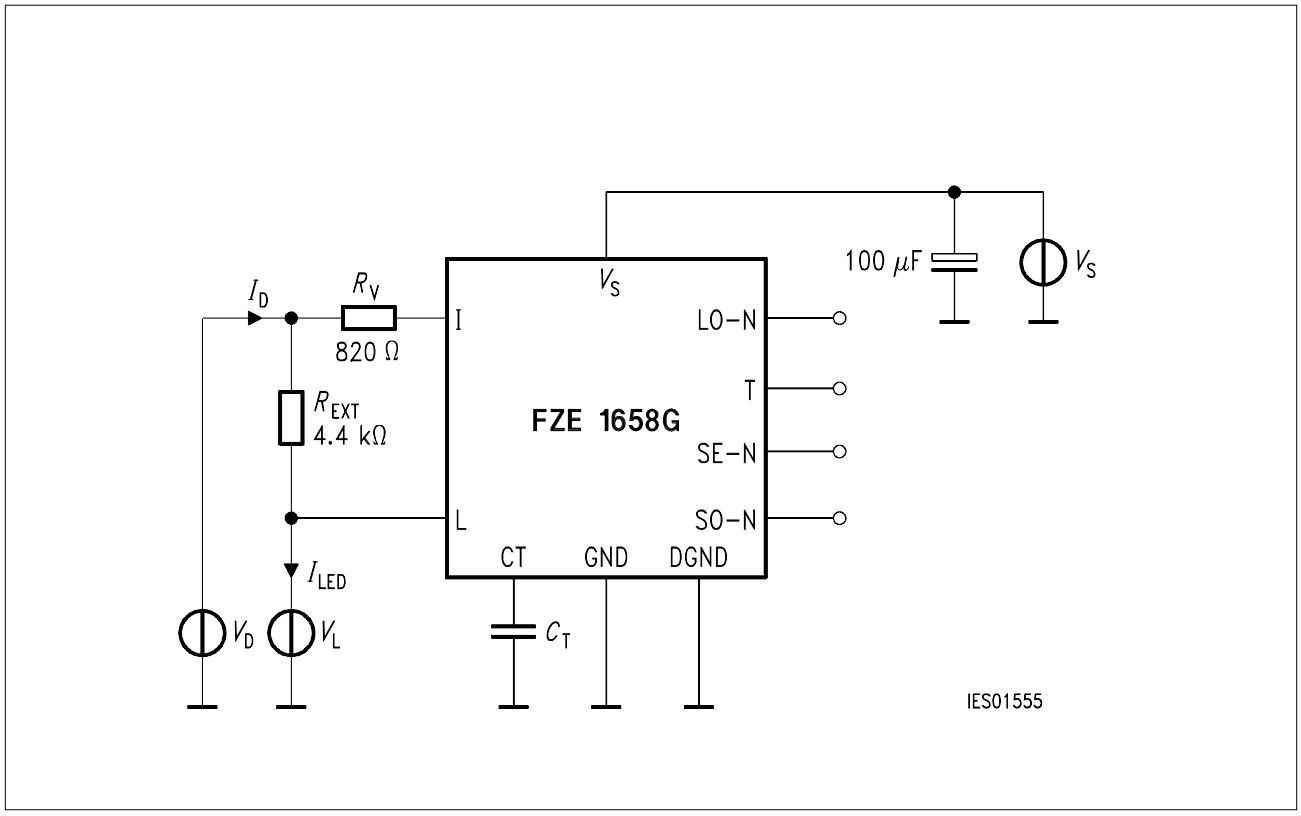
Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
5-V Logic							
Input current T, LO-N	I_I	– 10		10	µA	V_i = 0 … 5 V	1
Input current SE-N	I_{ISE}	– 600		– 400	µA	V_i = 0 … 3 V	1
Input current T, LO-N, SE-N	I_{I0}	0		20	µA	V_i = 0 … 5 V V_S = 0 V	1
Input capacitance	C_I			10	pF		1
L-output current SO-N	I_{SOL}	5.5		8	mA	V_Q = 3 … 5 V	1
L-output level SO-N	V_{SOL}	0		0.5	V	I_{SO} = 2 mA	1
H-leakage current SO-N	I_{SOH}	0		50	µA	V_{SO} = 5 V	1
Output capacitance SO-N	C_{SOH}			20	pF	V_{SO} = 1.5 V	1
Rise/fall time of output current SO-N	t_{rSO}, t_{fSO}			50	ns	V_{SO} = 2.5 V	1
Delay time T to SO-N (see timing diagram)	t_{SOT}			150	ns	V_{SO} = 2.5 V	1
Delay time LO-N to SO-N (see timing diagram)	t_{SOLO}			300	ns	V_{SO} = 2.5 V	1
Hysteresis SE-N, LO-N			60		mV	no 100% testing	

Characteristics (cont'd)
V_S = 15 V to 30 V; V_{DGND} = 0, T_j = – 25 °C < T_j < 125 °C

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			
Hysteresis Clock input			200		mV	no 100% testing	
Voltage Supply							
Current drain static	I_S	2		5	mA	V_S = 10 … 30 V V_{LO-N} = 5 V V_T = 5 V I_{SE-N} = 0	2
Current drain during serial readout	I_S	2		6	mA	V_S = 10 … 40 V V_{LO-N} = 0 V f_T = 1 MHz	2
Current drain during high supply voltage	I_{SMAX}			7	mA	V_S < 45 V	2
Logic ground current	I_{DGND}	– 2.5		0	mA	V_{DGND} = – 1.5 … 1.5 V, LO-N = H	1
Under voltage lockout	V_{VSRO}			10	V	upper switching treshold	2
	V_{VSRU}	8			V	lower switching threshold	2
	V_{VSRH}	0.2			V	hysteresis	2

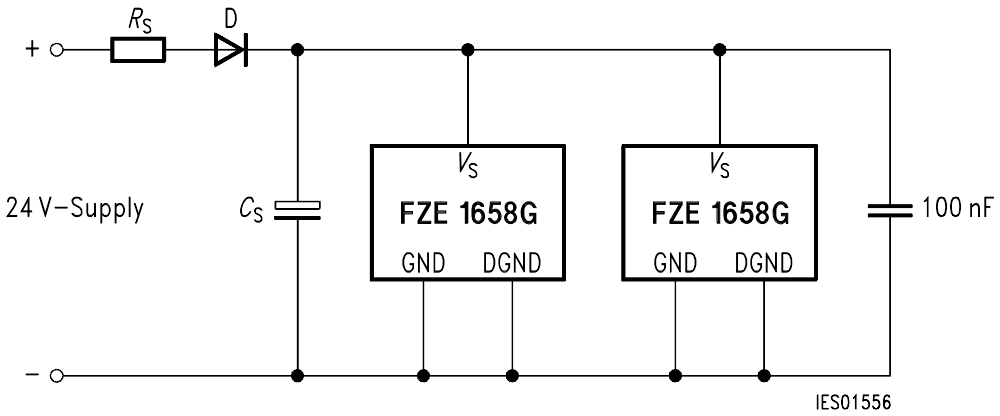


Test Circuit 1



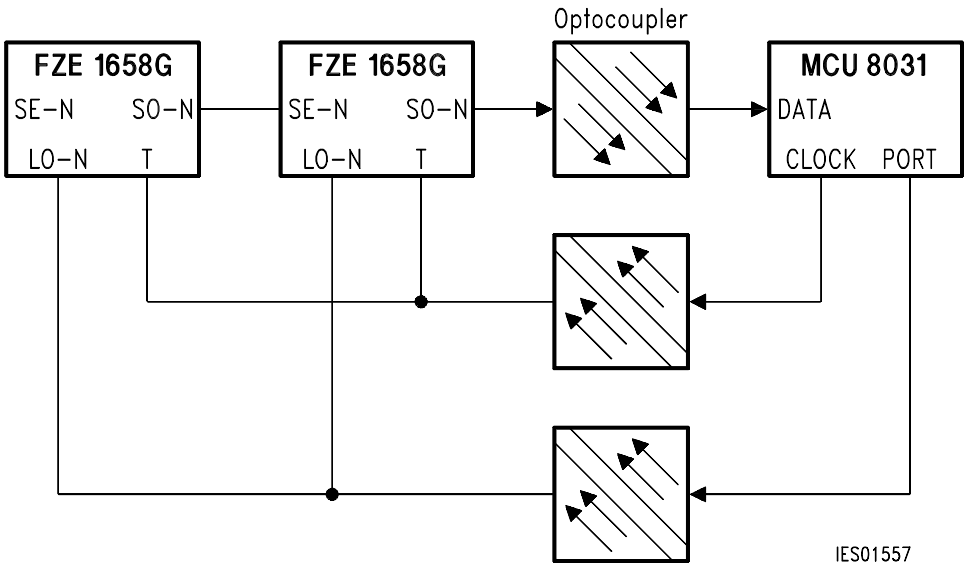
Test Circuit 2

Application Circuit

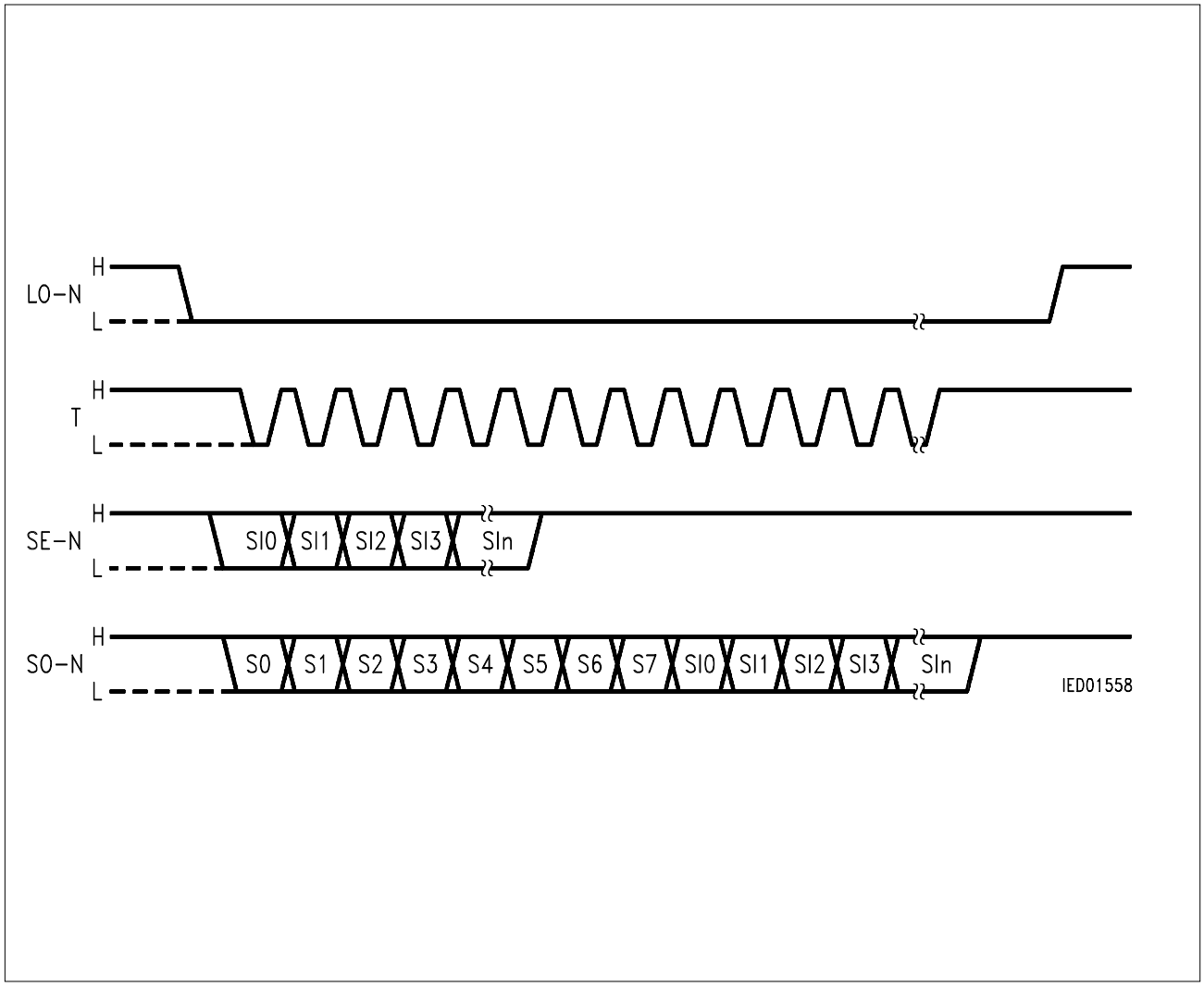


R_S = 820 Ω/number of FZE 1658G
$C_S \geq$ 1.5 ms/R_S 63 V rated voltage
D Reverse polarity protection diode with avalanche capability

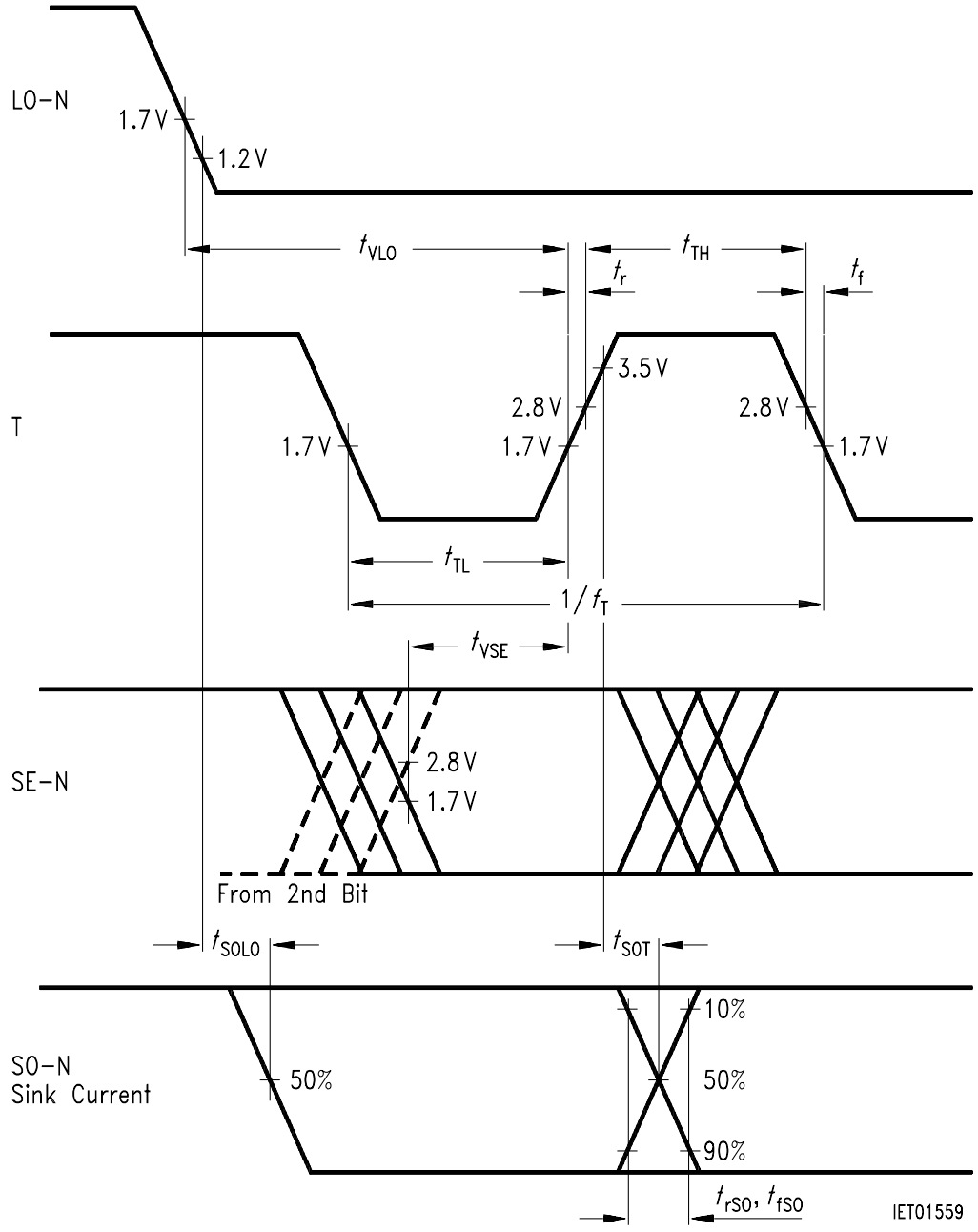
Supply Voltage Decoupling Circuit



Cascading Multiple FZE 1658G

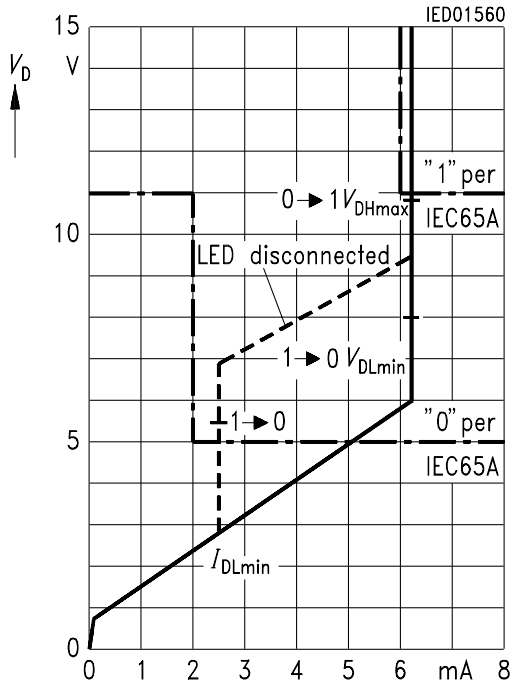


Serial Data Output Function



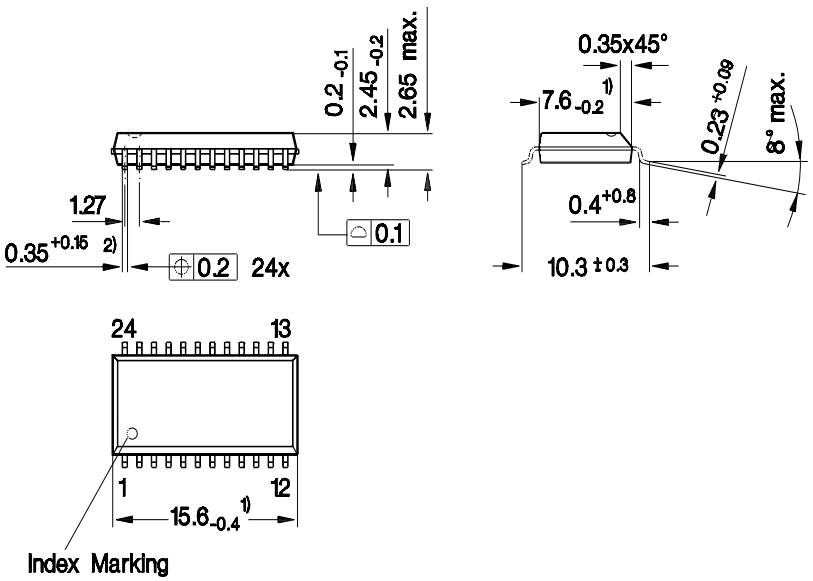
Timing Diagram

Input Characteristic with Worst-Case Values per IEC 65A Input D Rest Circuit D



Package Outlines

Plastic-Package, P-DSO-24-1 (SMD)
(Plastic Dual Small Outline Package)



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion

GPS05144

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm